Post-Implementation Timing Simulation
Objectives

- This tutorial will show you how to run a Post-Implementation timing simulation with Xilinx Vivado and Aldec Active-HDL
Simulation Settings

- In Vivado, after you have implemented your design, click on “Simulation Settings”.
Selecting the Simulator

- First, make sure that the Target Simulator is set to (Aldec) Active-HDL Simulator.
- Next, click on the “Simulation Tab”
Simulator Options

- Click in the box next to `activehdl.simulate.asim.more_options` and type "+access +w_nets" without the quotation marks.
- Click “OK” or “Apply” and close the window.
Now, click on “Run Simulation” and select “Run Post-Implementation Timing Simulation”
Running the Simulation

- Remove the internal signals from the waveform (unless you need them for some reason) and set up the stimulators as you normally would.
- Observe the differences between the behavioral and timing simulations.