ELEC 4200 Lab#5
Hierarchical & Parameterized VHDL Modeling, Simulation & Synthesis
Specifications (1)

- Write a parameterized VHDL model for a rising edge-triggered N-bit universal register/counter with the following specifications in order or precedence:
  - Active high reset (RST)
  - Active high clock enable (CE)
  - Two mode control inputs (M1 & M0)

- Reference the function table below for modes of operation.

- Note: during shift register mode \( Q_{n-1} \leftarrow D_{n-1} \)
Pre-lab Assignment

• Write a PARAMETERIZED VHDL model for the register/counter using the specifications previously mentioned.
• Write a separate VHDL model for the digital one-shot from Lab 4
• Write a hierarchical VHDL model that calls and connects the register/counter model and the digital one-shot.
  – The output of the digital one-shot drives the clock enable (CE)
• Determine the values of N you will use for simulation and design verification
• Determine the FPGA pin numbers you will use for LEDs, push buttons, and switches for both values of N
  – Make a table of these

Note: You should have THREE total VHDL models
Lab Exercise (1)

- Do the following for Each value of N
  - Simulate and verify your register/counter VHDL model
  - Simulate and verify your hierarchical model that combines the register/counter and digital one shot
    » Be sure to take into account how signals propagate through the one-shot
  - Synthesize your design for the Spratan3
    » Record the number of FFs, LUTs, and slices used
    » Put these in a table
  - Demonstrate your working circuit (all modes) to the GTA

- Be sure the GTA sees both values of N
Lab Exercise (2)

- Choose one of you N values and create one of the following circuits by hard coding M1 and M0
  - Counter (M1=1 and M0=0)
  - Shift Register (M1=0 and M0=1)
  - Parallel load register (M1=1 and M0=1)
- Demonstrate your working circuit to the GTA
- Record the number of FFs, LUTs, and slices used
- Repeat the process for the other two modes

Note: RST and CE must still function in each circuit
Note: There are a total of FIVE circuits you must demonstrate
Report Guidelines

• Be sure to include all sections required by the lab manual guidelines. In addition be sure your report includes the following:
  – All verified VHDL models
  – Annotated screenshots of your Aldec HDL simulation results
    » Be sure to describe your testing method
  – Design work (if applicable)
  – Table of synthesis results for each of the five circuits
    » First N value, Second N value, Counter, Shift, Load
  – Answers to the following questions…

1. What values did you choose for N and why?

2. What would be the advantages of choosing the values of 6 & 8 for N when simulating the circuit?