ELEC 4200 Lab#2
Sequential Design Using Schematic Capture

• References you may need:
  • Spartan 3 PCB Reference.pdf
  • Lab #0 Tutorial
Overview

• Design a Moore FSM with
  – 4 states (S0-S3)
  – Active high synchronous reset (RST)
    » Resets the FSM to state S0
    » Take precedence over all other operations
  – Active high synchronous enable (EN)
    » EN=0 → Hold state (unless reset)
    » EN=1 → Cycle to next state on active clock edge
      • S0 → S1 → S2 → S3 → S0
  – 4 active LOW outputs O0-O3.
    » One output for each state
    » i.e: Oi = 0 when FSM is in state Si
  – 2 output (C1 and C0) giving the binary value of the current state
    – (C1 is MSB)
Pre-lab Assignment

• Derive the following
  – State Diagram
  – State Table

• You can use any combination of D and JK flip-flops
  – In schematic capture library the FF’s are “fd” and “fjkc”
  – The clear on the JK FF is asynchronous and must be tied to ground

• Use K-maps to obtain minimized SOP expressions

• Draw a logic diagram
  – Share common product terms and gates if possible
  – Label all inputs and outputs

• Review the following in the Spartan 3 PCB reference manual
  – Chapter 4 (push buttons)
  – Chapter 8 (Clock sources)
    » You will be using the 50MHz clock source.
Lab Exercise

• Capture your design using the ISE schematic capture tool.
  – Try to be neat and compact as we will be adding additional circuitry to the sheet.

• Simulate your circuit in Aldec HDL
  – Your simulation should test every state of the FSM and each feature (next state, reset)
  – Fix any incorrect outputs

• Once your circuit works, add the digital one-shot discussed on the following page to the Enable(EN) input
Digital One-Shot

• Why a digital one-shot?
  – The clock on the board is pulsing at a rate of 50Mhz and any time the enable button is pressed over a clock edge, the FSM will move to the next state. Unless you can press and release the button in $1/50000000^{th}$ of a second (not to mention switch bouncing) you will fly through all of your 4 states. (If all you want is flickering LEDs and to get a “0”—leave it off)

• The digital one-shot will provide a single enable pulse for each push of the push-button as shown in the timing diagram. Study the circuit and the diagram to be sure you understand its function.
Synthesize your design for the Spartan3 FPGA.
- RST  Switch or Push-button
- EN  Connected to push-button via the one-shot
  » With the one-shot the Enable signal is now an internal net and should be connected to the one-shot output. The input of the one-shot should be connected to the push-button
- O0-O3  LED’s

Download and verify you design on the FPGA
- Fix any errors
- Demonstrate to the GTA
Be sure to include all sections required by the lab manual guidelines. In addition be sure your report includes the following:

- Screenshot of you verified schematic (Be sure labels are legible)
- Annotated screenshot of your Aldec HDL simulation results
  - Be sure to describe your testing method
- Design work (truth-tables, k-maps, equations, etc)
- Answers to the following questions…

1. What method did you use to encode the states in the state machine? Some of the possible methods you could have used were binary, gray code, one hot, or one cold.
2. How did this affect the resource usage on the FPGA? What effect would using an alternate encoding method have had on the resource usage of the FPGA?