ELEC 4200 – DIGITAL SYSTEM DESIGN
Spring 2015 – Lecture: Tuesday/Thursday 8:00-8:50am in Broun 306
Lab in Broun 320: Section 001 Monday 4-6:50pm; Section 002 Wednesday 5-7:50pm

Bulletin Data: ELEC 4200. Digital System Design (3) LEC. 2. LAB. 3. Pr. ELEC 2210 and ELEC 2220. Hierarchical, modular design of digital systems; synchronous and asynchronous sequential circuit analysis and design, programmable logic devices and field programmable gate arrays, and circuit simulation for design verification and analysis.


References: On course web page: http://www.eng.auburn.edu/~nelsovp/courses/elec4200/elec4200.html

Coordinator: Victor P. Nelson, Professor of ECE, nelsovp@auburn.edu, Br. 326
GTA: Jordan Richardson, jar0012@tigermail.auburn.edu, Office Br. 468

Course Goals:
1. To be able to analyze and design digital systems in a hierarchical, top-down manner.
2. To be able to model, simulate, verify, and synthesize digital systems using hardware description languages.
3. To be able to realize designs with programmable logic, including FPGAs

Prerequisites by topic:
1. Digital logic design and analysis or switching theory
2. Digital electronics
3. Computer system organization and design

Course Outline:

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<th>Lecture Topic</th>
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<th>Tentative Laboratory Projects</th>
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<td>1</td>
<td>Overview of digital IC design and FPGAs Review of combinational logic circuits</td>
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<td>Lab 0: Introduction to lab hardware and software</td>
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<td>Review of sequential logic circuits Flip-flop/latch implementations; system-level timing issues and analysis</td>
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<td>Lab 1: Schematic capture, simulation and synthesis of combinational logic</td>
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<td>VHDL syntax, entities, architectures</td>
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<td>Lab 2: Schematic capture, simulation and synthesis of sequential logic</td>
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<td>4</td>
<td>VHDL concurrent and sequential constructs</td>
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<td>Lab 3: VHDL modeling, simulation and synthesis of combinational logic</td>
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<td>VHDL modeling guidelines and parameterization, Test #1</td>
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<td>Lab 4: VHDL modeling, simulation and synthesis of sequential logic</td>
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<td>VHDL hierarchical design and test benches</td>
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<td>VHDL data type definitions</td>
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<td>Lab 6: VHDL parameterized register file with hierarchical modeling and test bench for design verification</td>
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<td>VHDL FSM modeling and simulation</td>
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<td>Lab 7: VHDL hierarchical modeling, simulation and synthesis of manually controlled display system</td>
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<td>PicoBlaze microcontroller architecture, operation, instruction set.</td>
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<td>Computer input/output functions. Test #2</td>
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<td>Lab 9: PicoBlaze serial/interrupting interface</td>
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<td>Programmable logic arrays, programming technologies and interfaces</td>
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<td>Lab 10 (multi-week): VHDL hierarchical modeling, simulation and synthesis of PicoBlaze controlled display system</td>
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<td>FPGA and PLD/CPLD architectures and operation</td>
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<td>Introduction to Verilog</td>
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<td>Boundary scan interface</td>
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<td>Final Exam: Tuesday May 5, 8:00-10:30am</td>
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Typical methods for evaluating student performance:

Hour quizzes (2)  40%
Final exam  20%
Lab projects  40%

Computer usage: VHDL modeling, simulation, and synthesis assignments will require the use of *Aldec Active-HDL* and *Xilinx ISE* computer-aided design (CAD) tools. Some information regarding these tools is available on the ELEC 4200 class web page link listed above. Designs will be downloaded and tested on Digilent/Xilinx Spartan 3 FPGA development boards.

Laboratory Assignments: All laboratory exercises are to be done individually. Each lab will be graded on a 50-point scale, with 10 points for pre-lab work, 10 points for in-lab work, and 20 points for the lab report. Lab assignments (pre-lab and lab reports) and projects must be turned in on or before the designated date/time to receive credit. Pre-lab assignments will be checked at the start of each lab session. Lab reports are due at the beginning of the lab session following the scheduled date for that lab exercise.

Guidelines and format for lab reports: The required content and format of the lab reports is contained in the “ELEC 4200 Digital System Design Lab” handout, available on the course web page.

Academic Honesty Policy: All portions of the Auburn University student academic honesty code (Title XII) found online at [http://www.auburn.edu/academic/provost/academicHonesty.html](http://www.auburn.edu/academic/provost/academicHonesty.html) apply to this class.

> Note that each student is expected to do his/her own laboratory project. Discussion of various aspects of the project with fellow students is acceptable, provided that designs are not copied. Copied work will be considered a violation of the academic honesty code, and dealt with accordingly.

Class attendance: Students are expected to attend class regularly and on time as indicated by the Auburn University “Policy on Class Attendance”. In case of absence, the student is responsible for all course business conducted in class. Make-up exams will be scheduled for excused absences covered by Paragraph 4 of the AU “Policy on Class Attendance”.

Policy on unannounced quizzes: There will be no unannounced quizzes.

Accommodations: Students who need accommodations should initiate the process by first making an appointment with The Program for Students with Disabilities, 1244 Haley Center, 844-2096 (V/TT).

Contribution of course to meeting the professional component

- Engineering topics: 3 credits
  - 33% engineering science (1 credit)
  - 67% engineering design (2 credits)

Primary program outcomes related to this course:

- Outcome 1. Ability to apply knowledge of math, science and engineering to solve problems.
- Outcome 2. Ability to apply in-depth knowledge in one or more disciplines
- Outcome 3. Ability to design an electrical component or system to meet desired needs.
- Outcome 6. Proficiency in the use of computers and other modern tools to solve engineering problems.
- Outcome 8. Proficiency in communicating ideas and information orally and in writing.

Prepared by: V. P. Nelson  Date: January 14, 2015