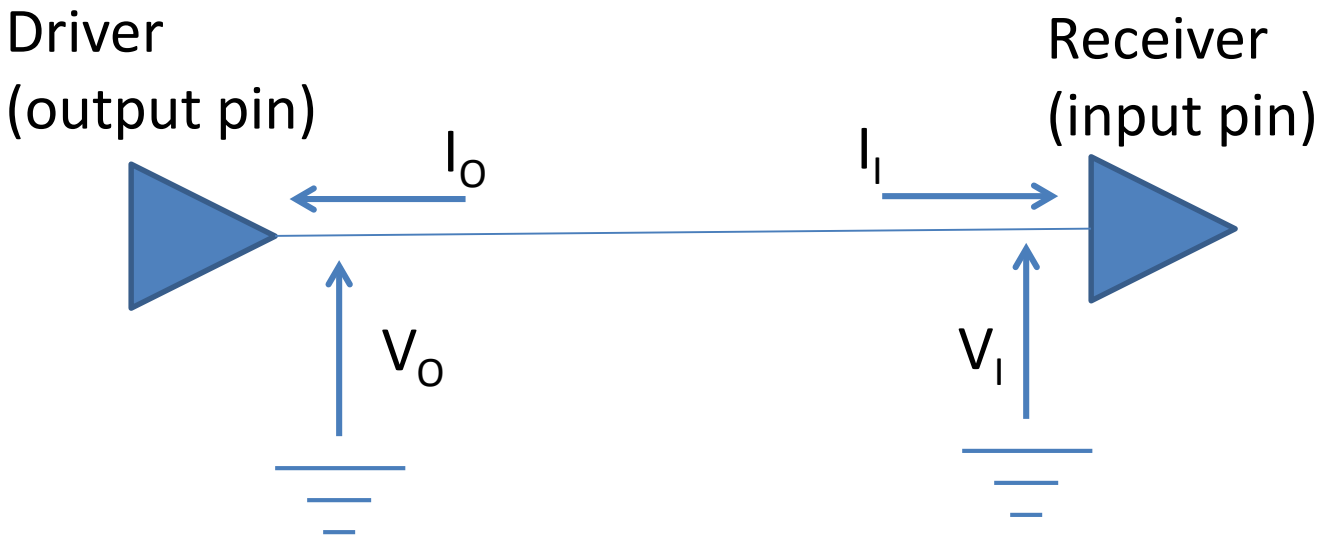
Digital system voltages/currents

And reading component data sheets

Logical vs. electrical values



Output Voltages for Logic Levels

High state/Logic 1: $\mathbf{V_O > V_{OH}}$ (V_{OH} is minimum output voltage for high/1 state)

Low state/Logic 0: $\mathbf{V_O < V_{OL}}$ (V_{OL} is maximum output voltage for low/0 state)

Input Voltage Thresholds for Logic Levels

High state/Logic 1: $\mathbf{V_I > V_{IH}}$ (V_{IH} is minimum voltage interpreted as logic high/1)

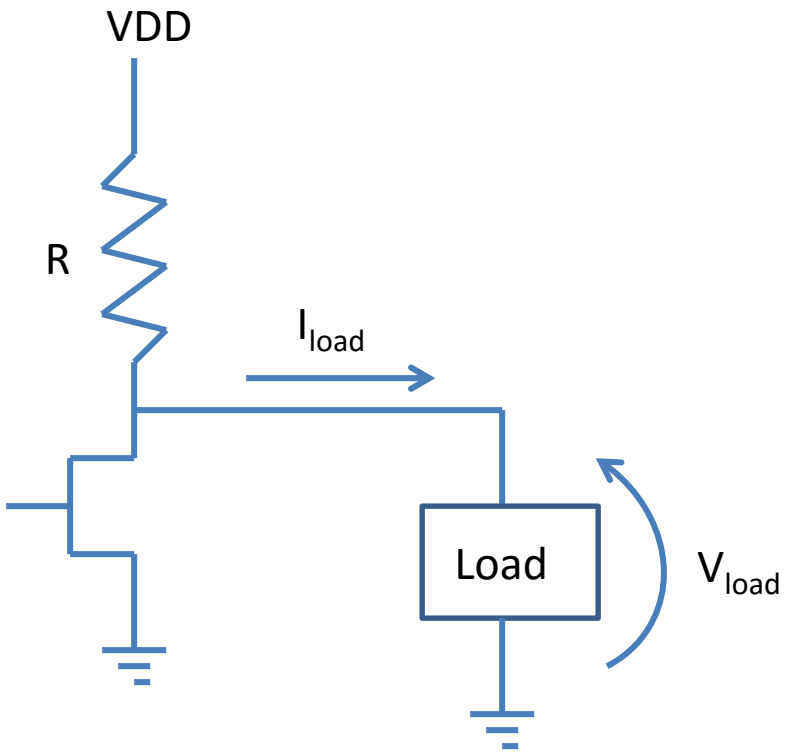
Low state/Logic 0: $\mathbf{V_I < V_{IL}}$ (V_{IL} is maximum voltage interpreted as logic low/0)

"Noise Margin"- allow logic level to be correct despite some voltage variation

High state/Logic 1: $\mathbf{V_{OH} = V_{IH} + V_{noise}}$ (noise doesn't pull voltage below threshold)

Low state/Logic 0: $\mathbf{V_{OL} = V_{IL} - V_{noise}}$ (noise doesn't pull voltage above threshold)

Digital output pin drivers



Logic 0: transistor ON = short ckt
(pin sinks current)
$V_{load} \approx 0 = R_{ON} * I_{load}$

Logic 1: transistor OFF = open ckt
(pin sources current)
$V_{load} = VDD - R * I_{load}$

If I_{load} too large (too much "load")
$V_{load} > V_{IL}$ (logic 0)
or $V_{load} < V_{IH}$ (logic 1)

Load has: Resistance - affects I_{load}
Capacitance – affects V_{load} rise/fall times

Voltage standards

- Specify V_{OH}, V_{OL}, V_{IH}, V_{IL} levels for design
- TTL Standard:
  - V_{IH} = 2.0v, V_{OH} = 2.4v
  - V_{IL} = 0.8v, V_{OL} = 0.4v
  - Unpredictable results for 0.8v < V_I < 2.0v
- STM32L100RC microcontroller I/O pins (from data sheet)
  - $V_{IH} \geq 0.7 \times VDD$ = 2.1v (VDD = 3v)
  - $V_{IL} \leq 0.3 \times VDD$ = 0.9v (VDD = 3v)
- EEBoard DIO outputs (logic high)
  - DIO pin connected to GPIO pin = 3.01v
  - DIO drivers operate with 3.3v supply

Below, or too close to VIH if uC VDD = 5v. May produce undesirable Results.

STM32L100RC Data Sheet Voltage Characteristics

- Absolute max ratings, to prevent “damage”

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} – 0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.10*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 10* for maximum allowed injected current values.

Discovery board: $V_{DD} = V_{DDA} = 3v$

$V_{SS} = V_{SSA}$ = ground

STM32L100RC Data Sheet Current Characteristics

- Absolute max ratings, to prevent “damage”

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	80	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	80	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$I_{INJ(PIN)}$ (2)	Injected current on five-volt tolerant I/O(3)	+0 /-5	
	Injected current on any other pin (4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

Discovery board: I_{VDD} can be supplied by USB

STM32L100RC Data Sheet Electrical Characteristics

- Operating conditions – for “normal operation”

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	32	
f_{PCLK2}	Internal APB2 clock frequency		0	32	
V_{DD}	Standard operating voltage	BOR detector enabled, at power on	1.8	3.6	V
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA} (1)	Analog operating voltage	Must be the same voltage as V_{DD} (2)	1.8	3.6	V

Discovery board: $V_{DD} = V_{DDA} = 3v$

$V_{SS} = V_{SSA}$ = ground

STM32L100RC Data Sheet Electrical Characteristics

- GPIO pin static characteristics (input pins)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{SS} - 0.3	-	0.8	V
V_{IH}	Standard I/O input high level voltage		2(1)	-	V_{DD}+0.3	
	FT(2) I/O input high level voltage			-	5.5V	
V_{IL}	Input low level voltage	CMOS ports 1.8 V ≤ V_{DD} ≤ 3.6 V	–0.3	-	$0.3V_{DD}$(3)	
V_{IH}	Standard I/O Input high level voltage	CMOS ports 1.8 V ≤ V_{DD} ≤ 3.6 V		-	V_{DD}+0.3	
	FT(5) I/O input high level voltage	CMOS ports 1.8 V ≤ V_{DD} ≤ 2.0 V	0.7 V_{DD}(3)(4)	-	5.25	
		CMOS ports 2.0 V ≤ V_{DD} ≤ 3.6 V		-	5.5	

2.1v 0.9v

for V_{DD} = 3v

These are compatible with EEBoard DIO drivers

STM32L100RC Data Sheet Electrical Characteristics

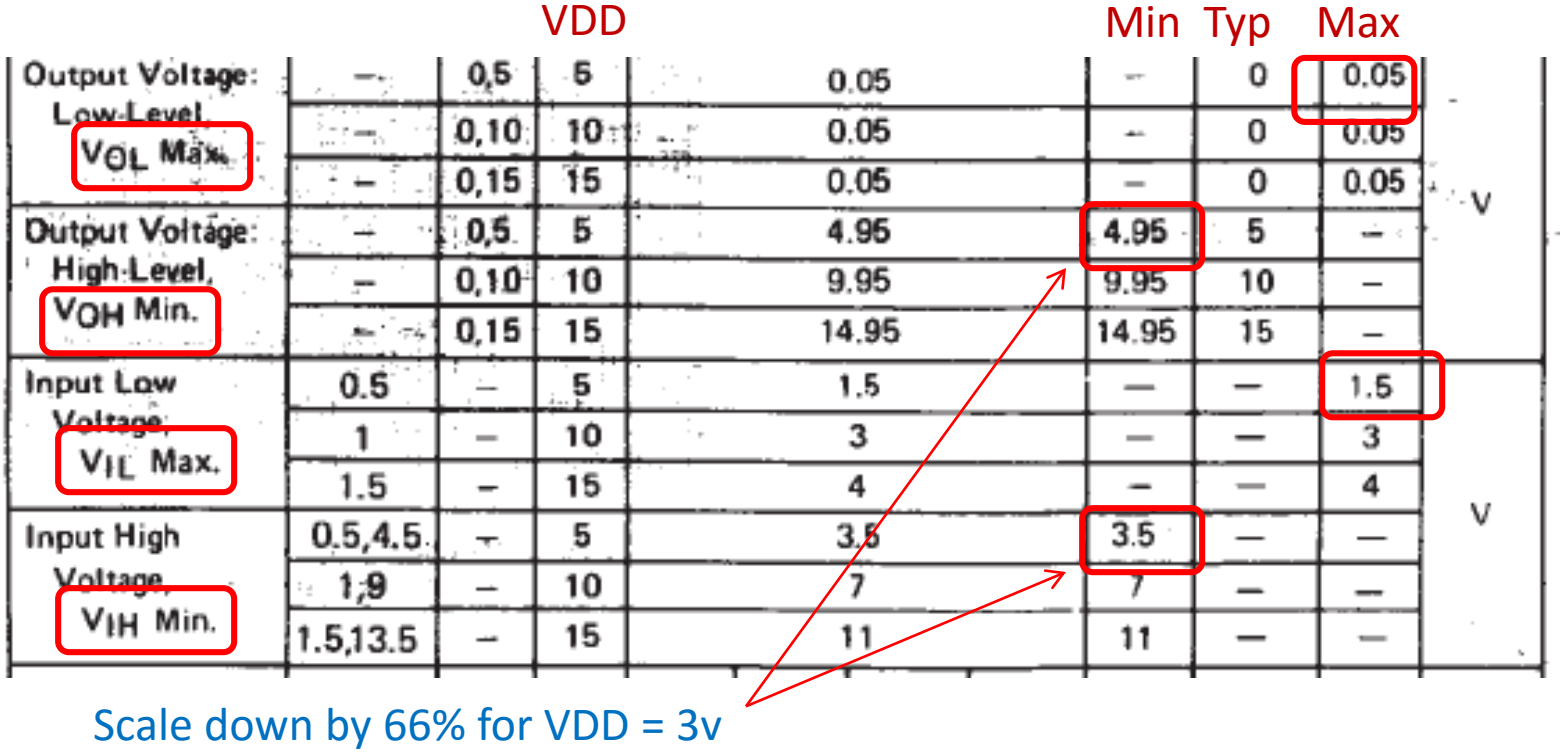
- GPIO pin static characteristics (output pins)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)(2)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (3)(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} =+ 4 mA 1.8 V < V_{DD} < 2.7 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}-0.45	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin when 4 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin when 4 pins are sourced at same time		V_{DD}-1.3	-	

Vout depends on loading conditions

CD4082B dual 4-input AND gates

- VDD levels from 3v to 18v
- I/O voltages compatible with STM32L100RC



			VDD		Min	Typ	Max	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05	–	0	0.05	V
	–	0,10	10	0.05	–	0	0.05	
	–	0,15	15	0.05	–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95	4.95	5	–	
	–	0,10	10	9.95	9.95	10	–	
	–	0,15	15	14.95	14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5	–	5	1.5	–	–	1.5	V
	1	–	10	3	–	–	3	
	1.5	–	15	4	–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5	3.5	–	–	
	1,9	–	10	7	7	–	–	
	1.5,13.5	–	15	11	11	–	–	

Scale down by 66% for VDD = 3v