Programmable Logic Devices & Field-Programmable Gate Arrays

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Text: Chapter 5 (combinational)
Chapter 11 (sequential)
History of Programmable Logic

- **Programmable Logic Arrays ~ 1970**
  - Incorporated in VLSI devices
  - Can implement any set of SOP logic equations
    - Outputs can share common product terms

- **Programmable Logic Devices ~ 1980**
  - MMI Programmable Array Logic (PAL)
    - 16L8 – combinational logic only
      - 8 outputs with 7 programmable PTs of 16 input variables
    - 16R8 – sequential logic only
      - 8 registered outputs with 8 programmable PTs of 16 input variables
  - Lattice 16V8
    - 8 outputs with 8 programmable PTs of 16 input variables
      - Each output programmable to use or bypass flip-flop
  - Complex PLDs – arrays of PLDs with routing network

- **Field Programmable Gate Arrays ~ 1985**
  - Xilinx Logic Cell Array (LCA)

- CPLD & FPGA architectures became similar ~ 2000
Programming Technologies

- PLAs were mask programmable
- PALs used fuses for programming
- Early PLDs & CPLDs used floating gate technology
  - Erasable Programmable Read Only Memory (EPROM)
    - Ultra-violet erasable (UVEPROM)
    - Electrically erasable (EEPROM)
    - Flash memory came later and was used for CPLDs
- FPGAs used RAM for programming
- Later trends
  - Fuses were replaced with anti-fuses
    - Better reliability
  - Large CPLDs went to RAM-based programming
Programmable logic array structure

Implement sum of products logic expressions

Each one “product” of the inputs

Each one “sum” of the products
NOR function in programmable logic

$X_i = 0$ turns transistor OFF (transistor = open circuit)
$X_i = 1$ turns transistor ON (transistor shorts $Z$ to ground/0)
$+V$ pulls $Z$ up to 1 if not shorted to ground

Truth Table:

<table>
<thead>
<tr>
<th>X1</th>
<th>X2</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- both transistors OFF/Z pulled up to $+V$
- transistor 2 ON/shorts $Z$ to ground
- transistor 1 ON/shorts $Z$ to ground
- both transistors ON/short $Z$ to ground

Manipulate sum of products form to use NOR-NOR structures
PLA with 3 inputs/5 products/4 sums

<table>
<thead>
<tr>
<th>Product Term</th>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$A$</td>
<td>$B$</td>
</tr>
<tr>
<td>$A'B'$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$AC'$</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>$B$</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>$BC'$</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>$AC$</td>
<td>1</td>
<td>—</td>
</tr>
</tbody>
</table>
Compact representation of previous PLA circuit
PLD Basic Structure

- Programmable product terms (AND plane)
  - AND gates can connect to any input/FF bit or bit-bar
- Fixed OR plane determine maximum # PTs
- Programmable macrocell
  - XOR gate selects SOP or POS for fewer PTs
  - FF for sequential logic or bypass for combinational logic
  - Feedback current state into array for FSM design

Inputs and Current State from FFs (Bit & Bit-Bar)
Full adder with a PAL
PALs

16L8 – combinational logic

- 10 to 16 inputs, each with true and complement signal
- 2 to 8 outputs, each with
  - 7 product terms can AND any of up to 16 inputs or their complements
  - Tri-state control product term for inverting output buffer
- When output in tri-state, I/O pin can be used as input
- High impedance output with no signal driven
PALs

16R8 – sequential logic

- 8 inputs, each with true & complement
- 8 outputs, each with
  - D flip-flop
    - With feedback for FSMs
- 8 product terms that can AND any of:
  - 8 inputs or their complements
  - 8 feedbacks or their complements from D flip-flops
- One clock for all FFs
- One tri-state control for all outputs
Sequential circuit with a PAL
PLDs

22V10 replaced all PALs
- Combinational and/or sequential logic
  - Macrocell program bits C0, C1
- Up to 22 inputs w/complement
- Up to 10 outputs, each with
  - Macrocell
  - 8-16 product terms
  - Tri-state control product term
- Global
  - preset & clear PTs
  - clock
CPLD implementation of a Mealy machine
CPLDs

- An array of PLDs
  - Global routing resources for connections
    - PLDs to other PLDs
    - PLDs to/from I/O pins
- Example: Cypress 39K
  - Each Logic Block (LB) similar to a 22V10
  - Each cluster of 8 LBs has two 8K RAMs & one 4K dual-port RAM/FIFO
    - Programmable Interconnect Modules (PIMs) provide interconnections
  - Array of up to 24 clusters with global routing
Altera MAX architecture (PAL-based logic modules)
Basic FPGA architecture

programmable basic logic cell

programmable input/output cell

programmable interconnect
Basic FPGA Operation

- Writing configuration memory \(\Rightarrow\) defines system function
  - Input/Output Cells
  - Logic in PLBs
  - Connections between PLBs & I/O cells
- Changing configuration memory data \(\Rightarrow\) changes system function
  - Can change at anytime
  - Even while system function is in operation
Programmable ASIC logic cells

- Chip contains an array of basic logic cells
- Xilinx: “configurable logic block” (CLB) contains
  - SRAM lookup tables (LUTs) to implement combinational logic
  - D flip flops
  - Multiplexers to establish paths in the CLB
- Actel “ACT”: multiplexers implement logic
- Altera “Flex”: similar to Xilinx CLB
- Altera “MAX”: PALs implement logic
Actel ACT architecture (Fig. 5.1) (mux-based logic modules)
Xilinx FPGAs

- **Virtex and Spartan 2**
  - Array of 96 to 6,144 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 FF/latches
  - 4 to 32 4K-bit dual-port RAMs

- **Virtex II, Virtex II Pro**
  - Array of 352 to 11,204 PLBs
    - 8 LUTs/RAMs (4-input)
    - 8 FF/latches
  - 12 to 444 18K-bit dual-port RAMs
  - 12 to 444 18×18-bit multipliers
  - 0 to 2 PowerPC processor cores

- **Virtex 4**
  - Array of 1,536 to 22,272 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 LUTs (4-input)
    - 8 FF/latches
  - 48 to 552 18K-bit dual-port RAMs
    - Also operate as FIFOs
  - 32 to 512 DSP cores include:
  - 0 to 2 PowerPC processor cores

- **Spartan 3**
  - Array of 192 to 8,320 PLBs
    - 4 LUTs/RAMs (4-input)
    - 4 LUTs (4-input)
    - 8 FF/latches
  - 4 to 104 18K-bit dual-port RAMs
  - 4 to 104 18×18-bit multipliers
Xilinx Spartan 3 Family Architecture

Digital Clock Manager → DCM → IOB

Notes:
1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.
## Xilinx “Spartan” FPGAs

<table>
<thead>
<tr>
<th>Spartan Family*</th>
<th>Gates</th>
<th>I/Os</th>
<th>Block RAM</th>
<th>Embedded Multipliers</th>
<th>DCM**</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spartan-3E</td>
<td>1.6M</td>
<td>376</td>
<td>648Kb</td>
<td>36 18x18</td>
<td>8</td>
<td>3.3V - 1.2V†</td>
</tr>
<tr>
<td>Spartan-3</td>
<td>5M</td>
<td>784</td>
<td>1872Kb</td>
<td>104 18x18</td>
<td>4</td>
<td>3.3V - 1.2V†</td>
</tr>
<tr>
<td>Spartan-3L</td>
<td>4M</td>
<td>633</td>
<td>1728Kb</td>
<td>96 18x18</td>
<td>4</td>
<td>3.3V - 1.2V†</td>
</tr>
<tr>
<td>Spartan-IIIE</td>
<td>600K</td>
<td>514</td>
<td>288Kb</td>
<td>–</td>
<td>4</td>
<td>3.3V - 1.5V†</td>
</tr>
<tr>
<td>Spartan-II</td>
<td>200K</td>
<td>284</td>
<td>56Kb</td>
<td>–</td>
<td>4</td>
<td>3.3V - 1.5V†</td>
</tr>
<tr>
<td>Spartan-XL</td>
<td>40K</td>
<td>224</td>
<td>25Kb</td>
<td>–</td>
<td>–</td>
<td>3.3V</td>
</tr>
</tbody>
</table>

*Note: * indicates a revision or a specific model within the family.

**DCM**: Digital Clock Manager

†Voltage range indicates the ability to operate at lower voltages for power savings.
### Xilinx FPGA families (2013)

**FPGA Comparison Table**

<table>
<thead>
<tr>
<th></th>
<th>Spartan-6</th>
<th>Artix-7</th>
<th>Kintex-7</th>
<th>Virtex-7</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic Cells</strong></td>
<td>150,000</td>
<td>215,000</td>
<td>480,000</td>
<td>2,000,000</td>
</tr>
<tr>
<td><strong>BlockRAM</strong></td>
<td>4.8Mb</td>
<td>13Mb</td>
<td>34Mb</td>
<td>68Mb</td>
</tr>
<tr>
<td><strong>DSP Slices</strong></td>
<td>180</td>
<td>740</td>
<td>1,920</td>
<td>3,600</td>
</tr>
<tr>
<td><strong>DSP Performance</strong></td>
<td>140GMACs</td>
<td>930GMACs</td>
<td>2,845GMACs</td>
<td>5,335GMACs</td>
</tr>
<tr>
<td><strong>Transceiver Count</strong></td>
<td>8</td>
<td>16</td>
<td>32</td>
<td>95</td>
</tr>
<tr>
<td><strong>Transceiver Speed</strong></td>
<td>3.2Gb/s</td>
<td>6.6Gb/s</td>
<td>12.5Gb/s</td>
<td>23.05Gb/s</td>
</tr>
<tr>
<td><strong>Total Transceiver Bandwidth</strong></td>
<td>50Gb/s</td>
<td>211Gb/s</td>
<td>800Gb/s</td>
<td>2.784Gb/s</td>
</tr>
<tr>
<td><strong>Memory Interface</strong></td>
<td>800Mb/s</td>
<td>1,066Mb/s</td>
<td>1,866Mb/s</td>
<td>1,866Mb/s</td>
</tr>
<tr>
<td><strong>PCI Express® Interface</strong></td>
<td>x1 Gen1</td>
<td>x4 Gen2</td>
<td>x8 Gen2</td>
<td>x8 Gen3</td>
</tr>
<tr>
<td><strong>Analog Mixed Signal (AMS)/XADC</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Configuration Signal</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>I/O Pins</strong></td>
<td>576</td>
<td>500</td>
<td>500</td>
<td>1,200</td>
</tr>
<tr>
<td><strong>I/O Voltage</strong></td>
<td>1.2V, 1.5V, 1.8V, 2.5V, 3.3V</td>
<td>1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V</td>
<td>1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V</td>
<td>1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V</td>
</tr>
<tr>
<td><strong>EasyPath™ Cost Reduction Solution</strong></td>
<td>-</td>
<td>-</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Digikey.com (11/15/13):**
- Spartan3 XC3S50A: $6.10
- Spartan6 XC6SLX4: $10.90
- Virtex7 XC7V2000T: $39,452.20
In this diagram, the Spartan-6 LX45 FPGA is used in an automotive infotainment system. The FPGA supports audio/video acceleration, graphics subsystem, and vehicle networking functions. The diagram illustrates the integration of various components such as ADC, Host DSP/µC, and Video Input interfaces, among others.
Xilinx: Basic CLB Architecture

- Look-up Table (LUT) implements truth table
- Memory elements:
  - Flip-flop/latch
  - Some FPGAs - LUTs can also implement small RAMs
- Carry & control logic implements fast adders/subtractors
Look-up Tables

- Configuration memory holds outputs for truth table.
- Internal signals connect to control signals of multiplexers to select value of truth table for any given input value.
A Simple PLB

Two 3-input LUTs
- Can implement any 4-input combinational logic function

1 flip-flop
- Programmable:
  - Active levels
  - Clock edge
  - Set/reset

22 configuration memory bits
- 8 per LUT
  - C0-7
  - S0-7
- 6 controls
  - CB0-7
Example PLB

- ¼ of a PLB (called a slice) from Xilinx Spartan 3
  - Two 4-input Look-Up Tables (LUTs)
    - Can perform any combinational logic function of up to 4 inputs
    - Can function as small RAM (16x1-bit) or shift register (up to 16-bit)
  - Two D-type flip-flops
    - Programmable as level sensitive latches
    - Programmable clock edge, clock enable, set/reset
  - Extra logic
    - Fast carry for adders
    - MUXs for Shannon expansion
    - And more
Functions of more variables than # of LUT inputs
Input/Output Cells

- Bi-directional buffers
  - Programmable for input or output
  - Tri-state control for bi-directional operation
  - Flip-flops/latches for improved timing
    - Set-up and hold times
    - Clock-to-output delay
  - Pull-up/down resistors
- Routing resources
  - Connections to core of array
- Programmable I/O voltage & current levels
Interconnect Network

- Wire segments of varying length
  - \( xN \) = \( N \) PLBs in length
    - 1, 2, 4, and 6 are most common
  - \( xH \) = half the array in length
  - \( xL \) = length of full array

- Programmable Interconnect Points (PIPs)
  - Also known as Configurable Interconnect Points (CIPs)
  - Transmission gate connects to 2 wire segments
  - Controlled by configuration memory bit
    - 0 = wires disconnected
    - 1 = wires connected
Xilinx interconnect structures

(a)

(b)

(c)
Spartan 3 Routing Resources

PLB consists of 4 slices
over 2,400 PIPs mostly MUX PIPs

x6 wire segments
x2 wire segments
xH & xL wire segments

over 450 total wire segments in PLB
Lab 0 – in Spartan 6
(routing details)
Ex: modulo7 counter (device xc6slx25t)
Recent Trends

- Incorporate specialized cores
  - RAMs – single-port, dual-port, FIFOs
    - 128 bits to 36K bits per RAM
    - 4 to 575 RAM cores per FPGA
  - DSPs – 18x18-bit multiplier, 48-bit accumulator, etc.
    - up to 512 per FPGA
  - Microprocessors and/or microcontrollers
    - up to 2 per FPGA
      - Hard core processor
    - Support soft core processors
      - Synthesized from HDL into programmable resources
Spartan 3 (XC3S200)

- 24 rows
- x 20 columns
- = 480 PLBs
- 4 slices/PLB
- 2 LUTs&FFs/slice

- 12 18K-bit dual port RAMs
- 12 18x18-bit multipliers
## Ranges of Resources

<table>
<thead>
<tr>
<th>FPGA Resource</th>
<th>Small FPGA</th>
<th>Large FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLBs per FPGA</td>
<td>256</td>
<td>25,920</td>
</tr>
<tr>
<td>LUTs and flip-flops per PLB</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td><strong>Routing</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wire segments per PLB</td>
<td>45</td>
<td>406</td>
</tr>
<tr>
<td>PIPs per PLB</td>
<td>139</td>
<td>3,462</td>
</tr>
<tr>
<td><strong>Specialized Cores</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits per memory core</td>
<td>128</td>
<td>36,864</td>
</tr>
<tr>
<td>Memory cores per FPGA</td>
<td>16</td>
<td>576</td>
</tr>
<tr>
<td>DSP cores</td>
<td>0</td>
<td>512</td>
</tr>
<tr>
<td><strong>Other</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input/output cells</td>
<td>62</td>
<td>1,200</td>
</tr>
<tr>
<td>Configuration memory bits</td>
<td>42,104</td>
<td>79,704,832</td>
</tr>
</tbody>
</table>
Configuration Interfaces

- **Master** – FPGA retrieves its own configuration from ROM after power-up
  - Serial or Parallel options
- **Slave** – FPGA configured by external source (i.e., a µP)
  - Serial or Parallel options
  - Used for dynamic reconfiguration
  - Can also read configuration memory contents
- **Boundary Scan Interface**
  - 4-wire IEEE standard serial interface for testing
  - Write and read access to configuration memory
    - Not available in all FPGAs
    - Used for dynamic partial reconfiguration
  - Interfaces to FPGA core
    - Not available in all FPGAs
    - Connections between Boundary Scan Interface and internal routing network and PLBs (Xilinx provides 2 of these ports)
- **Other configuration interfaces in some FPGAs**
Daisy Chain Configuration