Chapter 8
Packaging and Yield

- Electrical and electronic devices forming the ICs are fabricated through a multiple-step sequence of photolithographic and chemical processing steps on a wafer.
- Along the way, several other processes need to be completed to have individual ICs to be used in Electrical and electronic devices:
  - Wafer testing / Device testing
  - Die preparation / separation
  - Die attachment / wire bonding
  - Packaging and Yield (good bad die and IC)

Wafer

- Each wafer contains 100s to 1000s of dice
- Each lot contains 10s to 100s of wafers
- Cost to Process a Wafer is Relatively Fixed for a Given Process
- Larger Wafer $\rightarrow$ Lower Cost/Die
- Larger number of wafer $\rightarrow$ Lower Cost/Die
IC Testing
Example

- Each wafer / IC needs to be tested for proper operation
- Examples: SoC (system on Chip), TSV (testing through vias), VLSI (very large scale in IC), etc.
- Built-in-Self-testing: used to make faster, less-expensive integrated circuit manufacturing tests (verifies all or a portion of the internal functionality of the IC).

IC Testing
Example: IC Pick-and-Handler System
Testing at Wafer Level

- After metallization and passivation-layer processes, each die is separated and tested individually for functionality
- The pad is in contact with a probe / computer system – dc tests for basic process parameters
- Defected dice are marked for removal and discarding
- Yield: functional dice / total dice

<table>
<thead>
<tr>
<th>Wafer ID</th>
<th>Yield</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer 1</td>
<td>80%</td>
<td>90%</td>
</tr>
<tr>
<td>Wafer 2</td>
<td>70%</td>
<td>60%</td>
</tr>
<tr>
<td>Wafer 3</td>
<td>80%</td>
<td>70%</td>
</tr>
<tr>
<td>Wafer 4</td>
<td>90%</td>
<td>80%</td>
</tr>
<tr>
<td>Wafer 5</td>
<td>60%</td>
<td>80%</td>
</tr>
<tr>
<td>Wafer 6</td>
<td>70%</td>
<td>80%</td>
</tr>
<tr>
<td>Wafer 7</td>
<td>80%</td>
<td>70%</td>
</tr>
<tr>
<td>Wafer 8</td>
<td>90%</td>
<td>80%</td>
</tr>
<tr>
<td>Wafer 9</td>
<td>75%</td>
<td>70%</td>
</tr>
<tr>
<td>Wafer 10</td>
<td>80%</td>
<td>Average 76.25%</td>
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</tbody>
</table>

Testing and Packaging

- And then, packaged for easy handling and mounting in electronic circuits
- Cost = total yield of assembled and tested devices
- For packaging, many other steps processing steps are performed
- Expected yield ~60 to 80% for mature fabrication facility
Die Separation

- 0.350 to 1.250 mm thick wafers
- For some applications, thinner or thicker wafer is needed
- Mounted on screen ready for dicing saw (diamond saw)
- Then separated
- Good dice will then be packaged

Die Attachment

- Once the wafer is separated into individual dice, further inspection is needed to eliminate broken dice during separation (discard the marked – un functional dice)
- The next step is to assemble the circuit (attachment of dice)
- There are two commonly known methods.
  - Epoxy Die Attachment
  - Eutectic Die Attachment
Die Attachment (cont.)

- **Epoxy Die Attachment:**
  - Epoxy is an adhesive material that enables the semiconductor packaging process with robust interconnect solutions.
  - However, they are very poor thermal conductors and are electrical insulators.

- **Eutectic Die Attachment:**
  - In power electronics devices, metal bonding is preferred.
  - Metal layer deposition before die separation.
  - Then, by heating to eutectic temperature for bonding, pressure is applied.
  - Gold – silicon eutectic point is 370 °C (3.6% to 96.4%).
  - Or, preform layer between the die and the package then heat.

http://iopscience.iop.org/0960-1317/23/1/015017/article

**Figure 2.** Conceptual views of and heat dissipation paths in

(a) typical (single-sided) power module with a single heat dissipation path and
(b) advanced power module integrated with double-sided cooling structure.
Table 1. Comparison of available bonding techniques for power modules

<table>
<thead>
<tr>
<th></th>
<th>Conventional solder</th>
<th>HT Solder</th>
<th>(Nano) silver sintering</th>
<th>TLP bonding</th>
</tr>
</thead>
<tbody>
<tr>
<td>High temp. sustainability</td>
<td>Generally &lt; 250°C</td>
<td>Generally &gt;250°C</td>
<td>Up to ~900°C (performance varies)</td>
<td>~400-900°C (depending on material)</td>
</tr>
<tr>
<td>Repeatability</td>
<td>X</td>
<td>X</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>Process temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Process temperature</td>
<td>&lt; 250°C</td>
<td>&gt;250°C</td>
<td>250-280°C</td>
<td></td>
</tr>
<tr>
<td>Process Pressure</td>
<td></td>
<td></td>
<td>&lt;5 MPa</td>
<td>100-300 kPa</td>
</tr>
<tr>
<td>Material cost</td>
<td></td>
<td></td>
<td>Relatively high cost</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Low material cost</td>
<td>Relatively low material cost (except AuSn, AuSn, AgIn)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compatibility</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Conventional method</td>
<td>Compatible with conventional method</td>
<td>Not conventional material</td>
<td>General materials widely used in conventional power modules</td>
</tr>
</tbody>
</table>

©: Best, O: Good, Δ: Moderate, X: Bad
Wire Bonding

- In the packaging stage, the bond wires are attached to the die and connected to the external electrical contacts.
- Can also be used to connect an IC to other electronics or to connect from one PCB to another.
- Generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages.
- Aluminum, Copper, and Gold are most used metals
- Wire diameters start at 15 μm and can be up to several 100 μm for high-powered applications.

Wire Bonding

- There are two common types (geometrically):
  - Peripheral Bonding Pads
  - Area Array Bonding Pads
- Three common processing types:
  - Thermocompression bonding
  - Ultrasonic bonding
  - Thermosonic bonding

Pads range from 125 μm x 125 μm down to 25 μm x 25 μm
### Wire Bonding – others

<table>
<thead>
<tr>
<th>Horizontal placement</th>
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<tbody>
<tr>
<td></td>
<td>Wire bonding type</td>
<td>Flip chip type</td>
</tr>
<tr>
<td>Stacked structure</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Wire bonding type</td>
<td>Wire bonding + flip chip type</td>
</tr>
<tr>
<td>Interposer type</td>
<td></td>
<td>PoP, e.g. flip chip type</td>
</tr>
<tr>
<td>Interposer - less type</td>
<td>Terminal through via type</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Chip (WLP) embedded + chip on surface type</td>
<td>3D chip embedded type</td>
</tr>
</tbody>
</table>

**Embedded structure**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>WLP embedded + chip on surface type</td>
<td></td>
</tr>
</tbody>
</table>

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### Wire Bonding – Architectures

![Wire Bonding Architectures](image.png)
http://www.google.com/patents/US8322028
Publication number: US8322028 B2
Title: Method of producing an isolator for a microelectromechanical system (MEMS) die

Figure 1. Schematic illustrations of different bonding processes.
Thermocompression Bonding

- "Nail-head" or "ball bonding"
- Pressure and temperature to "weld" gold wire to aluminum bonding pads
  - Substrate is at ~ 150 to 200 °C, bonding interface is at ~ 280 to 350 °C
  - Problem with formation of Au₂₆Al (tan-color) -- low conductivity compound
  - Problem with epoxy -- cannot withstand these "high" temperatures

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**Figure 8.3 - Courtesy of Kulicke and Soffa Industries, Inc. (K&S).**
(a) An SEM of gold ball bonding
(b) SEM of high density gold ball bonding
(c) SEM of bonded die.
Themosonic Ball-Wedge Bonding

FIGURE 8.3
Themosonic ball-wedge bonding of a gold wire.
(a) Gold wire in a capillary;
(b) ball formation accomplished by passing a hydrogen torch over the end of a gold wire or by capacitance discharge;
(c) bonding accomplished by simultaneously applying a vertical load on the ball while ultrasonically exciting the wire (the chip and substrate are heated to about 150 °C);


Themosonic Ball-Wedge Bonding (cont.)

FIGURE 8.3
(d) a wire loop and a wedge bond ready to be formed;
(e) the wire is broken at the wedge bond;
(f) the geometry of the ball-wedge bond that allows high speed bonding.
Because the wedge can be on an arc from the ball, the bond head or package table does not have to rotate to form the wedge bond.

Ultrasonic Bonding

To avoid oxidation at high temperature
Combination of pressure and rapid mechanical vibration (20 to 60 kHz)

FIGURE 8.5
(a) In ultrasonic bonding, the tool guides wire to the package terminal;
(b) pressure and ultrasonic energy form the bond;
(c) and (d) the tool feeds out wire and repositions itself above the IC chip.
The tool lowers and ultrasonically forms the second bond;
(e) tool lifts, breaking the wire at the bond. Reprinted with permission from Circuits

More Wire Bonding

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Packaging

- Packaging is used for both protecting the chip surface from environmental factors and making electrical connections big enough for soldering.
  - Electrical connection
  - Environmental protection
- Microchip is “glued” inside a package, electrical connections are made to package pads, and then chip is covered with a cap or a plastic mold

Packages
Packages

- Common types listed in your text book:
  - Round TO-Style
  - Dual-In-Line (DIP)
  - Pin-Grid-Array (PGA)
  - Leadless-Chip-Carrier (LCC)
  - Packages for surface mounting

- From 4 to 48 pin configuration
- Kovar (iron-nickel) leads
- Glass seal
- Metal cap after die attachment / wire bonding

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Packages

**Ball-and wedge-bonded Si die in a plastic Dual-In-Line Packages (DIPs)**

Easy and inexpensive 4 to 80 pin

(b) Ball- and wedge-bonded silicon die in a plastic DIP. The die support paddle may be connected to one of the external leads. For most commercial products, only the die paddle and the wedge-bond pads are selectively plated. The external leads are solder-plated or dipped after package molding.
**Pin Grid Array (PGAs)**

- Pin Grid Array (PGA) Package with Upward Facing Cavity
- PGAs also come with the Cavity Facing Downward

**Leadless Chip Carriers**

Figure 8.8
(a) Ceramic leadless chip carriers with top connections. (b) LCC with edge connections in grooves on the side of the package.

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**Packages for Surface Mounting**

- Dual in-line package (DIP)
- Single in-line package (SIP)
- Zip-ty in-line package (ZIP)
- Through hole (DIPs)

Permits soldering of the Packages directly to the Printed circuit board

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Flip-Chip Technology

• Die-mounting and wire bonding processes involve large number of manual operation
• One-at-a-time wire bonding reduces reliability – in fact it is the most common reliability problem
• Flip-chip and tape-automated-bonding permit batch fabrication of die-to-package interconnections

Solder dots are deposited on each of the pads
Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry
Solder balls are then remelted
Mounted chip is "underfilled" using an electrically-insulating adhesive

Flip-Chip Technology (cont.)
Flip-Chip Technology (cont.)

Fig. 8.a Solder Ball Formation

- Layers of chrome, copper, lead and tin are sequentially deposited
- After heating for reflow, the 5% tin - 95% lead solder ball forms
- Dice are placed face down on substrate – die is bonded directly to substrate

Flip-Chip Technology (cont.)

Figure 8.10 (b)
Flip-chip Pb/Sn (Lead/Tin) solder bumps in standard 250 μm pitch (right) and 50 μm. Courtesy of MCNC Optical and Electronic Packaging Group.

Figure 8.11
Gold Bumps formed by modification of the wire-bond process. Courtesy of Kulicke and Soffa Industries, Inc. (K&S).
Ball Grid Array Layout

Fig. 8.2 (a) Either peripheral wire bond with solder balls (b) or large array of solder balls placed over the full die area

Ball Grid Array (BGA) Technology

• A type of surface-mount packaging - It applies the solder ball technique to the package (rather than the chip)
• BGA packages are used to permanently mount devices and can provide more interconnection pins than on a dual in-line or flat package.
• The whole bottom surface of the device can be used (the leads are shorter than with a perimeter-only type) -> better performance at high speeds.
Ball Grid Array (BGA)

Figure 8.12
(a) Ball grid array cross section
(b) Intel microprocessor using a BGA. Courtesy of Intel Corp.

Tape Automated Bonding

- Dice are attached to copper leads supported by a tape (film)
- Film is coated with copper; and the leads are defined by lithography and etching
- Die attachment requires process similar to the solder-ball technology
FIGURE 8.13
Process sequence for making gold bumps on aluminum metallurgy devices.
(a) The wafer is cleaned and sputter-etched:
(b) a contact/barrier layer (which also serves as a conductive film for electroplating) is sputter-deposited with a layer of gold for oxidation protection;
(c) a thick-film photoresist (25 μm) is laminated and developed;

(d) gold is electroplated to a height of approximately 25 μm to form the bumps;
(e) the resist is stripped;
(f) the sputter-deposited conductive film is removed chemically or by back sputtering.

Tape Automated Bonding (cont.)

FIGURE 8.14
Tape-automated-bonding procedure. (a) Preformed leads of film are lowered into position and aligned above bonding pads on the die, which is held in place with a wax; (b) bonding tool descends and forms bond with pressure and heat; heat melts the wax, releasing the die; (c) tool and film are raised, lifting the bonded die clear so a new die can be moved into position and the process can be repeated. Reprinted with permission from Small Precision Tools Bonding Handbook. Copyright 1976.

Chip Scale Packages (CSP)

Packages whose are is not much larger than the chip

Figure 8.15
(a) Chip scale package using wire bonding (wire bonded die)
(b) Alternate form of CSP (employs a form of TAB
(c) Chip-on-board packaging (by mounting bare die directly on the printed circuit board or flexible substrate)
Yield

- Number of available chips for sale – number of good chips to over all chips
- Losses
  - die loses at the wafer level after fabrication
  - during die preparation and packaging operation
  - number of packaged devices will fail at final testing

Yield (cont.)

Wafer yield is related to complexity of the processes and depends on the area of the wafer

Figure 8.16: Illustration of wafers showing effect of die size on yield. Dots indicate the presence of a defective die location. (Die are inked at test.)
(a) For a particular die size, yield is 43%.
(b) If the die size were doubled, the yield would be only 22%
Probability of Defects

- Probability of defects is given by binomial distribution

\[ P_k = \frac{n!}{k!(n-k)!} N^{-n} (N-1)^{n-k} \]

- For large \( n \) and \( N \), the binomial distribution approximates to the Poisson Distribution

\[ P_k = \frac{\lambda^k}{k!} \exp(-\lambda) \]

Where \( \lambda = n / N \)

1. Uniform Defect Densities

If we assume the defect density is uniform, then, the yield is given by the probability that a die is found with no defects:

\[ Y = P_o = \exp(-\lambda) \]

We know that the area of the wafer is \( N \times A \), \( (A \) is the area of a die, \( N \) is the number of dies on a wafer)

Average number of defects is:

\[ \lambda = n / N = D_o A \]

Then, yield is:

\[ Y = \exp(-D_o A) \]

May not be good enough because:
- Low estimates for large size dice with \((D_oA)>1\)
- More defects around edges than the center
- Defects tend to be found in clusters
Examples of Defects on Wafer

Mathematical Functions Defining Yield

Figure 8.17
(a) Impulse where every wafer has exactly the same number of defects
(b) A triangular approximation to a Gaussian density
(c) A uniform density function
Yield Modeling: Theory

Yield: \[ Y = \int_{0}^{\infty} \exp(-DA)f(D)dD \]

Impulse Distribution \( f(D) = \delta(D_0) \): \( Y = \exp(-D_0A) \)

\( D_0 = 4 \text{ cm}^2 \quad A = 1 \text{ cm}^2 \quad Y = 1.8\% \)

Mature Process \( Y > 70\% \)

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Uniform and Non-uniform Defect Densities

Yield: \[ Y = \int_{0}^{D} \exp(-DA)f(D)dD \] Binomial definition

Impulse Distribution \( f(D) = \delta(D_0) \): \( Y = \exp(-D_0A) \)

Triangular Distribution:
\[ Y = \left[ 1 - \frac{\exp(-D_0A)}{D_0A} \right]^2 \]

Uniform Distribution:
\[ Y = \frac{1 - \exp(-2D_0A)}{2D_0A} \]
Uniform and Non-uniform Defect Densities

Yield: \[ Y = \int_0^\infty \exp(-DA)f(D)dD \]

Binomial/Gamma Distributions: \[ Y = \left[ 1 + \frac{D_0A}{\alpha} \right]^{-\alpha} \]

\( \alpha = \) clustering parameter (0.5 - 10)

- ITRS 2010 (\( \alpha = 5 \))
  - \( D_0 \leq 0.1/cm^2 \)
  - Critical Defect Size < 30 nm

Yield Modeling: Yield Curves

Theoretical yield curves versus defect density - area product

Yield drops off rapidly as die area increases, but not as rapidly as Poisson distribution predicts

Early predictions were based upon \( Y = \exp(D_0A) \). Fortunately, this result was far too pessimistic.