

# A Comparison of SEU Tolerance in High-Speed SiGe HBT Digital Logic Designed With Multiple Circuit Architectures

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**Abstract**—The single-event upset (SEU) responses of three D flip-flop circuits, including two unhardened, and one current-sharing hardened (CSH) circuit, are examined using device and circuit simulation. The circuit that implements the conventional D flip-flop logic using standard bipolar NAND gates shows much better SEU performance than the other two. Cross coupling at transistor level in the storage cell of the other two circuits increases their vulnerability to SEU. The observed differences are explained by analyzing the differential output of the emitter coupled pair being hit. These results suggest a potential path for achieving sufficient SEU tolerance in high-speed SiGe heterojunction bipolar transistor (HBT) digital logic for many space applications.

**Index Terms**—Charge collection, circuit modeling, current-mode logic, heterojunction bipolar transistor (HBT), SiGe, single event effects.

## I. INTRODUCTION

SiGe heterojunction bipolar transistor (HBT) technology, because it has higher intrinsic performance than Si technology at similar process complexity, and delivers better cost performance than GaAs technology, has recently emerged as a contender for high-speed digital, radio-frequency, and microwave applications. The technology has proven hard to various types of ionizing radiation and is attractive for space applications. High-speed SiGe HBT logic circuits, however, were recently found to be vulnerable to single-event effects through testing and modeling. It is well known that single event effects in bipolar digital logic depend on the details of the circuit implementation, and circuit configuration can be optimized to minimize SEU sensitivity. In this work, we compare the SEU responses of three SiGe HBT D flip-flop circuits, including 1) the current-sharing hard-

ened (CSH) flip-flop circuit used in the shift registers reported in [1]; 2) the unhardened version of the current-sharing hardened (CSH) D flip-flop circuit reported in [1]; and 3) a straightforward bipolar NAND gate implementation of the standard D flip-flop logic, which we have designed recently. The circuit SEU responses are simulated by including SEE-induced transient terminal currents obtained from device simulation in circuit simulation [2], [3]. MEDICI from Avant!, Fremont, CA, [4] and Spectre from Cadence are used for device simulation and circuit simulation, respectively. All of the circuits are designed using the SiGe HBT design kit from IBM, which describes SiGe HBTs using the Vertical Bipolar Inter Company (VBIC) transistor model. Our results will provide guidelines on the selection of transistor level circuit implementation of high-speed SiGe HBT digital logic for space applications.

## II. DEVICE TECHNOLOGY

The SiGe HBTs used were fabricated by IBM, and are typical of first-generation SiGe technology. A schematic cross-section is shown in Fig. 1. The SiGe HBT has a planar, self-aligned structure with a conventional poly emitter contact, silicided extrinsic base, and deep- and shallow-trench isolation. The SiGe base was grown using UHV/CVD. The details of the fabrication process can be found in [5]. The p-type substrate and the n-p-n layers of the intrinsic transistor form a n-p-n-p multi-layer structure, complicating charge collection like in advanced bipolar process [6]. The p-type substrate is usually biased at the lowest potential ( $-5.2$  V here) for isolation. Key performance metrics of the SiGe HBTs include: 1) 50 GHz cut-off frequency ( $f_T$ ); 2) 70 GHz maximum oscillation frequency ( $f_{max}$ ); 3) less than 0.5 dB minimum noise figure ( $NF_{min}$ ) at 2 GHz; and 4) an excellent power added efficiency of 65% at 900 MHz. Power-added efficiency (PAE) is defined as  $PAE = (P_{RF_{out}} - P_{RF_{in}})/P_{dc}$ , where  $P_{RF_{out}}$  is the RF output power,  $P_{RF_{in}}$  is the RF input power, and  $P_{dc}$  is the average dc power consumption [7]; and 5) an excellent linearity efficiency of 10 at 2 GHz. Linearity efficiency is defined as the ratio of input third order intercept (IIP3) to dc power consumption [8].

## III. DEVICE AND CIRCUIT SIMULATION APPROACH

The SEE-induced transient terminal currents are obtained using quasi-three-dimensional device simulation [2]. The semi-

Manuscript received August 22, 2002; revised October 17, 2002. This work was supported by DTRA under the Radiation Tolerant Microelectronics Program, NASA-Goddard Space Flight Center (GSFC), Greenbelt, MD, under the Electronics Radiation Characterization (ERC) Program, and the Auburn University CSPAE, Auburn, AL.

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Digital Object Identifier 10.1109/TNS.2002.805390

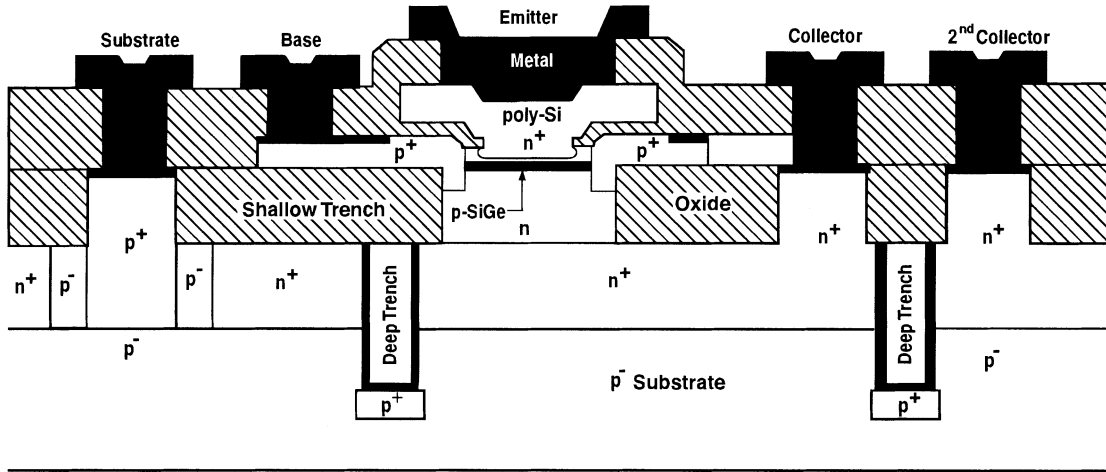


Fig. 1. Schematic cross section of the SiGe HBT used in simulation.

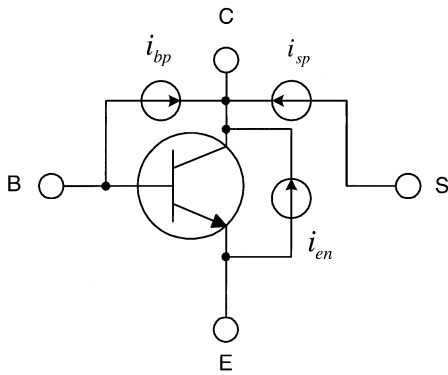


Fig. 2. Equivalent circuit model for including the SEE-induced terminal currents in circuit simulation.

conductor equations were solved using cylindrical coordinates, and the center of the emitter was chosen as  $r = 0$ . The SiGe HBT doping profile and Ge profile were constructed using measured SIMS data and calibration of dc and ac electrical characteristics against measured data. A set of advanced physical models, as opposed to the default simplest models, was selected, and the coefficients were tuned to match the measured dc and ac electrical characteristics. A top substrate contact as shown in Fig. 1 was used in the simulation to better mimic reality. A simulation depth of  $50 \mu\text{m}$  was used and verified to satisfy the boundary conditions at the bottom of the simulated structure. Gridding validity was checked by repeating the simulation on finer grids. The charge track was generated over a period of 10 ps using a Gaussian waveform. The Gaussian has a  $1/e$  characteristic time scale of 2 ps, a  $1/e$  characteristic radius of  $0.2 \mu\text{m}$ , and the peak of the Gaussian occurs at 4 ps. The depth of the charge track is assumed to be  $10 \mu\text{m}$  below the emitter metal contact. An LET of  $0.5 \text{ pC}/\mu\text{m}$  is used along the charge track. An LET of  $97 \text{ MeV}\cdot\text{cm}^2/\text{mg}$  corresponds to a charge deposition of  $1 \text{ pC}/\mu\text{m}$  in silicon. Most of the material in a SiGe HBT is silicon, except for the less than 100 nm thin base region which has less than 10% Ge at its peak. The substrate doping is  $5 \times 10^{15}/\text{cm}^3$ .

The SEE-induced transient currents are included in the circuit simulation using the equivalent circuit model shown in Fig. 2. The SEE-induced transient currents at the emitter and collector are denoted as  $i_{en}$  and  $i_{cn}$ , where the subscript  $n$  indicates “electron collection.” Similarly, the ion-induced currents at the base and substrate are denoted as  $i_{bp}$  and  $i_{sp}$ , where  $p$  indicates “hole collection.”  $i_{en}$ ,  $i_{cn}$ ,  $i_{bp}$ , and  $i_{sp}$  can be simulated using a device simulator as a function of time for a given ion strike. The sum of all of the terminal currents is always zero, which is verified by summing the simulated terminal currents. As a result, we only need to describe any three of the four currents, and the other current is automatically accounted for. The equivalent circuit shown in Fig. 2 explicitly describes  $i_{bp}$ ,  $i_{sp}$ , and  $i_{en}$ .

- $i_{bp}$  represents the SEE-induced transient base current.
- $i_{sp}$  represents the SEE-induced transient substrate current.
- $i_{en}$  represents the SEE-induced transient emitter current.

The SEE-induced collector current  $i_{cn}$  is given by

$$i_{cn} = -(i_{bp} + i_{sp} + i_{en}). \quad (1)$$

The whole purpose of the equivalent circuit in Fig. 2 is to faithfully reproduce the SEE-induced transient currents at all of the transistor terminals obtained from device simulation in circuit simulation. Despite the use of current sources connecting various terminals, the equivalent circuit does not assume any physical model for the charge collection process.

In Fig. 2, currents going into the terminals (E,B,C,S) are defined to be positive, a convention used by all of the device simulators. This facilitates the inclusion of device simulation output in circuit simulation as it is without any additional manipulation. The actual values of these currents can be either positive or negative during the SEU process, and can change sign during the process, as we will detail in the following. Waveforms of the simulated transient currents are shown in Fig. 3. Upon the ion strike, positive transient currents are induced at all the terminals. For most of the time, the SEE-induced collector current is positive (going in), while the SEE-induced base and substrate currents are negative (coming out). The SEE-induced emitter current is much smaller compared to the SEE-induced collector current.

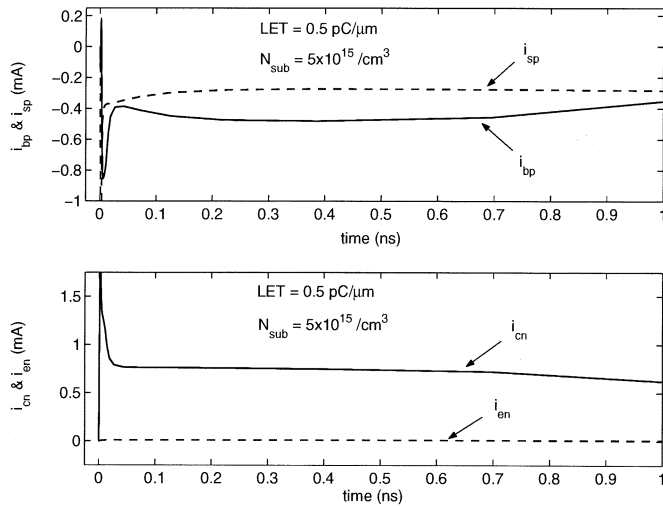


Fig. 3. SEE-induced base, substrate, collector, and emitter currents for  $LET = 0.5 \text{ pC}/\mu\text{m}$ .  $N_{\text{sub}} = 5 \times 10^{15}/\text{cm}^3$ .

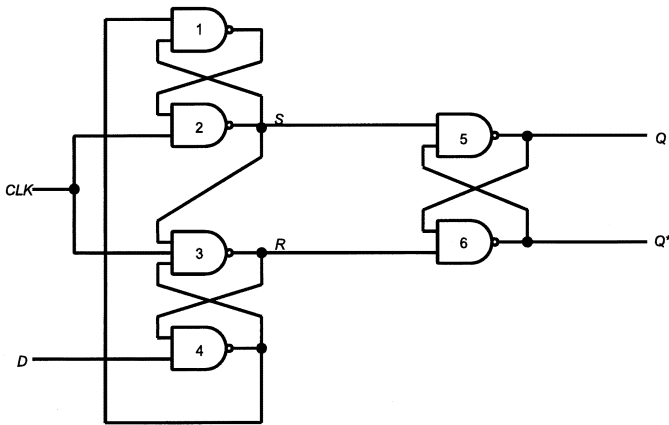


Fig. 4. Logic diagram of a standard rising edge-triggered D flip-flop.

#### IV. CIRCUIT DESCRIPTION

Three D flip-flop circuits are investigated, including two unhardened circuits, denoted as circuit A and B and a current sharing hardened circuit, denoted as circuit C. All of the three circuits have identical logic function of a rising edge-triggered D flip-flop under normal operation (without SEU).

##### A. Circuit A

Circuit A is a straightforward gate-level implementation of the standard rising edge-triggered D flip-flop logic diagram shown in Fig. 4. Each NAND gate in the D flip-flop is implemented using standard differential ECL circuit as shown in Fig. 5. The inputs to the multilevel NAND gate are accordingly level shifted (using level shifters, not shown for brevity) to ensure operation of all transistors in nonsaturating region. IN1 and IN2 are the two inputs, and IN1\* and IN2\* indicate their logic complement. V1 is the NAND gate output, while V2 is the compliment of V1. VCS sets the switching current.

##### B. Circuit B

Circuit B is the unhardened version of the D flip-flop used in the shift registers tested in [1], implemented using current mode

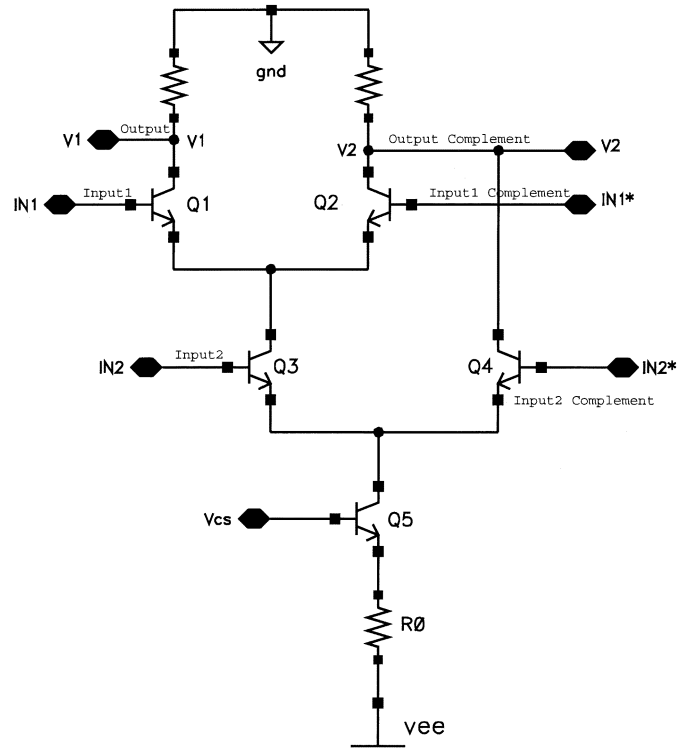


Fig. 5. Standard ECL implementation of two-input NAND gate. Level shifters needed to get to the correct input level for IN2 are not shown.

logic (CML). The transistor level circuit is shown in Fig. 6. Circuit B, unlike circuit A, is not a gate-level implementation of the D flip-flop logic. It uses a lot fewer transistors than circuit A. While circuit A has 56 transistors, circuit B has 14 transistors and consumes much less power. The delay in circuit B is only that needed for switching currents in the differential ECL cells, as opposed to individual gate delays in circuit A and hence is best suited for high-speed logic circuits [9]. The circuit consists of a master stage and a slave stage. The master stage consists of a pass cell (Q1 and Q2), a storage cell (Q3 and Q4), a clocking stage (Q5 and Q6), and a biasing control (Q7). The transistors in the pass and storage cells are stacked over the CLK and control transistors. Hence, the input levels at the clock stage and the control have to be level shifted for the transistors to operate in forward active mode while conducting. The slave stage has a similar circuit configuration. The storage cell of the master stage and the pass cell of the slave stage are controlled by CLK, and the pass cell of the master stage and the storage cell of the slave stage are controlled by CLK\*.

##### C. Circuit C

Circuit C is the current sharing hardened version of circuit B. The circuit was used as a basic building block of the 32 stage shift-register tested in [1]. Each transistor element in Fig. 6 is now implemented with a multipath ( $5 \times$ ) CSH architecture with 70 transistors in all. The CSH concept is illustrated in Fig. 7 using a single level basic current-mode logic gate [10]. The current source transistor Q7 is divided into five paths, with  $V_{cs1}$  controlling three paths and  $V_{cs2}$  and  $V_{cs3}$  controlling one path each. These paths are maintained separately through the clocking stage and through the pass and storage cells. In essence, the input and output nodes of five copies of the switching circuits, including

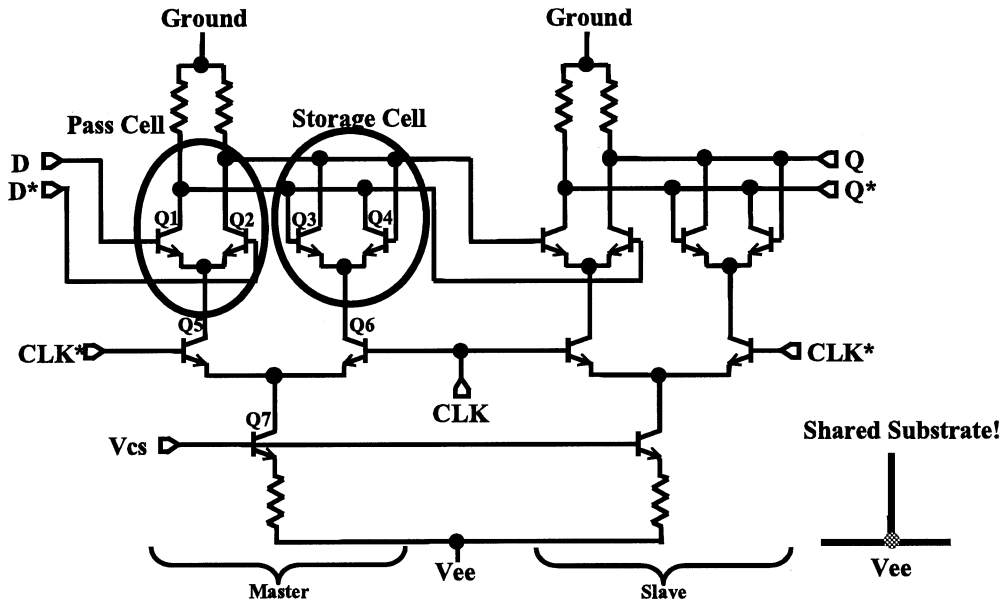


Fig. 6. Schematic of circuit B—the unhardened counterpart of the D flip-flop used in the shift registers tested in [1].

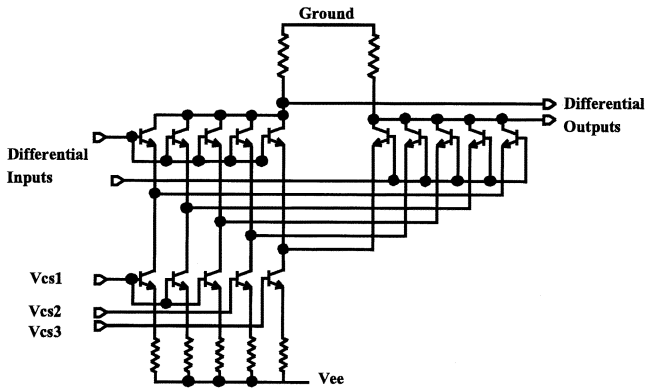


Fig. 7. Illustration of current-sharing hardening (CSH) concept using a basic ECL gate. Five parallel transistors are used to maintain separate current paths.

the controlling switch, clock, master and storage cells, are connected in parallel. The load resistance is shared by all the current paths. The full schematic is not shown because of the large number of transistors and interconnects.

## V. RESULTS AND DISCUSSION

### A. Performance Comparison

We first compare the three circuits for a fixed switching current of 1.5 mA. The input data was chosen to be alternating series of “0” and “1” at a data rate of 2 Gb/s. For each circuit under investigation, sensitive transistors were first identified by applying the SEE-induced transient currents to each transistor during circuit simulation.

In circuit A, we found that NAND gate 2 in Fig. 4, which is in the “storage cell” of the flip-flop could be vulnerable to ion-strike. In particular, transistor Q1, which is at the output node of NAND gate (in this case gate 2), was “struck” (Fig. 5). Under normal operation, when input D and clock are both low, the two inputs to NAND gate 1 are high, reinforcing the output of NAND gate 2 to “1.” If we cause an upset in NAND gate

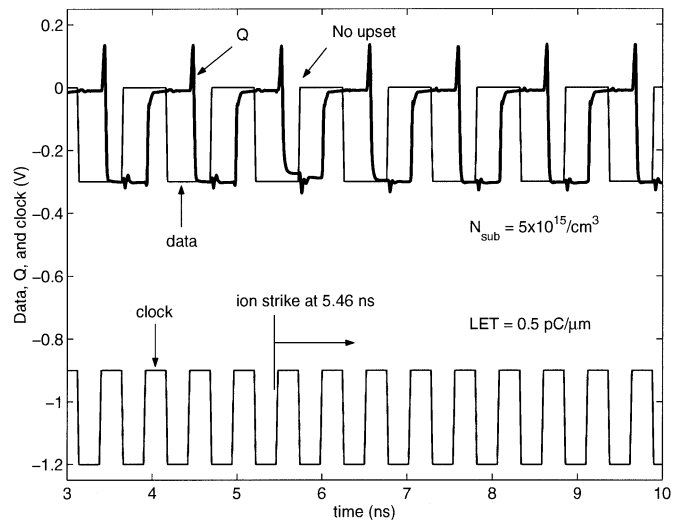


Fig. 8. Output waveform for circuit A.  $LET = 0.5 \text{ pC}/\mu\text{m}$ . Switching current is 1.5 mA.

2 by, for example, driving the input of NAND gate 2 (connected to the output of NAND gate 1) high, and when the clock changes from “0” to “1,” we generate a “0” at the output of NAND gate 2, which in normal operation would have stayed high. This leads to observable upset in the output of the flip-flop. The afore mentioned transitions of input levels and clock occur at 5.46 ns after the start of simulation. In circuits B and C, Q3 of the storage cell in the master stage was found to be the most sensitive (Figs. 6 and 7). The upset due to SEE-induced transient currents in storage cell quite certainly propagates to the output producing observable changes at the output.

Figs. 8–10 show the simulated SEU responses for circuit A, B, and C, respectively. An LET of  $0.5 \text{ pC}/\mu\text{m}$ , and a substrate doping  $N_{\text{sub}} = 5 \times 10^{15}/\text{cm}^3$  are used. The SEU currents are activated at 5.46 ns, within the circuit hold time, right after the clock goes from low to high, a sensitive time instant for SEE-induced transient currents to produce an upset at the output. The

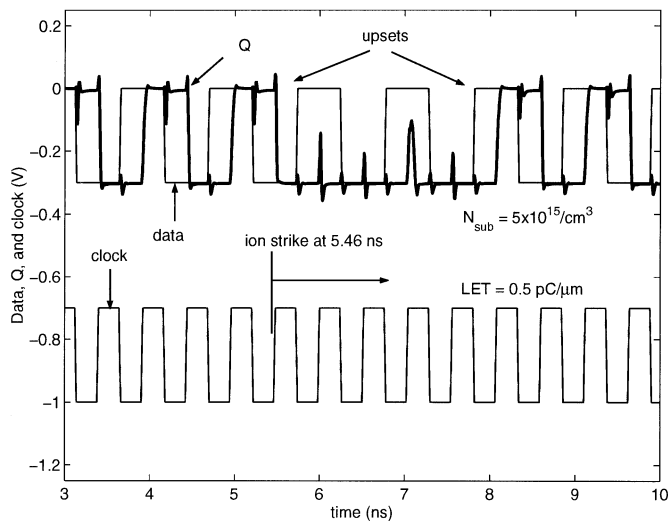


Fig. 9. Output waveform for circuit B. LET = 0.5 pC/μm. Switching current is 1.5 mA.

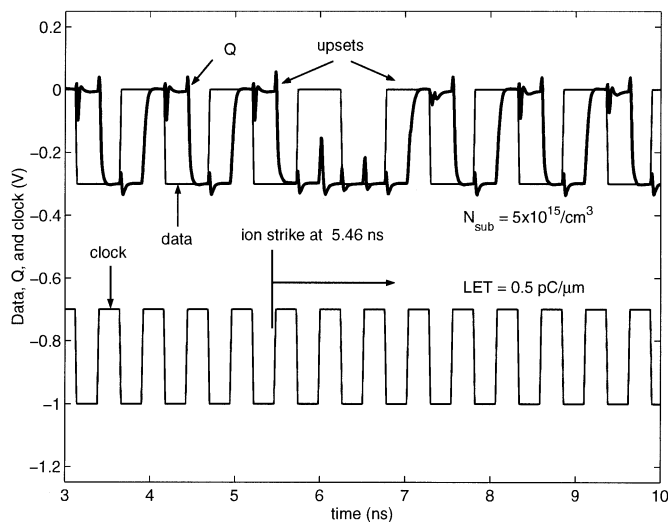


Fig. 10. Output waveform for circuit C (CSH hardened version of circuit B). LET = 0.5 pC/μm. Switching current is 1.5 mA.

dependence of worst-case SEU response on time instant was demonstrated by simulations at 5 ns in circuit B (again, right after clock transition from low to high). A “strike” at this instant did not yield as many upsets as the “strike” at 5.46 ns.

An examination of the results shows that circuit A shows no upset at all, while circuits B and C show 5 and 3 continuous bits of upset, respectively. These results indicate that circuit A shows the best SEU performance. Circuit C, the CSH hardened version, shows better SEU performance than its unhardened version, circuit B. Although circuit A is in principle slower than circuit B and C when the circuits are operated at frequencies close to the cutoff frequency of the transistors, all of the three circuits simulated show similar performance for the 2 Gb/s data rate used in our applications. The high speed of the SiGe HBTs used (50 GHz peak  $f_T$  and 70 GHz peak  $f_{max}$ ) yields sufficiently small gate delay even for circuits operating with data rates much higher than 2 Gbits/s.

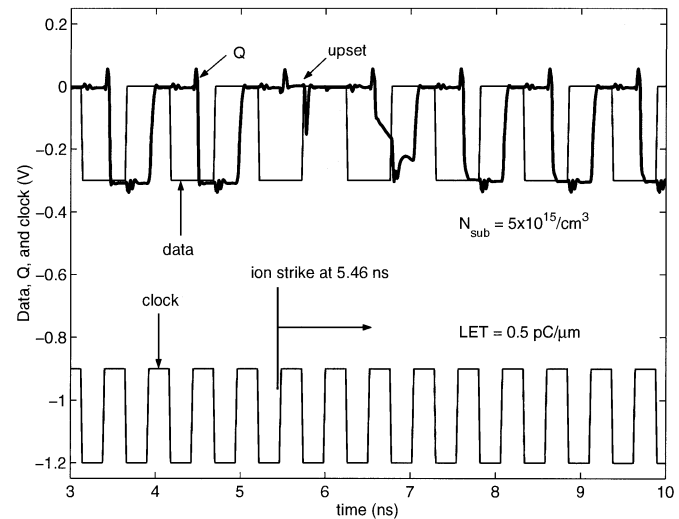


Fig. 11. Output waveform for circuit A at a switching current of 0.6 mA.

Circuit A, which shows no upset at a switching current of 1.5 mA, shows upset when the switching current is lowered to 0.6 mA (Fig. 11). The load resistance is increased to maintain the voltage swing needed for correct differential switching. Since the amount of SEE-induced change in differential output voltage ( $V1-V2$ ) is fundamentally determined by the product of the transient collector current and the load resistance, the increased load resistance leads to a larger differential voltage upset. This, combined with the reduced input differential voltage threshold for a smaller switching current, leads to more upsets for a lower switching current. This is consistent with our earlier observation that increasing switching current is effective in improving SEU performance for circuit C [2]. Similarly, the SEU tolerance can be improved by decreasing the load resistance, which necessarily requires an increase of the switching current to produce adequate voltage swing for proper switching, and thus a higher power consumption.

### B. Understanding the Results

The fundamental reason for the better SEU performance of circuit A than circuits B and C, we believe, is that only one of the two outputs of the emitter coupled pair being hit is affected by SEE transients. This naturally provides certain amount of redundancy at the transistor level in circuit A. As long as the differential output remains above or below its corresponding threshold, the output of the entire circuit remains correct. Such redundancy, however, is destroyed in circuits B and C, because of transistor level cross coupling of the differential input and output, as can be seen from Fig. 6. Detailed explanations are given as follows.

Consider striking NAND gate 2 in circuit A. Under normal operation, IN1 and IN2 (Fig. 5) are both low when CLK is low. Q1 and Q3 are OFF, Q4 is ON, and Q2 is OFF. Current flowing through Q4 pulls V2 low and as no current flows in the other branch, V1 is high. At the very instant clock goes high, the SEE-induced transient currents are activated on Q1 (being hit). The SEE-induced transient collector current drives the node voltage V1 low, which under normal operation, would

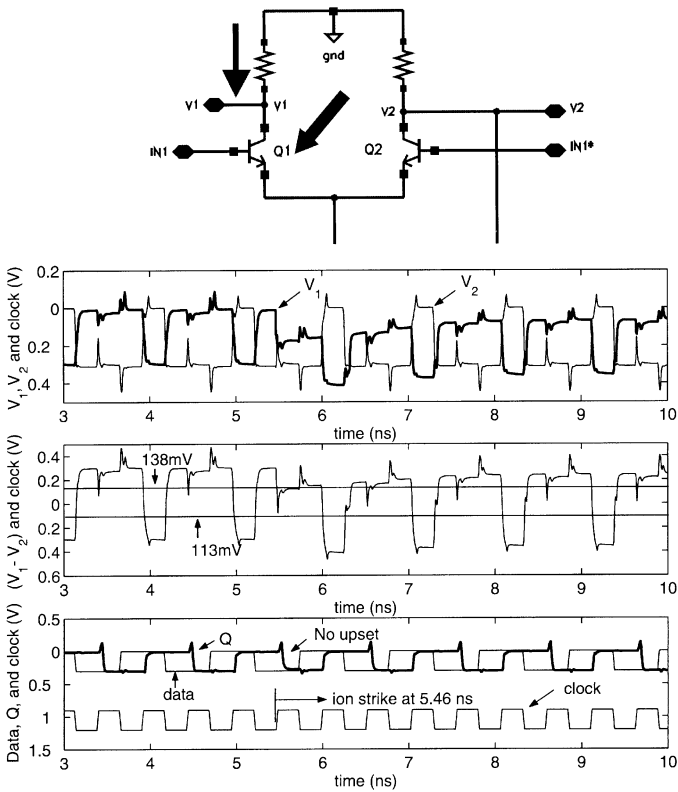


Fig. 12. Output voltages and differential output for the emitter coupled pair struck by heavy ion in circuit A. Switching current is 1.5 mA. In the circuit diagram shown here, the inclined arrow points to the transistor being hit (Q1) and the downward arrow shows the flow of the resultant transient current (through the collector of Q1).

have stayed high. In the absence of change in external data levels, IN1\* stays high, IN2\* is driven low when clock goes high, and the switching currents continue to flow through Q2, maintaining V2 low. As a result, the ion strike of Q1 changes only V1, the output of the transistor being struck, but does not affect the node voltage V2, the complement output. What matters for the next stage, NAND gate 5, however, is the differential output V1-V2, as can be seen from Fig. 4. As long as the differential output (V1-V2) remains above or below the corresponding high-to-low or low-to-high transition threshold, no upset is observed at the next stage. Fig. 12 shows the simulated (V1-V2), along with the thresholds for low-to-high and high-to-low transitions. Even though the collector voltage of NAND gate 2 (V1) goes low upon ion strike, no upset is observed at the output, because the differential output remains above its threshold. In other words, the complement output that comes naturally with a differential logic helps SEE immunity, because the complement output is not affected by SEE, thus providing certain amount of redundancy.

This redundancy, however, is destroyed in circuits B and C, because of transistor level cross coupling of the differential inputs and the differential outputs. Observe that in Fig. 6, transistors Q3 and Q4 are cross coupled at the transistor level. The base (input) and collector (output) of transistor Q3 are connected to the collector and base of Q4, respectively. This cross coupling of Q3 and Q4 gives rise to a positive feedback between the two transistors, which is necessary for proper circuit function. How-

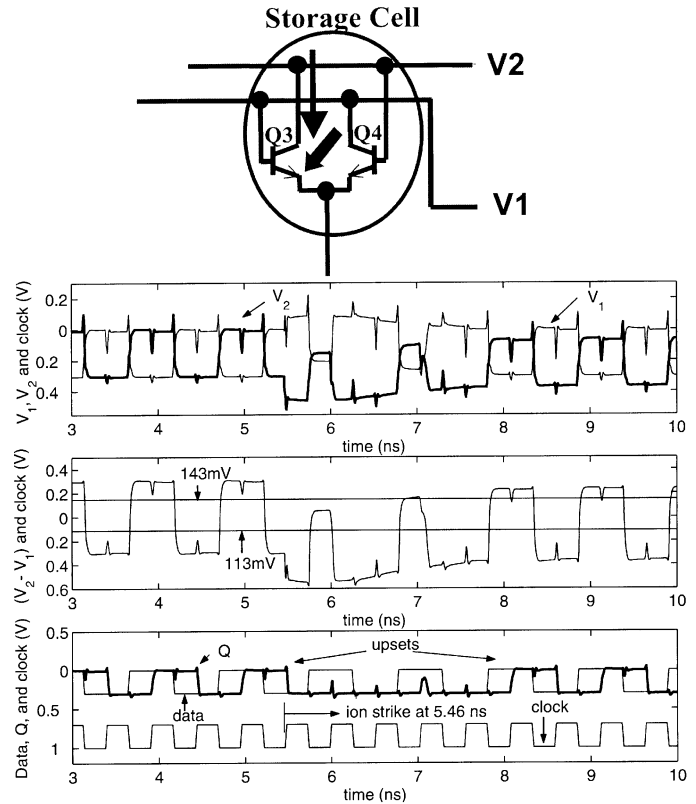


Fig. 13. Output voltages and differential output for the emitter coupled pair struck by heavy ion in circuit B. Switching current is 1.5 mA. Time instant of "strike" is 5.46 ns. In the circuit diagram shown here, the inclined arrow points to the transistor being hit (Q3) and the downward arrow shows the flow of the resultant transient current (through the collector of Q3). Cross-coupling at transistor level enhances the upset in the differential output.

ever, the upset of one output due to ion strike of one of the two transistors necessarily causes an upset of the complement output as well in the event of SEE, because of cross coupling. The upset of the differential output, which is what matters for the next stage, is much more severe.

Let V1 and V2 represent the collector voltages of Q4 and Q3, as shown in Fig. 13. Consider striking Q3, a transient collector current is produced in Q3, which pulls down V2. The decrease of V2 (base of Q4) reduces the collector current of Q4, causing an increase of V1, which in turn causes further decrease of V2. The positive feedback not only enhances the SEE-induced drop of V2 (compared to without SEE), but also also makes V1 go higher than without SEE. Both outputs of the storage cell are disturbed to equal extent even if only one of the two transistors of the differential pair receives an ion-strike. Since the differential output of this stage is applied to the differential input of the next stage, the upsets propagate to the output. This analysis is supported by the simulated V1, V2, and (V2-V1) shown in Fig. 13 for the storage cell. The SEE-induced upset of the differential output and hence, the output of the overall circuit is much worse than in circuit A.

In order to demonstrate the importance of instance of "strike" for capturing the worst-case scenario, SEE-induced transient currents were triggered at 5 ns in circuit B, when the differential input (V2-V1) to the slave stage was high. The results are shown in Fig. 14. Interestingly, the overall number of upsets is less than

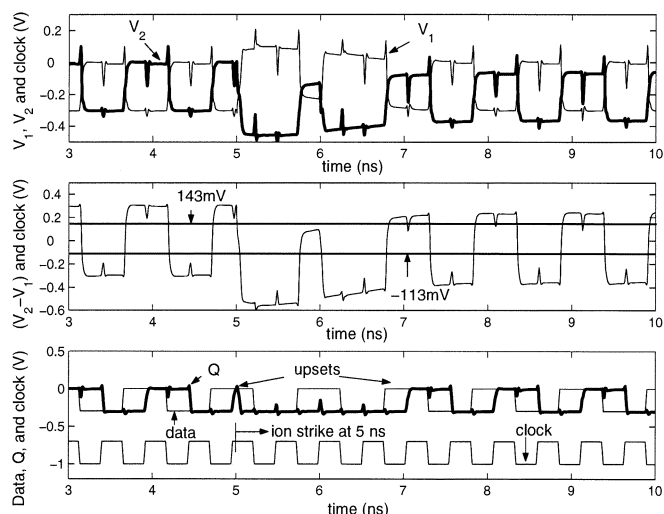


Fig. 14. Output voltages and differential output for the emitter coupled pair struck by heavy ion in circuit B. Switching current is 1.5 mA. Time instant of “strike” is 5 ns.

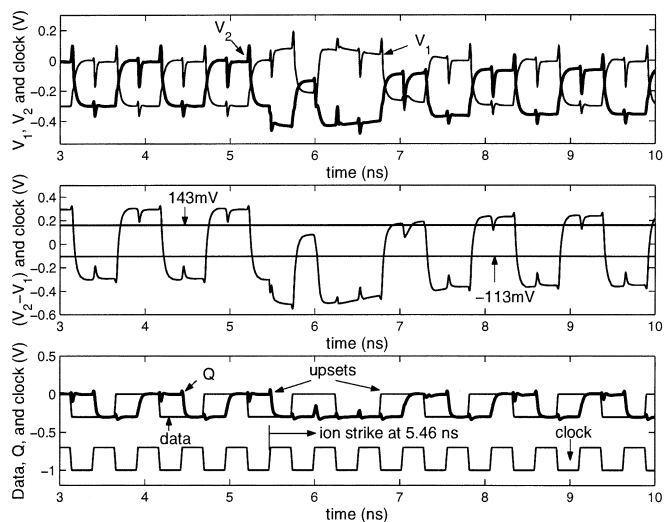


Fig. 15. Output voltages and differential output for the emitter coupled pair struck by heavy ion in circuit C. Switching current is 1.5 mA. Time instant of “strike” is 5.46 ns.

that for activating the SEU transients at 5.46 ns, despite immediately causing upset at the output. At 5.46 ns, the differential input was already low, and the triggering of SEU transients further lowered this voltage, as shown by (V2-V1) waveform in Fig. 13, thus ensuring correct logic at the output. However, the recovery of the whole circuit takes longer time than when the SEU transients are activated at 5 ns. These results indicate that the total number of upsets produced by one strike critically depends on the time instant of the “strike,” and a time instant that produces an immediate upset at the circuit output is not necessarily the worst case.

The reason for the better SEU performance of circuit C over circuit B is the lower recovery time for the differential output

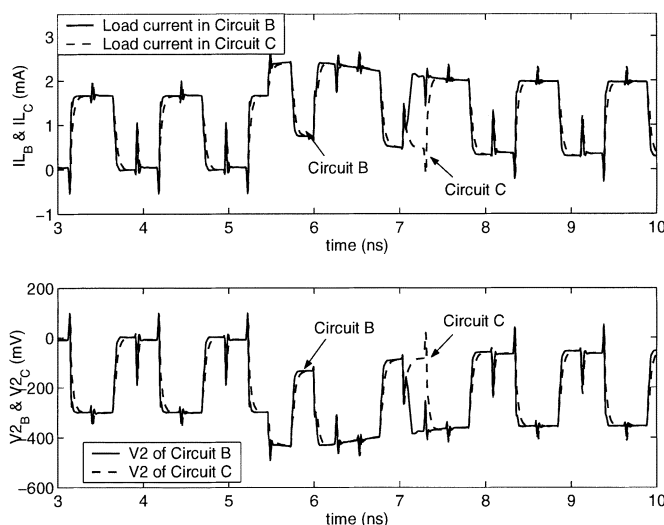


Fig. 16. Overlap of load voltages (V2) and load currents for circuit B and C, flowing through the load resistor connected to the collector of the transistor being “hit.”

(V2-V1) in circuit C (Fig. 15). Fig. 16 compares the simulated (V2-V1) waveforms as well as the load currents through the load resistance for circuits B and C. While (V2-V1) waveform for circuit B has still not recovered at 7 ns, the (V2-V1) waveform for circuit C has recovered by that time instant. The faster recovery of circuit C is likely due to the higher parasitic loading capacitances (both linear and nonlinear) associated with multiple current paths.

## VI. SUMMARY

We have compared the SEU responses of three SiGe HBT D flip-flop circuits using device simulation and circuit simulation, including one previously tested CSH hardened circuit and two unhardened circuits. One circuit performs significantly better than the other two circuits. The differences are explained by analyzing the differential output of the emitter coupled pair being hit. When SEU occurring at one of the output nodes of a differential pair does not affect the compliment output, the overall differential output might still be above or below the threshold required for correct logic to propagate to the output. This offers a certain amount of immunity to SEU in the circuit. Such immunity, however, is destroyed when the differential inputs and outputs are cross coupled at the transistor level, making such circuits more prone to SEU. These results suggest that cross coupling at transistor level, which gives rise to strong positive feedback, should be avoided in circuits intended for space applications.

## ACKNOWLEDGMENT

The authors would like to thank L. Cohn, B. Kauffman, K. LaBel, H. Brandhorst, D. Hame, S. Subbanna, D. Ahlgren, G. Freeman, B. Meyerson, D. Herman, and the IBM SiGe team for their contributions to this work.

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