

Logic Synthesis and Circuit Modeling of a Programmable Logic Gate Based on Controlled Quenching of Series-Connected Negative Differential Resistance Devices

Kevin J. Chen, *Member, IEEE*, and Guofu Niu, *Senior Member, IEEE*

Abstract—The circuit concept of programmable logic gates based on the controlled quenching of series-connected negative differential resistance (NDR) devices is introduced, along with the detailed logic synthesis and circuit modeling. At the rising edge of a clocked supply voltage, the NDR devices are quenched in the ascending order of peak currents that can be reordered by the control gates and input gates biases, thus, providing programmable logic functions. The simulated results agree well with the experimental demonstration of the programmable logic gate fabricated by a monolithic integrated resonant tunneling diode/high electron mobility transistor technology.

Index Terms—Controlled quenching, high electron mobility transistor (HEMT), negative differential resistance (NDR), programmable logic gate, resonant tunneling diode.

I. INTRODUCTION

FUNCTIONAL devices and circuits based on quantum effect resonant tunneling diodes (RTDs) and transistors (RTTs) have generated substantial research interest owing to their unique negative differential resistance (NDR) [1]–[4]. Taking advantage of the NDR feature, circuit complexity can be greatly reduced and new circuit applications have also emerged. Recently, RTDs and RTTs have been employed in a new category of circuits, namely, the monostable–bistable transition logic element (MOBILE) [5], which features a clocked supply voltage. These circuits take advantage of the NDR feature and consist of two NDR devices with different peak currents connected in series. The key to understanding the MOBILE circuit is a *controlled quenching* (see Section II for detailed definition) sequence of series-connected NDR devices. During a critical period when the clocked supply voltage rises, the voltage at the output node between the two NDR devices goes to one of the two stable states (low and high, corresponding to “0” and “1” in binary logic), depending on which NDR device is quenched first. Since the invention of MOBILE, a large number of functional circuits with faster operation speed [6] and far less device count [7]–[9] have been demonstrated with different device technologies, such

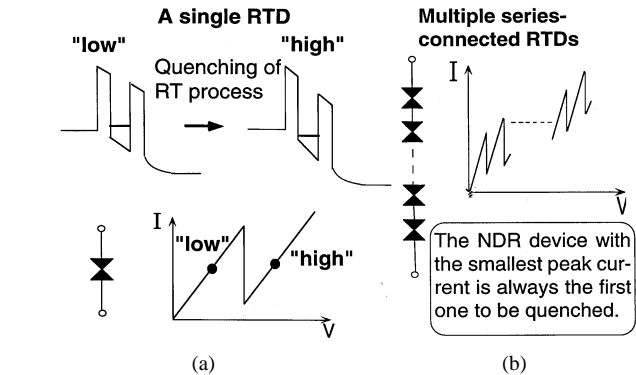


Fig. 1. Schematic energy diagram showing the quenching process of (a) a single RTD and (b) multiple RTDs connected in series.

as InP-based RTD/high electron mobility transistor (HEMT) integration [10], surface tunnel transistors [11], and resonant interband tunneling diode (RITD)/HEMT integration [12]. Since the core of the MOBILE operation is the controlled quenching (or switching) of series-connected NDR devices, the introduction of more than two NDR devices will provide more quenching sequence combinations and control flexibility. As a result, we have demonstrated an exclusive-OR logic gate [13] and a programmable logic gate [14] (the gate can be programmed to function as AND, OR, NAND, NOR, XOR, and XNOR) using three NDR devices connected in series. Design of large-scale integrated circuits using this new circuit concept requires accurate device models and logic synthesis.

In this paper, we provide detailed analysis on logic synthesis and circuit simulation using SPICE-based device models.

II. OPERATING PRINCIPLE

In a double-barrier quantum-well (QW) RTD, the quenching of the resonant-tunneling (RT) process is defined as the situation when the voltage drop across the RTD is large enough to pull the resonant state in the QW below the conduction band minimum in the emitter, as shown in Fig. 1(a). When this situation occurs, electrons from the emitter cannot tunnel through the resonant state. As a result, the RT process is quenched and the NDR is obtained. The RTD is in low-voltage state (logic “0”) before and high-voltage state (logic “1”) after the quenching. When multiple NDR devices are connected in series and a voltage is swept across them, the NDR devices will be quenched one by

Manuscript received May 7, 2002; revised August 29, 2002.

K. J. Chen is with the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: eekjchen@ust.hk).

G. Niu is with the Department of Electrical and Computer Engineering, Auburn University, Auburn, AL 36849 USA (email: guofu@eng.auburn.edu).

Digital Object Identifier 10.1109/JSSC.2002.807403

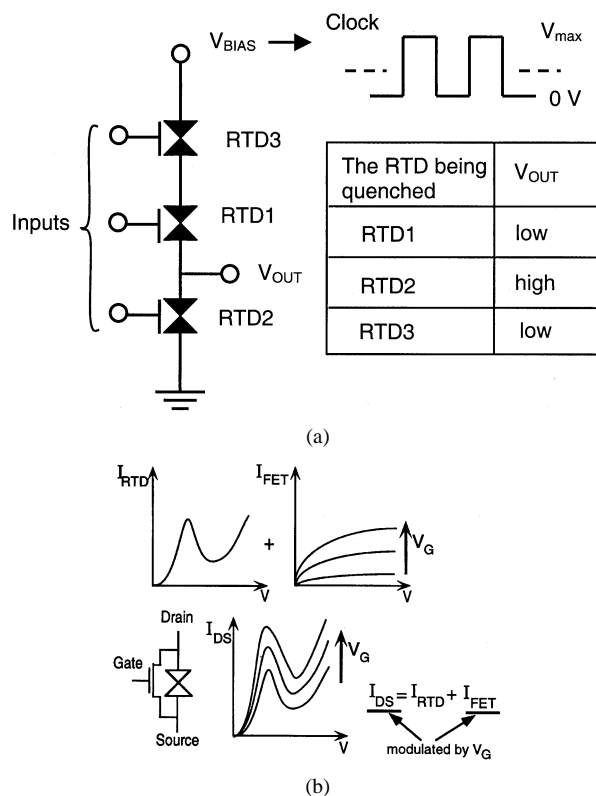


Fig. 2. (a) Basic operating principle of logic circuits based on controlled quenching of series-connected NDR devices. The inserted table lists the output when different RTDs (NDR devices) are quenched. (b) Schematics illustrating the modulation scheme of the peak current based on the parallel integration of an RTD and an FET. The total source-to-drain current I_{DS} is the sum of the currents through the RTD and FET: $I_{DS} = I_{RTD} + I_{FET}$. Since I_{FET} is modulated by the gate voltage, so is I_{DS} .

one in a predetermined sequence, as illustrated in Fig. 1(b). The quenching sequence will be determined by the magnitude of the peak currents of individual NDR device: the device with the lowest peak current is always quenched first, then the one with the second lowest peak will be quenched next, and so on. As a result, if the relation in the peak currents among the NDR devices can be changed by external signals (inputs and control signals), the quenching sequence can be varied and different logic functions can be realized.

Fig. 2(a) shows a circuit with three NDR devices (which are RTDs in parallel with current modulating FET gates) connected in series. The NDR devices are designed such that their peak currents differ from each other. The supply voltage V_{BIAS} is a clocked signal with a maximum value of V_{max} . V_{max} is chosen such that when V_{BIAS} increases from 0 V to V_{max} , only one of the NDR devices can be quenched and switch to the high-voltage state. The output is high (“1”) or low (“0”) depending on which NDR device is quenched, as summarized in Fig. 2(a). The NDR device with the lowest peak current is always the one quenched. Therefore, if external (input) voltages can modulate the peak currents of these NDR devices and change ascending order of the peak currents in different NDR devices, we can select the NDR device to be quenched and obtain certain logic functions. According to the operating principle stated above, the building block of logic circuits based on controlled quenching is an NDR device with a *controlled peak current*. Such a de-

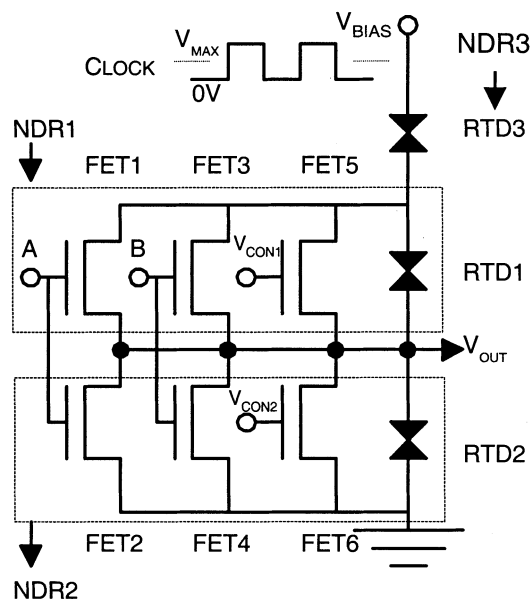


Fig. 3. Circuit configuration of the programmable logic gate. Areas of RTD1, RTD2, and RTD3 are $2 \times 3 \mu\text{m}^2$, $2 \times 4 \mu\text{m}^2$, and $2 \times 5.5 \mu\text{m}^2$, leading to different peak currents. Gate widths of FET1 and FET3 are $15 \mu\text{m}$, while those of FET2 and FET4 are $5 \mu\text{m}$. Gate width of FET5 and FET6 are 15 and $10 \mu\text{m}$, respectively. The detailed device characteristics are given in [13].

vice can be obtained from an integrated RTD/FET pair [7], as shown in Fig. 2(b). The total current of the RTD/FET pair is modulated by the FET gate voltage, despite the fact that the RTD current remains unchanged. The device model, logic synthesis, and circuit simulation discussed in this paper are based on an InP-based monolithic integrated RTD/HEMT technology, which includes both high-performance RTD and HEMT structures grown by molecular-beam epitaxy (MBE) on a semi-insulating InP substrate. The details of material growth and device fabrication have been reported in [10].

A programmable logic gate is designed as shown in Fig. 3. The circuit is extended to feature three NDR devices connected in series, with NDR1 between NDR2 (grounded) and NDR3 (connected to a clocked bias voltage V_{BIAS}), as shown in Fig. 3. NDR3 is a single RTD, while both NDR1 and NDR2 are integrated RTD/FET devices, in which one RTD and three FETs (two input gates and one control gate) are connected in parallel. The width of input FET gates (FET1 and FET3) in parallel with RTD1 is designed three times that of FET gates (FET2 and FET4) in parallel with RTD2 to provide higher transconductance. The RTD provides the fundamental NDR feature, while FET gates can modulate the peak current of NDR1 and NDR2. The supply voltage V_{BIAS} is a clocked signal with a maximum value of V_{max} , which is chosen such that only the NDR device with the smallest peak current can switch its bias status from peak to valley (defined as the *quenching* sequence) during a critical period when V_{BIAS} increases from 0 to V_{max} . The output is high (logic “1”) when NDR2 is quenched, and low (logic “0”) when either NDR1 or NDR3 is quenched. At certain control FET gate voltages, the peak current order among NDR devices at each input logic combination determines the truth table of logic output, thus, realizing certain logic functions. The peak current order among NDR devices at the same input

logic combination can be changed by programming the control gate voltages, thus obtaining different logic functions.

III. DEVICE MODEL AND PARAMETER EXTRACTION

The physics-based RTD current–voltage equation in [15] was implemented as a voltage-controlled current source in AIM-SPICE [16] which has a built-in HEMT (used as the FETs) model. Due to the lack of reliable measurement data in the NDR region, the RTD parameters extracted from general-purpose least square minimization often result in considerable error in peak (and valley) voltages and currents which are critical to the operation of the circuits demonstrated here. Thus, we propose another method capable of accurately fitting the critical RTD characteristics. The RTD current–voltage equation [15] is

$$I(V) = A \ln \left(\frac{1 + \exp\left(\frac{B + n_1 V}{V_t}\right)}{1 + \exp\left(\frac{B - n_1 V}{V_t}\right)} \right) \times \left(\frac{\pi}{2} + \tan^{-1}\left(\frac{C - n_1 V}{D}\right) \right) + H \left(\exp\left(\frac{n_2 V}{V_t}\right) - 1 \right) \quad (1)$$

where $V_t = kT/q$ is the thermal voltage. The first part describes the basic resonant tunneling process, and produces peak current and negative differential resistance with A , B , C , D , and n_1 as parameters. The second part produces the exponentially rising region above the valley voltage using standard diode equation with H and n_2 as parameters. Note that $B - C$ in the original equation of [15] is replaced by B here since $B - C$ in the original equation can be viewed as an independent variable without loss of generality, thereby simplifying expressions of partial derivatives of I to model parameters in parameter extraction, and making its implementation in the circuit simulator easier. A , B , C , D , n_1 , n_2 , and H are determined by solving the following system of equations.

1) Set the differential conductance at $V = 0$ to its measurement value g_0

$$\left. \frac{dI(V)}{dV} \right|_{V=0} = g_0. \quad (2)$$

2) Set the differential conductance at the peak voltage V_{peak} to 0

$$\left. \frac{dI(V)}{dV} \right|_{V=V_{\text{peak}}} = 0. \quad (3)$$

3) Set the current at V_{peak} to the peak current I_{peak}

$$I(V_{\text{peak}}) = I_{\text{peak}}. \quad (4)$$

4) Set the differential conductance at the valley voltage V_{valley} to 0

$$\left. \frac{dI(V)}{dV} \right|_{V=V_{\text{valley}}} = 0. \quad (5)$$

5) Set the current at V_{valley} to the valley current I_{valley}

$$I(V_{\text{valley}}) = I_{\text{valley}}. \quad (6)$$

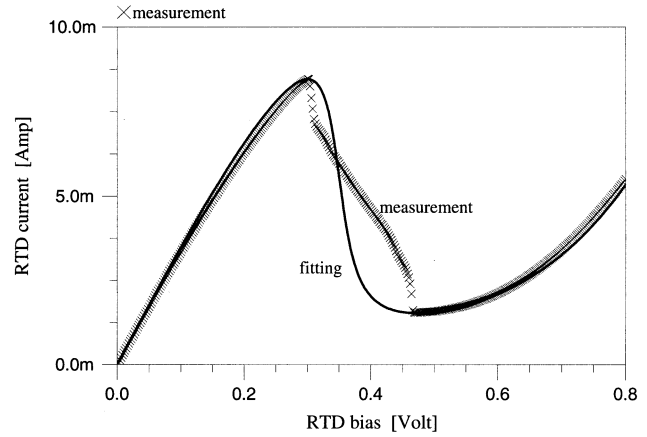


Fig. 4. RTD current versus voltage from measurement of fabricated device [13] and fitting using the proposed parameter extraction method.

6) Set the current to be equal to $(I_{\text{peak}} + I_{\text{valley}})/2$ at a bias voltage V_1 (which is above V_{valley}) where the same current was measured

$$I(V_1) = \frac{I_{\text{peak}} + I_{\text{valley}}}{2} \quad (V_1 > V_{\text{valley}}). \quad (7)$$

7) Set the current at V_2 defined as $(V_{\text{valley}} + V_1)/2$ to its measured value I_2

$$I(V_2) = I_2 \quad \left(V_2 \equiv \frac{V_{\text{valley}} + V_1}{2} \right) \quad (8)$$

where the differential conductance is given by

$$\begin{aligned} \frac{dI(V)}{dV} &= \frac{n_1}{V_t} A \\ &\times \frac{\exp\left(\frac{B}{V_t}\right) \left[\exp\left(\frac{n_1 V}{V_t}\right) + \exp\left(-\frac{n_1 V}{V_t}\right) + 2 \exp\left(\frac{B}{V_t}\right) \right]}{\left[1 + \exp\left(\frac{B + n_1 V}{V_t}\right) \right] \left[1 + \exp\left(\frac{B - n_1 V}{V_t}\right) \right]} \\ &\times \left(\frac{\pi}{2} + \tan^{-1}\left(\frac{C - n_1 V}{D}\right) \right) \\ &- \frac{n_1}{D} A \ln \left(\frac{1 + \exp\left(\frac{B + n_1 V}{V_t}\right)}{1 + \exp\left(\frac{B - n_1 V}{V_t}\right)} \right) \frac{1}{1 + \left(\frac{C - n_1 V}{D}\right)^2} \\ &+ H \frac{n_2}{V_t} \exp\left(\frac{n_2 V}{V_t}\right). \end{aligned} \quad (9)$$

Equations (3) and (5) ensure the occurrences of peak and valley voltage at their measured values, and (4) and (6) further guarantee the values of peak and valley currents. Equations (7) and (8) are mainly used to extract n_2 and H , which account for the dominating thermoionic current when the RTD bias is above V_{valley} . Equation (1) is used together with (3)–(8) to form a system of seven equations to extract the seven parameters uniquely. Fig. 4 shows the comparison between measured current–voltage characteristic of the fabricated RTD [13] and fitting from (1) with A , B , C , D , n_1 , n_2 , and H extracted using

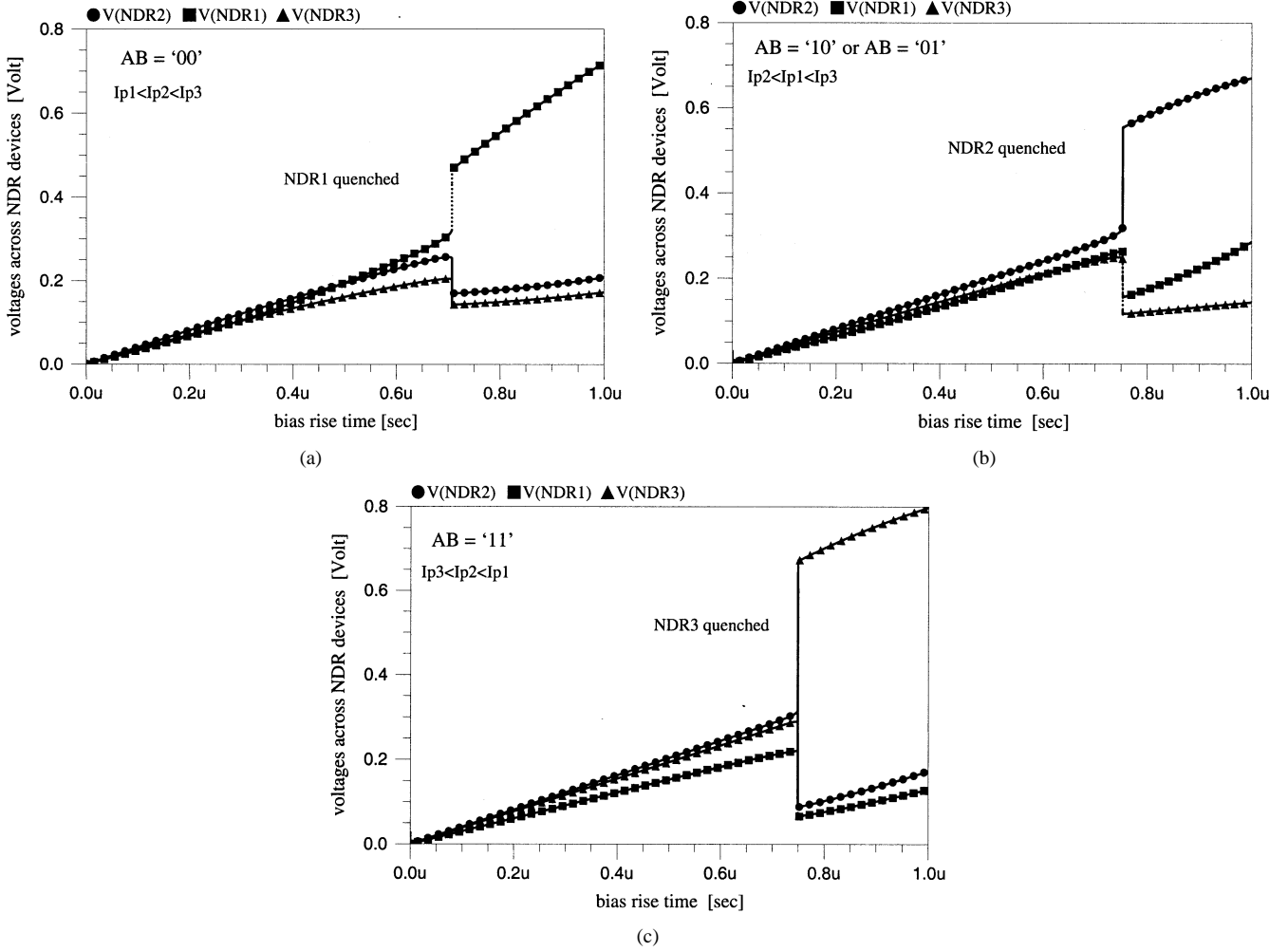


Fig. 5. Traces of voltages across NDR1 through NDR3 when V_{BIAS} rises from 0 to V_{max} of 1.1 V at various input logic combinations.

the proposed method. The RTD has an area of $2 \times 5 \mu\text{m}^2$. Measurement data in the NDR region are not reliable due to the well-known problem of self-oscillation. $A = 0.483951$, $B = -0.072975$, $C = 0.112192$, $D = 0.007098$, $n_1 = 0.321298$, $n_2 = 0.145963$, and $H = 0.059034$. Parameters of the HEMT model in AIM-SPICE [16] are determined from the measured electrical characteristics of the fabricated HEMTs [13]. The key parameters in the HEMT model include the threshold voltage $V_T = -0.25$ V, the peak transconductance $g_{m, \text{max}} = 900$ mS/mm, and the source-drain saturation current $I_{dss} = 550$ mA/mm. Considering that the parasitic and intrinsic capacitances associated with the HEMT channel charge storage are much larger than the capacitances in the RTD, we did not include the RTD capacitances in the circuit simulation. Nevertheless, for accurate circuit simulation at the higher clock rate, it will be necessary to include the capacitance of the RTD, since a slight change in displacement current through the capacitive path of the RTD can result in changes in the peak currents of the NDR devices and, therefore, alter the controlled quenching sequence.

IV. LOGIC SYNTHESIS

As an example, to realize XOR logic function, control gate voltages V_{CON1} and V_{CON2} are programmed such that $I_{p1} <$

$I_{p2} < I_{p3}$ (NDR1 quenched, output low) when both A and B are logic “0,” $I_{p2} < I_{p1} < I_{p3}$ (NDR2 quenched, output high) when either A or B is logic “1” (0.6 V), and $I_{p3} < I_{p2} < I_{p1}$ (NDR3 quenched, output low) when both A and B are logic “1.” V_{CON1} and V_{CON2} satisfying such requirement can be determined from

$$\begin{aligned} I_{p1} &= I_{p, \text{RTD1}} + 2I_{0, \text{FET1}} + (A + B)\Delta I_{\text{FET1}} + I_{\text{CON1}} \\ I_{p2} &= I_{p, \text{RTD2}} + 2I_{0, \text{FET2}} + (A + B)\Delta I_{\text{FET2}} + I_{\text{CON2}} \end{aligned} \quad (10)$$

where $I_{p, \text{RTD1}}$ and $I_{p, \text{RTD2}}$ are peak currents of RTD1 and RTD2, $I_{0, \text{FET1}}$ and $I_{0, \text{FET2}}$ are the drain currents of FET1 (FET3) and FET2 (FET4) when input A (B) is logic “0,” and ΔI_{FET1} and ΔI_{FET2} are the modulation of drain currents of FET1 (FET3) and FET2 (FET4) when input A (B) rises from “0” to “1.” All the FET currents are determined by assuming that RTD1 and RTD2 are biased at the peak state. The fact that the source of FETs in parallel with RTD1 is not grounded ($V_{\text{OUT}} \neq 0$) should be noted and taken into account. I_{CON1} and I_{CON2} are the drain current through the control gates FET5 and FET6, respectively. $V_{\text{CON1}} = 0.4$ V and $V_{\text{CON2}} = 0.15$ V satisfying the requirement of XOR are chosen here. Similarly, other

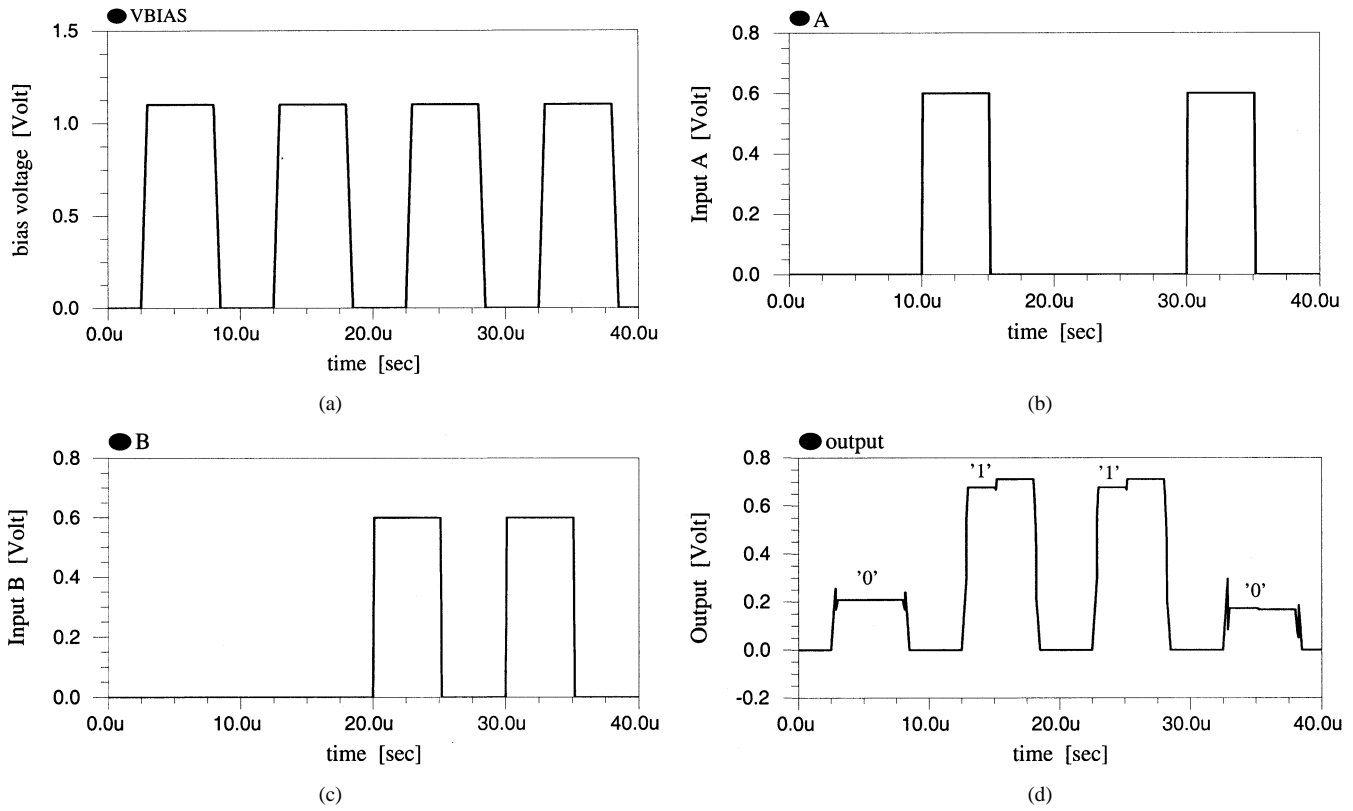


Fig. 6. Input and output traces of the two-input circuit programmed as XOR gate. Input sequence (AB) is 00, 10, 01, and 11 at the rising edges of the clocked V_{BIAS} .

logic functions including AND, OR, NAND, and NOR can be synthesized by programming V_{CON1} and V_{CON2} according to (10).

- AND: $I_{p1} < I_{p2} < I_{p3}$ (NDR1 quenched, output low) when $AB = "00," "01,"$ and $"10,"$ and $I_{p2} < I_{p1} < I_{p3}$ (NDR2 quenched, output high) when $AB = "11."$
- OR: $I_{p1} < I_{p2} < I_{p3}$ (NDR1 quenched, output low) when $AB = "00,"$ and $I_{p2} < I_{p1} < I_{p3}$ (NDR2 quenched, output high) when $AB = "01," "10,"$ and $"11."$
- NAND: $I_{p2} < I_{p3} < I_{p1}$ (NDR2 quenched, output high) when $AB = "00," "01,"$ and $"10,"$ and $I_{p3} < I_{p2} < I_{p1}$ (NDR3 quenched, output low) when $AB = "11."$
- NOR: $I_{p2} < I_{p3} < I_{p1}$ (NDR2 quenched, output high) when $AB = "00,"$ and $I_{p3} < I_{p2} < I_{p1}$ (NDR3 quenched, output high) when $AB = "01," "10,"$ and $"11."$

For the realization of the XNOR gate, it is necessary to increase the amplitude of the clocked V_{BIAS} so that two NDR devices can be quenched when V_{BIAS} reaches its peak value. The currents passing through the control gates, I_{CON1} and I_{CON2} , are chosen such so that the following relations are achieved. When $AB = "00,"$ $I_{p1} < I_{p2} < I_{p3}$, so that NDR1 and NDR2 are quenched, and the output is high. When $AB = "01,"$ or $"10,"$ $I_{p1} < I_{p3} < I_{p2}$, so that NDR1 and NDR3 are quenched, and the output becomes low. When $AB = "11,"$ we have $I_{p3} < I_{p2} < I_{p1}$ so that NDR2 and NDR3 are quenched, and the output becomes high again.

V. CIRCUIT OPERATION AND EXPERIMENTAL RESULTS

Again, XOR is used as an example to explain circuit operation. Fig. 5 shows the simulated traces of voltage drop across each

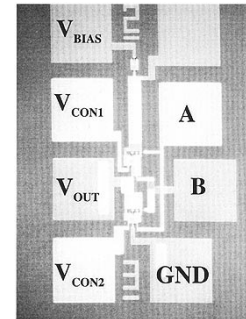


Fig. 7. Photomicrograph of the fabricated chip with monolithically integrated RTD and HEMT.

NDR device (V_{NDR1} , V_{NDR2} and V_{NDR3}) when a linear ramp V_{BIAS} with V_{max} of 1.1 V is applied. V_{NDR2} is also the output. In simulation, the time step is controlled sufficiently small to avoid finding solutions which are mathematically possible but physically incorrect. When both A and B are "0," the voltage drop across each NDR device all increase with V_{BIAS} first until the moment at which the supply current reaches the peak current of NDR1 which is the smallest, then NDR1 is quenched because of negative differential resistance, thereby switching its bias status from peak to valley, as can be seen from the figure. Since the sum of voltage drops across all NDR devices is the same at the two moments right before and after the quenching, voltage drop across NDR2 and voltage drop across NDR3 decrease correspondingly, and the output becomes low ("0"). When either A or B is logic "1" while the other is "0," both I_{p1} and I_{p2} increase compared to $AB = "00,"$ however, I_{p1} becomes higher

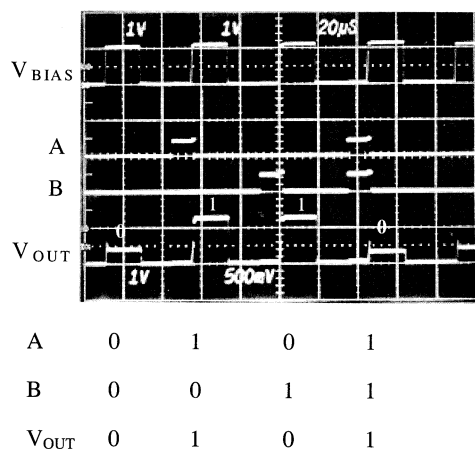


Fig. 8. Experimental input and output traces of the circuit in Fig. 3 when programmed as XOR gate.

TABLE I
EXPERIMENTAL BIAS CONDITIONS FOR EACH LOGIC FUNCTION
OBTAINED IN A FABRICATED CIRCUIT AS SHOWN IN FIG. 3

V_{\max} (V)	V_{CON1} (V)	V_{CON2} (V)	Logic Function
1.1	0.1	0.05	AND
1.1	0.4	0.05	OR
1.1	0.7	0.15	NAND
1.1	0.8	0.35	NOR
1.1	0.4	0.15	XOR
2.2	0.1	0.3	XNOR

than I_{p2} , because of higher transconductance of input gates in parallel with NDR1 ($\Delta I_{\text{FET1}} > \Delta I_{\text{FET2}}$); and both of them are less than I_{p3} . With increasing bias, V_{NDR1} through V_{NDR3} all increase first; at the moment the supply current reaches the peak current of I_{p2} which is the smallest, NDR2 is quenched, and the output becomes high (“1”). When both A and B are “1,” the modulation of peak currents I_{p1} and I_{p2} are doubled so that both I_{p1} and I_{p2} are higher than I_{p3} according to the programmed control gate voltages. Similarly, with rising bias, NDR3 is quenched when the supply current reaches I_{p3} which is the smallest, the voltage across NDR3 switches from peak to valley, thus, lowering voltages across NDR1 and NDR2, and turning the output to low (“0”). Fig. 6 shows the input and output traces of the circuit when programmed as the XOR gate with clocked V_{BIAS} . The logic level of output is determined during the critical period when V_{BIAS} rises and remains unchanged until V_{BIAS} switches back to 0 V, despite the change in inputs. It should be noted that the change in inputs does cause a minor change of voltage level in output. Traces of voltage drop across each NDR device when V_{BIAS} rises for other logic functions (controlled by V_{CON1} and V_{CON2}) have also been simulated and the logic operations have been confirmed. In addition, N -input programmable logic gates can be realized by simply increasing number of input FETs in parallel with NDR2 and NDR3, and can be programmed as AND, OR, NAND, NOR, and NON-EQUIVALENCE (output low only when N -inputs are equal to one an-

other). Apart from the programmable flexibility, all the input gates are in parallel, thus, avoiding the problem of charging through the chain of N load transistor in series (either n - or p -type depending on functions) in conventional N -input gates, and making it possible to obtain a single-stage delay at a large number of inputs. Logic synthesis of the N -input gate is similar to the two-input case.

The circuit is fabricated on an epitaxial wafer which includes both FET and RTD structures grown by MBE on a semi-insulating InP substrate. Device fabrication details are the same as those in [10]. The photomicrograph of the fabricated chip is shown in Fig. 7. Fig. 8 shows the measured input and output traces of this circuit when programmed to function as XOR gate. Other logic functions (AND, OR, NAND, NOR, XNOR) have also been demonstrated experimentally by programming the control gate voltages V_{CON1} and V_{CON2} [14]. Table I shows the combination of the control voltages for different logic operations of the programmable logic gate. It should be noted that the magnitude V_{\max} of the clocked V_{BIAS} has to be increased to 2.2 V to obtain XNOR operation, as discussed in the end of Section IV. This increase in V_{\max} simply implies the case where two NDR devices are quenched instead of one.

VI. CONCLUSION

Logic synthesis and circuit operation of programmable logic gates based on controlled quenching of series-connected NDR devices have been presented. The circuit features a single stage delay with fewer components than implementation using conventional transistors and programmable flexibility. The circuit also has the advantage of resistor-free process over other RTD-based logic circuits, implying improved manufacturability and more compact layout.

REFERENCES

- [1] F. Capasso, S. Sen, F. Beltram, L. M. Lunardi, A. S. Vengurlekar, P. R. Smith, N. J. Shah, R. J. Malik, and A. Y. Cho, “Quantum functional devices: Resonant-tunneling transistors, circuits with reduced complexity and multiple-valued logic,” *IEEE Trans. Electron Devices*, vol. 36, pp. 2065–2082, Oct. 1989.
- [2] P. Mazumder, S. Kulkarni, M. Bhattacharya, J. P. Sun, and G. I. Haddad, “Digital circuit applications of resonant tunneling devices,” *Proc. IEEE*, vol. 86, pp. 664–686, Apr. 1998.
- [3] P. v. d. Wagt, A. Seabaugh, and E. A. Beam, “RTD/HFET low standby power SRAM gain cell,” in *Tech. Dig. IEDM*, 1996, pp. 425–428.
- [4] K. J. Chen and M. Yamamoto, “Frequency multipliers using InP-based resonant-tunneling high electron mobility transistors (RTHEMTs),” *IEEE Electron Device Lett.*, vol. 17, pp. 235–238, May 1996.
- [5] K. Maezawa and T. Mizutani, “A new resonant tunneling logic gate employing monostable–bistable transition,” *Jpn. J. Appl. Phys.*, vol. 32, pp. L42–L44, 1993.
- [6] K. Maezawa, H. Matsuzaki, K. Awai, T. Otsuji, and M. Yamamoto, “High-speed and low-power operation of a resonant tunneling logic gate MOBILE,” *IEEE Electron Device Lett.*, vol. 19, pp. 80–82, Mar. 1998.
- [7] K. J. Chen, K. Maezawa, and M. Yamamoto, “InP-based high-performance monostable–bistable transition logic elements (MOBILEs) using integrated multiple-input resonant-tunneling devices,” *IEEE Electron Device Lett.*, vol. 17, pp. 127–129, Mar. 1996.
- [8] C. Pacha, U. Auer, C. Burwick, P. Closekötter, A. Brennemann, W. Prost, F. Tegude, and K. F. Gosser, “Threshold logic circuit design of parallel adders using resonant tunneling devices,” *IEEE Trans. VLSI Syst.*, vol. 8, pp. 558–572, Oct. 2000.
- [9] M. Bhattacharya and P. Mazumder, “Noise margins of threshold logic gates containing resonant tunneling diodes,” *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 1080–1085, Oct. 2000.

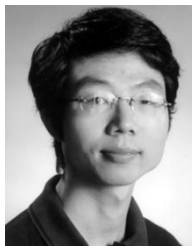
- [10] K. J. Chen, K. Maezawa, T. Waho, and M. Yamamoto, "Device technology for monolithic integration of InP-based resonant-tunneling diode and HEMT," *IEICE Tran. Electron.*, vol. E79-C, pp. 1515–1524, Nov. 1996.
- [11] T. Uemura and T. Baba, "Demonstration of a novel multiple-valued T-gate using multiple-junction surface tunnel transistors and its application to three-valued data flop-flop," in *Proc. 30th Int. Symp. Multiple-Valued Logic*, Portland, OR, 2000, pp. 305–310.
- [12] P. Fay, J. Lu, Y. Xu, G. H. Bernstein, A. Gonzalez, P. Mazumder, D. H. Chow, and J. N. Schulman, "Digital integrated circuit using integrated InAlAs/InGaAs/InP HEMTs and InAs/AlSb/GaSb RITDs," *Electron. Lett.*, vol. 37, no. 12, pp. 758–759, June 2001.
- [13] K. J. Chen, T. Waho, K. Maezawa, and M. Yamamoto, "An exclusive-OR logic circuit based on the controlled quenching of series-connected negative differential resistance devices," *IEEE Electron Device Lett.*, vol. 17, pp. 309–311, June 1996.
- [14] —, "Programmable logic gate based on controlled quenching of series-connected negative differential resistance devices," in *Proc. IEEE 54th Device Research Conf.*, Santa Barbara, CA, June 1996, pp. 170–171.
- [15] J. N. Schulman, H. J. De Los Santos, and D. H. Chow, "Physics-based RTD current–voltage equation," *IEEE Electron Device Lett.*, vol. 17, pp. 220–222, May 1996.
- [16] K. Lee, M. Shur, T. A. Fjeldly, and T. Ytterdal, *Semiconductor Device Modeling for VLSI*. Englewood Cliffs, NJ: Prentice-Hall, 1993.



Kevin J. Chen (M'96) received the B.S. degree in electronics from Peking University, Beijing, China, in 1988 and the Ph.D. degree from the University of Maryland, College Park, in 1993.

From January 1994 to December 1995, he was a Research Engineer with NTT LSI Laboratories, Atsugi, Japan, engaging in the research and development of functional quantum effect devices and heterojunction FETs (HFETs). In particular, he developed the device technology for monolithic integration of resonant tunneling diodes and HFETs (MISFET and HEMT) on both GaAs and InP substrates, for applications in ultrahigh-speed signal processing and communication systems. He also developed the Pt-based buried gate technology that is widely used in the enhancement-mode HEMT devices. From 1996 to 1998, he was an Assistant Professor with the Department of Electronic Engineering, City University of Hong Kong, carrying out research on high-speed device and circuit simulations. He then joined the Wireless Semiconductor Division, Agilent Technologies, Inc. (formerly Hewlett-Packard), Santa Clara, CA, in 1999, working on RF power amplifiers used in dual-band GSM/DCS wireless handsets. His work at Agilent covered RF characterization and modeling of microwave transistors, RF IC and package design. He joined the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Hong Kong, as an Assistant Professor in November 2000. His research interests include fabrication, characterization and modeling techniques of novel RF/microwave devices (both active and passive), design of RF power amplifiers, and RF micro-electromechanical systems.

Dr. Chen received a CUSPEA fellowship in 1988.



Guofu Niu (M'97–SM'02) was born in Henan, China, in December 1971. He received the B.S. (Honors), M.S., and Ph.D. degrees in electrical engineering from Fudan University, Shanghai, China, in 1992, 1994, and 1997, respectively.

From December 1995 to January 1997, he was a Research Assistant with City University of Hong Kong, working on mixed-level device/circuit simulation and quantum effect programmable logic gates. From May 1997 to May 2000, he conducted postdoctoral research at Auburn University, Auburn, AL, focusing on SiGe RF devices. He joined the faculty of Auburn University in June 2000, and is currently an Associate Professor in the Department of Electrical and Computer Engineering. His current research activities include SiGe devices and circuits, noise, single-event effects, SiC devices, low temperature electronics, and TCAD. He served on the Program Committee of the Asia-South-Pacific Design Automation Conference (ASPAC) in 1997. He has published more than 40 journal papers and more than 40 conference papers related to his research.

Dr. Niu currently serves on the Program Committee of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He has served as a reviewer for many journals, including the IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and the IEEE MICROWAVE AND GUIDED WAVE LETTERS. He received the T. D. Lee physics award in 1993 and 1994. He has been listed in *Who's Who in America*.