Homework for ELEC6710, Due Next Tue Class

1. Basic Requirement: For the 2D SiGe HBT RF example, modify the collector bias VCE, so that you can overlay fT-IC curves for VCE=0.5V, 1.0V, 2.0V, and 3.0V. You might pick a fast tux machine, or simply run your tasks on multiple machines in parallel if timing is an issue. On my faster machine, each simulation takes about 5 minutes. Include your code, highlight codes that took most of your time to figure out, and output plots.
2. Advanced Requirement (Optional):
    a. For VCE=2.0V, examine the 1D cuts through the center of emitter for 5 different IC but representative IC values on your fT versus IC curve. Choose 1 point before peak fT, 1 point around peak fT, and 3 points in the fT roll-off portion. Examine n, p, space charge density and e-field for these bias points, overlay them. This was what I wanted for the previous homework.
    b. For a fixed IC of 1mA/um, examine the 1D cuts through emitter center for all the VCE's simulated.
    c. Discuss in your own words, with the Tecplot graphics obtained above, the impact of high IC on fT, and the impact of VCE on the fT versus IC characteristics.