N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max $T_A = +25°C$
60V	7.5Ω @ V_{GS} = 5V	210mA

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Motor Control
- Power Management Functions

Features

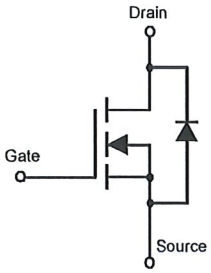
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Small Surface Mount Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Notes 3 & 4)**
- **Qualified to AEC-Q101 standards for High Reliability**

Mechanical Data

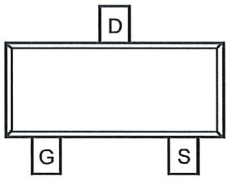
- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

SOT23

Top View



Equivalent Circuit



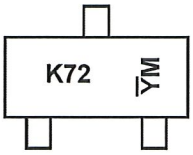
Top View

Ordering Information (Note 5)

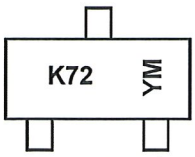
Part Number	Compliance	Case	Packaging
2N7002-7-F	Standard	SOT23	3,000/Tape & Reel
2N7002-13-F	Standard	SOT23	10,000/Tape & Reel
2N7002Q-7-F	Automotive	SOT23	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Product manufactured with Date Code V12 (week 50, 2008) and newer are built with Green Molding Compound. Product manufactured prior to Date Code V12 are built with Non-Green Molding Compound and may contain Halogens or Sb_2O_3 Fire Retardants.
5. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

K72 = Product Type Marking Code
YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
$\overline{Y}\overline{M}$ = Date Code Marking for CAT (Chengdu Assembly/ Test site)
Y or $\overline{Y}$ = Year (ex: A = 2013)
M = Month (ex: 9 = September)

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Code	N	P	R	S	T	U	V	W	X	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	60	V
Drain-Gate Voltage $R_{GS} \leq 1.0M\Omega$			V_{DGR}	60	V
Gate-Source Voltage		Continuous Pulsed	V_{GSS}	±20 ±40	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +85°C T_A = +100°C	I_D	170 120 105	mA
Continuous Drain Current (Note 7) V_{GS} = 10V	Steady State	T_A = +25°C T_A = +85°C T_A = +100°C	I_D	210 150 135	mA
Maximum Body Diode Forward Current (Note 7)	Pulsed Continuous		I_S	0.5 2	A
Pulsed Drain Current (10μs pulse, duty cycle = 1%)			I_{DM}	800	mA

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Total Power Dissipation	(Note 6)	P_D	370	mW
	(Note 7)		540	
Thermal Resistance, Junction to Ambient	(Note 6)	$R_{\theta JA}$	348	°C/W
	(Note 7)		241	
Thermal Resistance, Junction to Case	(Note 7)	$R_{\theta JC}$	91	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage		BV_{DSS}	60	70	—	V	V_{GS} = 0V, I_D = 10μA
Zero Gate Voltage Drain Current	@ T_C = +25°C @ T_C = +125°C	I_{DSS}	—	—	1.0 500	μA	V_{DS} = 60V, V_{GS} = 0V
Gate-Body Leakage		I_{GSS}	—	—	±10	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage		$V_{GS(th)}$	1.0	—	2.5	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	@ T_J = +25°C @ T_J = +25°C @ T_J = +125°C	$R_{DS(ON)}$	—	3.2 — 4.4	7.5 5.0 13.5	Ω	V_{GS} = 5.0V, I_D = 0.05A V_{GS} = 10V, I_D = 0.5A V_{GS} = 10V, I_D = 0.5A
On-State Drain Current		$I_{D(ON)}$	0.5	1.0	—	A	V_{GS} = 10V, V_{DS} = 7.5V
Forward Transconductance		g_{FS}	80	—	—	mS	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage		V_{SD}	—	0.78	1.5	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance		C_{iss}	—	22	50	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance		C_{oss}	—	11	25	pF	
Reverse Transfer Capacitance		C_{rss}	—	2.0	5.0	pF	
Gate resistance		R_g	—	120	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 4.5V)		Q_g	—	223	—	pC	V_{DS} = 10V, I_D = 250mA
Gate-Source Charge		Q_{gs}	—	82	—		
Gate-Drain Charge		Q_{gd}	—	178	—		
SWITCHING CHARACTERISTICS (Note 9)							
Turn-On Delay Time		$t_{D(on)}$	—	2.8	—	ns	V_{DD} = 30V, I_D = 0.2A, R_L = 150Ω, V_{GEN} = 10V, R_{GEN} = 25Ω
Turn-On Rise Time		t_r	—	3.0	—		
Turn-Off Delay Time		$t_{D(off)}$	—	7.6	—		
Turn-Off Fall Time		t_f	—	5.6	—		

Notes:
6. Device mounted on FR-4 PCB, with minimum recommended pad layout
7. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

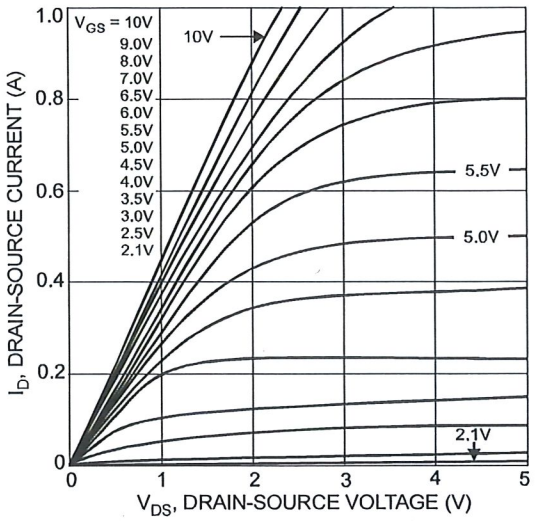


Fig. 1 On-Region Characteristics

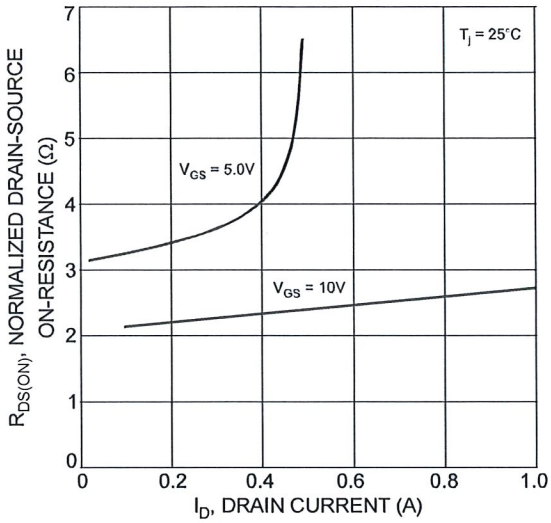


Fig. 2 On-Resistance vs. Drain Current

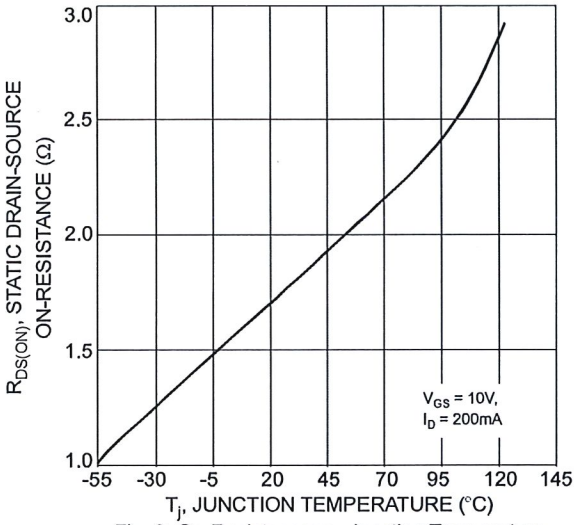


Fig. 3 On-Resistance vs. Junction Temperature

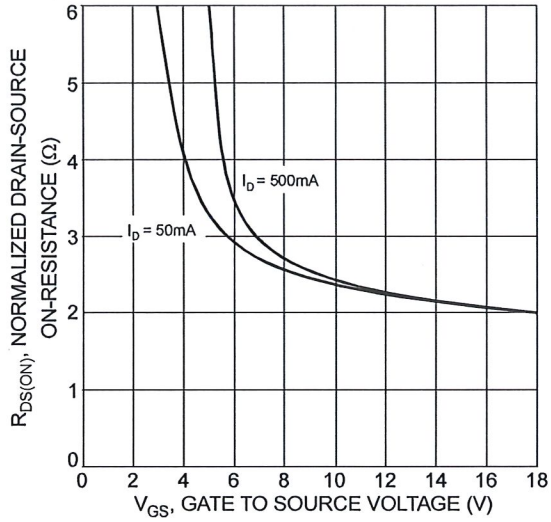


Fig. 4 On-Resistance vs. Gate-Source Voltage

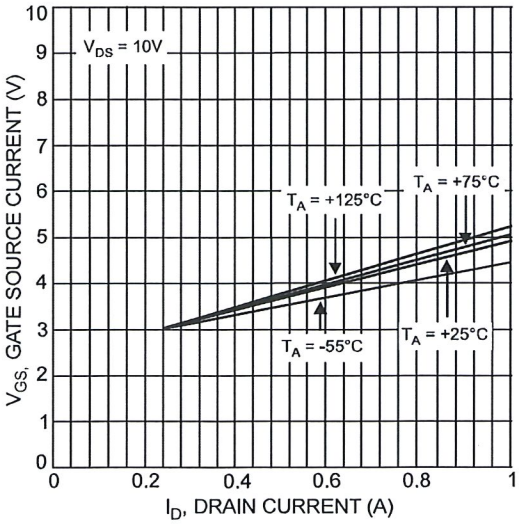


Fig. 5 Typical Transfer Characteristics

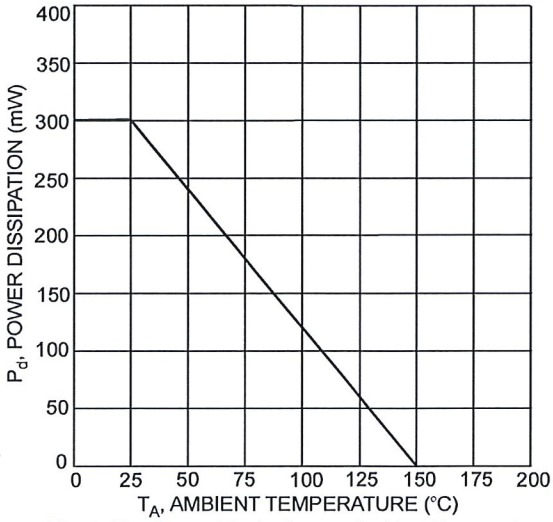
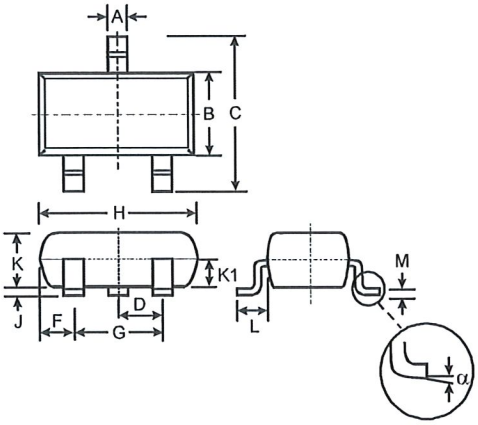


Fig. 6 Max Power Dissipation vs. Ambient Temperature

Package Outline Dimensions

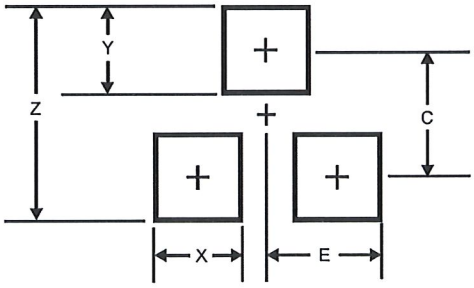
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT23			
Dim	Min	Max	Typ
A	0.37	0.51	0.40
B	1.20	1.40	1.30
C	2.30	2.50	2.40
D	0.89	1.03	0.915
F	0.45	0.60	0.535
G	1.78	2.05	1.83
H	2.80	3.00	2.90
J	0.013	0.10	0.05
K	0.903	1.10	1.00
K1	-	-	0.400
L	0.45	0.61	0.55
M	0.085	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.9
X	0.8
Y	0.9
C	2.0
E	1.35

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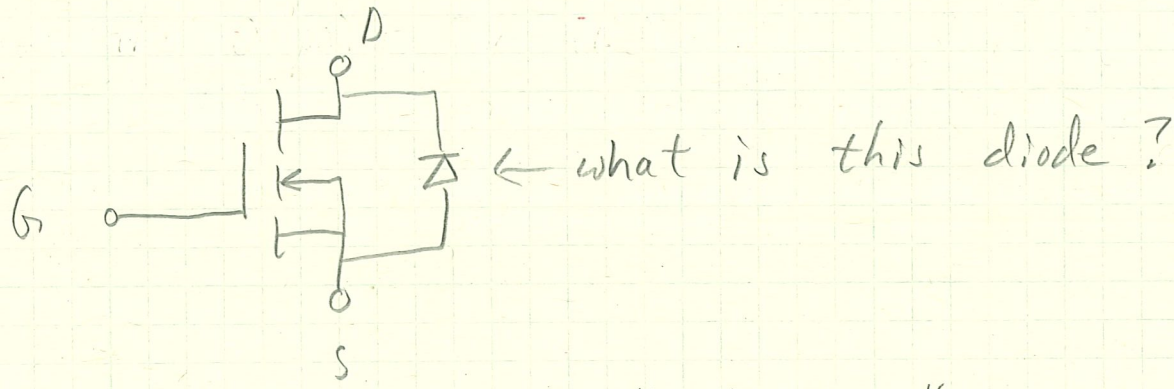
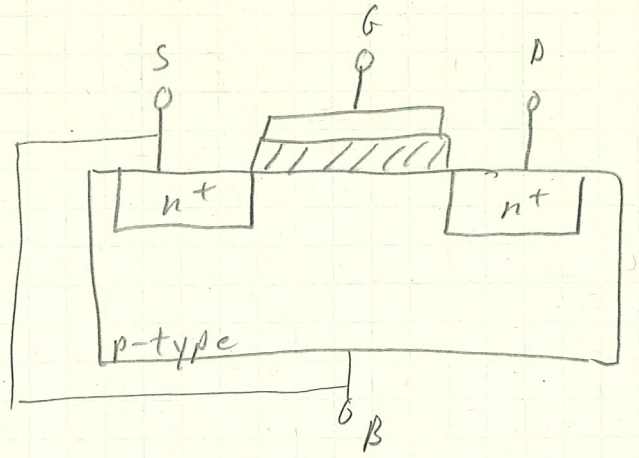
1) 2N7002 NMOS datasheet \$0.19/ea → Digikey



This diode is called the "body diode" and is part of the MOSFETs structure



with S + B shorted, if $V_{DS} < 0$, the pn junction between n^+ (Drain) and p-type is forward biased, and current will flow when $V_{SD} > V_{on}$ of the body diode

From 2N7002 datasheet:

$V_{(BR)DSS}$: Drain-Source breakdown voltage
→ the maximum voltage the NMOS is rated to block between D + S when $V_{GS} = 0V$

V_{GSS} : Maximum voltage that can be applied between the Gate and Source while the Drain and Source are shorted

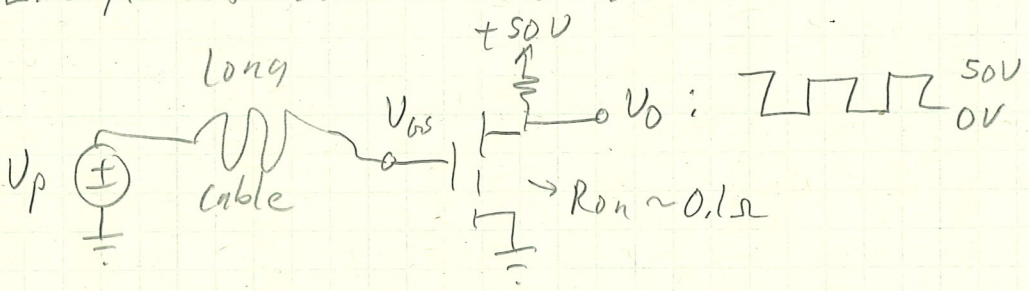
Notice that $V_{(BR)DSS}$ is 60V while V_{GSS} is ±20V continuous and ±40V pulsed

Exceeding $V_{(BR)DSS}$ or V_{GSS} can break the NMOS.

My experience : when a MOSFET fails, it usually results in a permanent short between Drain and Source

For the 2N7002: max continuous i_D at 25°C → 210mA } more i_D will overheat FET
max 1% Duty Cycle pulsed i_D → 800mA

Example of what not to do



V_{GS} ideal : 5V, 0

V_{GS} actual : 5V, 0 ← Gibbs phenomenon due to undesirable cable impedance

↑ exceeded V_{GSS}

FET fail: on all the time

↳ FET caught on fire

2. Other types of MOSFETs

a. Depletion-mode MOSFET

For NMOS, n-type doping added under gate structure to create a resistive layer between Drain and Source

V_{GS} must be pulled negative a few Volts to deplete this layer of e's and turn off the device

$\therefore V_{TN} < 0$, possibly $V_{TN} = -2V$

b. Junction Field-Effect (JFET) transistor

→ a pn junction depletion-mode device

$\therefore$ a negative V_{GS} is needed to deplete the channel of charge carriers and turn it off

→ important in RF applications and in BiFET IC processes: JFETs and BJT's (Bipolar Junction Transistors)

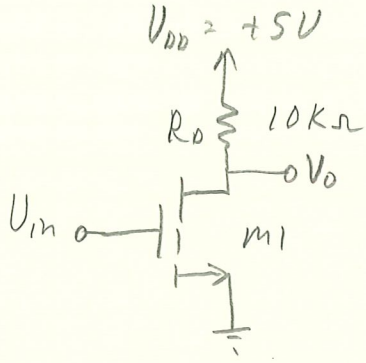
c. Review NMOS or N-JFET

Enhancement Mode Devices → $V_{GS} > V_{TN}$ to turn the device on: for $i_D > 0A$

Depletion Mode Devices: $\therefore V_{TN} < 0$ and $V_{GS} < 0 < V_{TN}$ to turn off the device, making $i_D = 0A$

MOSFET Digital Circuits → Elements from Chapter 6

consider this circuit:



$k_n = 1mA/V^2$

$\lambda = 0\ V^{-1}$

$V_{TN} = 1V$

Lets specify : $V_{in} = 0V$ or $V_{in} = 5V$ only

① For $V_{in} = 0V$

$V_{GS} - V_{TN} = -1V < 0$

∴ M1 is in cutoff

$I_D = 0A \rightarrow V_O = +5V$

② For $V_{in} = +5V$

$V_{GS} - V_{TN} = 5 - 1 = 4V > 0$

∴ M1 is on

→ Lets assume triode

$$\therefore \quad V_{DS} = V_O = V_{DD} - I_D R_D$$

$$\text{or} \quad I_D = \frac{V_{DD} - V_O}{R_D}$$

$$\text{or} \quad I_D = \frac{5 - V_O}{10{,}000} \quad ①$$

$$\therefore \quad I_D = k_n (V_{GS} - V_{TN} - 0.5V_{DS}) V_{DS}$$

$$= k_n (V_{GS} - V_{TN} - 0.5V_O) V_O$$

$$\text{or} \quad I_D = (1\times10^{-3})(4 - 0.5V_O) V_O \quad ②$$

solving: ① → ②

$\therefore V_0^2 - \frac{41}{5} V_0 + 1 = 0$

using quadratic formula: $V_0 = 8.076V$ and $0.1238V$

which V_0 is correct and why?

$V_0 = 0.1238\,V$

check triode region of operation: $V_{GS} - V_{TN} \geq V_{DS} \geq 0$

$V_{GS} - V_{TN} = 5 - 1 = 4V$

$V_{DS} = V_0 = 0.1238V$

$\therefore$ M1 is in Triode

Look at the truth table

V_{in}	V_0
0V	+5V
+5V	0.1238 V

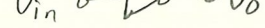
Lets define: $V =$ "1" for $4.5V \leq V \leq 5V$

and $V =$ "0" for $0 \leq V \leq 0.5V$

$\therefore$ truth table is

V_{in}	V_0
0	1
1	0

Inverter Logic Gate



$$I_D = \frac{V_{DD} - V_0}{R_D} = \frac{5 - 0.1238}{10{,}000} = 0.488\,mA$$