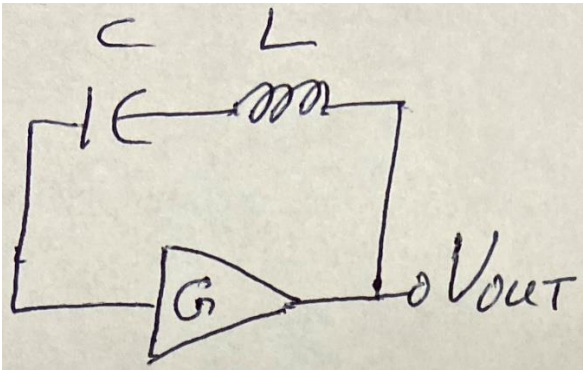
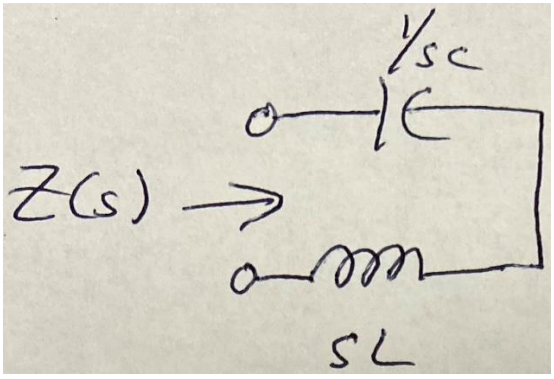
Lecture 9/21/22

## Capacitive Sensing

1. Capacitor Interface Circuitry: LC Oscillators



and



Assume that $G = 1|\underline{0^o}$ .

G is the amplifier gain.

$Z(s) = \frac{1}{sC} + sL \rightarrow Z(j\omega) = \frac{-j}{\omega C} + j\omega L$

At $\omega = \frac{1}{\sqrt{LC}} \rightarrow Z(j\omega) = 0|\underline{0^o}$, i.e. a short, allowing the circuit to oscillate at this frequency.

So, $\omega_n = \frac{1}{\sqrt{LC}}$ : assume L is fixed and C is our sensor.

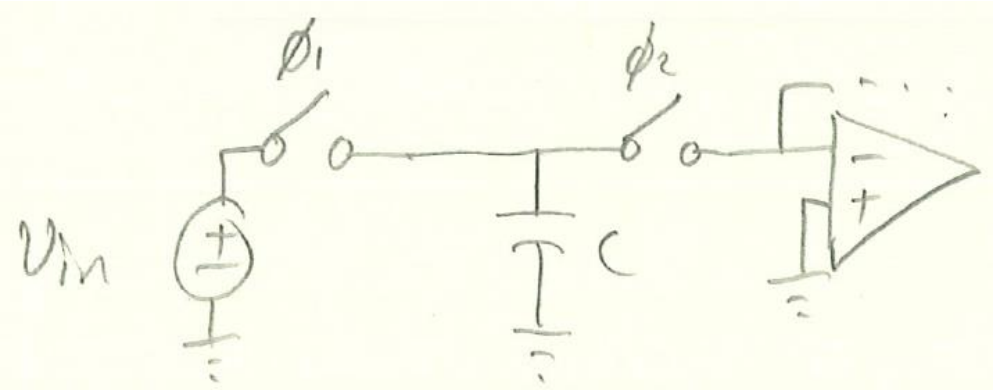
The output, $V_{OUT}$, is a sinusoidal signal where $f \propto \frac{1}{\sqrt{C}}$ : the frequency is a nonlinear function of C(t) or C(x).

This is the common operation of LC oscillators.

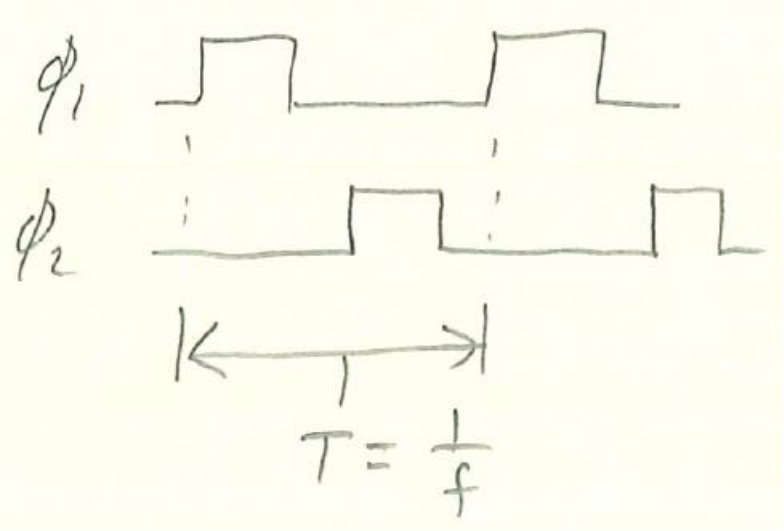
## 2. Capacitor Interface Circuity: Switched-Capacitor Circuits

Switching a capacitor on and off can make it behave like a resistor, under certain conditions.

Consider:



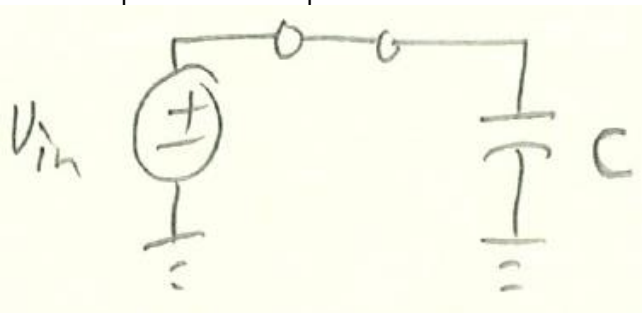

$\phi_1$ and $\phi_2$ are clocked waveforms that turn on and off the two switches: "1" = closed or a short, "0" = open or infinite resistance:




Both switches can be off at the same time, but never both on at the same time. They both operate at the same frequency, f, with period T = 1/f.

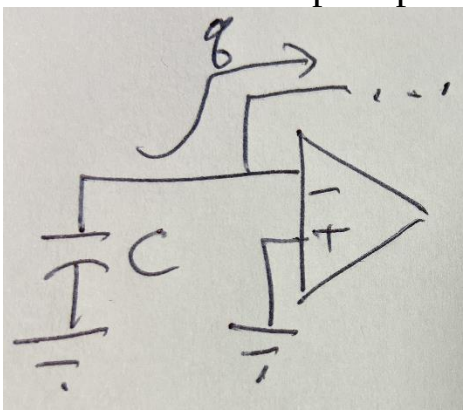
The rest of the op amp circuit (feedback network, etc.) is not shown. The $\phi_2$ switch is connected to a virtual ground through the op amp circuit.

When $\phi_1 = 1$ and $\phi_2 = 0$:




Charge, q, is stored on C: $q = Cv_{in}$.

Next, when $\phi_1 = 0$ and $\phi_2 = 1$, q is transferred through the virtual ground to the rest of the op amp circuit, fully discharging C:




For a given T, q charge moves through the circuit. Therefore, we can model this as:

$$i = \frac{dq}{dt} \approx \frac{\Delta q}{\Delta t} = \frac{q}{T} = \frac{Cv_{in}}{T} = Cfv_{in}$$

The current, i, is proportional to $v_{in}$. Therefore, we can define an equivalent resistance, $R_{eq}$:

$$R_{eq} = \frac{v_{in}}{i} = \frac{1}{Cf}$$

This is called a switched-capacitor resistor.

It is applicable to low-pass systems where f >> system bandwidth.

A LPF can be added at the circuit output to attenuate switching noise.

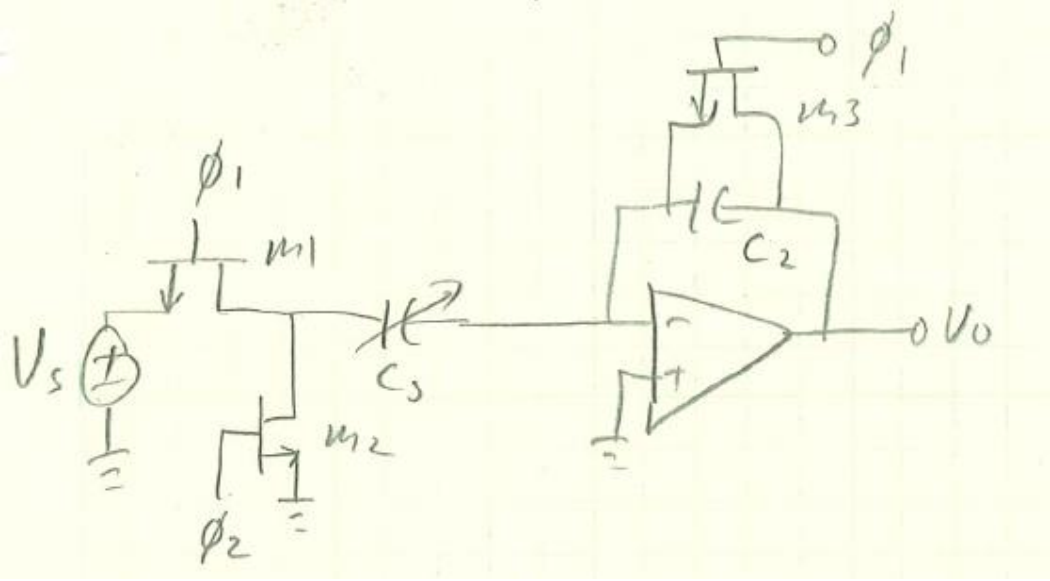
It can be used as a frequency tunable resistor.

In CMOS analog ICs, it's often used for resistors because on-chip capacitors have much tighter fabrication tolerances than on-chip resistors, particularly for audio signal processing applications:

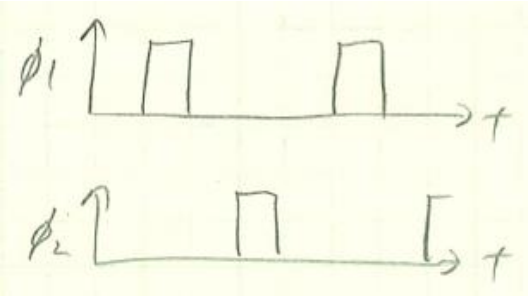
For a 20 kHz BW → use f ~ 200 kHz

MOSFETS (single of paired) are typically used as the switches.

Consider a capacitive sensor application:

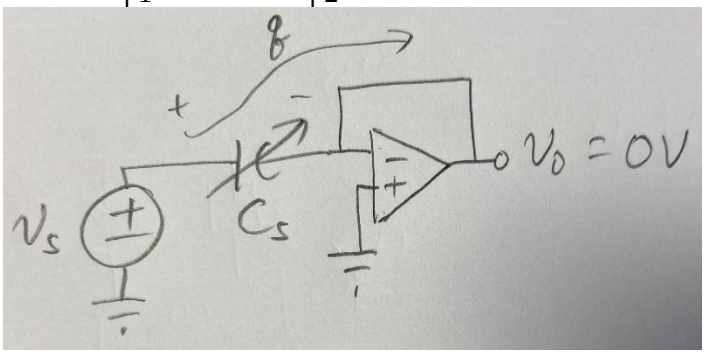



M1, M2, and M3 are MOSFET analog switches. $C_s$ is the sensor.



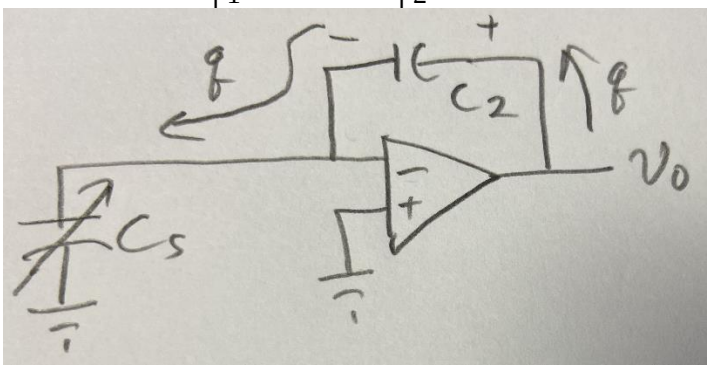

non-overlapping clock waveforms

When $\phi_1 = 1$ and $\phi_2 = 0$:




Charge $q = C_s v_s$ is stored on $C_s$.

Then when $\phi_1 = 0$ and $\phi_2 = 1$:




Charge q flows out of $C_s$ to ground, requiring q to flow through $C_2$:

$v_o = \frac{q}{C_2} = \frac{C_s v_s}{C_2}$ $\rightarrow \phi_2 = 1$ and $\phi_1 = 0$. However, $v_o = 0$ V otherwise.

Assuming that $\phi_2$ has a 50% duty cycle, averaged over time: $v_o \approx \frac{C_s v_s}{2C_2}$.

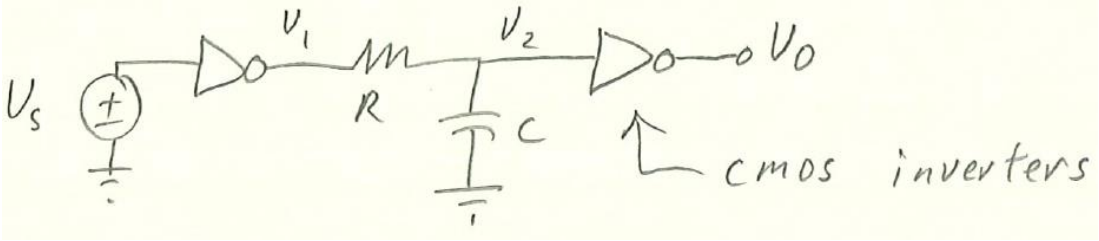
But, if you only measure $v_o$ when $\phi_2 = 1$, then use $v_o = \frac{C_s v_s}{C_2}$.

With fixed $v_s$ and $C_2$, $C_s$ is converted to a voltage, $v_o$, proportional to it.

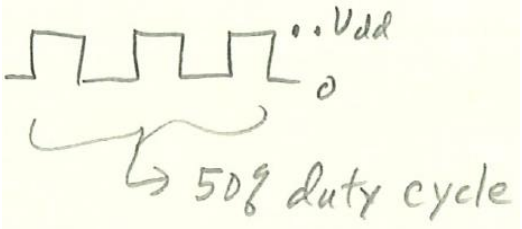
Therefore, this circuit is called a charge amplifier, and has a gain of $v_s/C_2$.

3. Capacitor Interface Circuity: Phase or State Delay Circuits

Consider this circuit:




Let $V_s$ be a pulse train:




$V_{tr} = \frac{V_{dd}}{2}$ → inverter trip voltage

$V_2 = V_1(1 - e^{-t/RC})$

Solve for t = f(RC) for $V_1 = V_{dd}$ and $V_2 = V_{tr}$

Therefore, $\frac{V_{dd}}{2} = V_{dd}(1 - e^{-t/RC})$

Or: $\frac{1}{2} = 1 - e^{-t/RC}$

Or: $e^{-t/RC} = \frac{1}{2}$

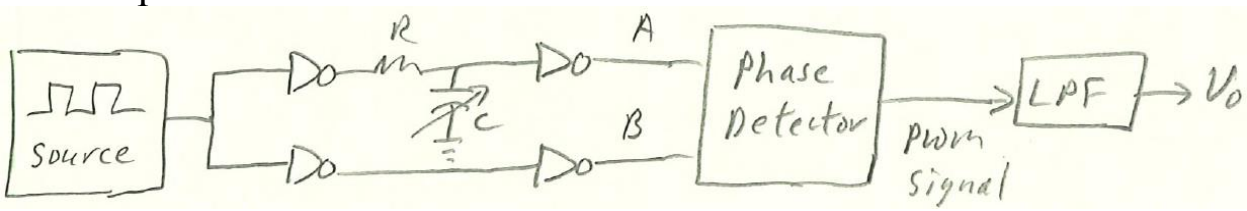
Leading to: $t = -RC \ln(0.5) = 0.693RC$

The last inverter squares up the signal out of the RC subcircuit.

Therefore, the pulse train is delayed 0.693RC s through the RC subcircuit.

Note: this assumes that C fully charges to $V_{dd}$ or discharges to 0 V before the next state change → otherwise the delay is not a linear function of C.

Let's expand the circuit to this:




Now there are two parallel inverter paths, one with $RC_s$ and one without.

$RC_s$ delays signal A compared to signal B.

The Phase Detector compares the logical signals, A and B, and produces a pulse width modulated (PWM) output signal.

Consider the Exclusive OR (EXOR) gate:

| A | B | Q |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

} only high when $A \neq B$

Therefore, pulse width (and duty cycle) is proportional to how out of phase A and B are ($0^o$ to $180^o$).

In phase: Q = 0

$180^o$ out of phase: Q = 1

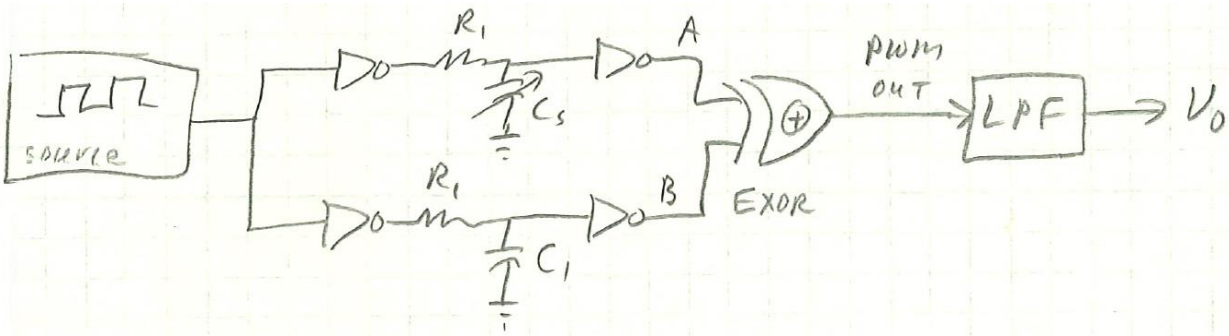
The average or DC value of the PWM signal is proportional to the PWM duty cycle, which is proportional to $C_s$. The low pass filter (LPF) produces $V_o$, which primarily consists of this DC term, which is proportional to $C_s$.

To optimize this capacitive sensor interface circuit:

(1) For the EXOR phase detector: we do not want a phase difference near $0^o$ or $180^o$ to avoid phase jitter issues.

(2) To avoid excessive nonlinear distortion, limit the phase delay range from the sensor to $45^o$, and place that about $90^o$ ($67.5^o$ to $112.5^o$).

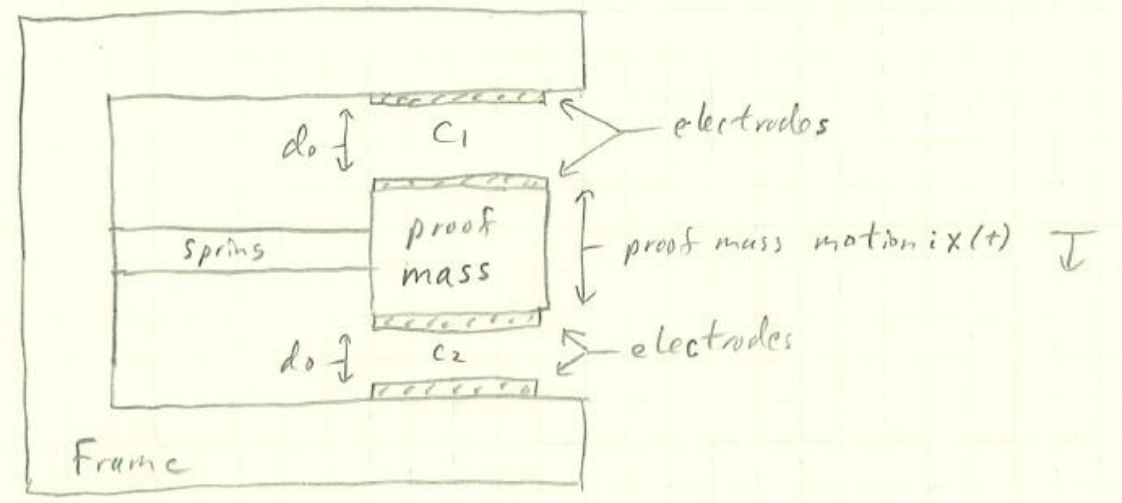
(3) Add a fixed RC delay stage in the lower inverter chain to achieve this:




Signal A's minimum delay differs from signal B by $67.5^o$, and signal A's maximum delay differs from signal B by $112.5^o$. One of the two resistors can be potentiometer so that the interface circuit can be tuned.

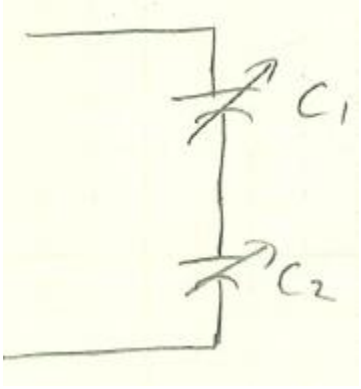
4. Capacitor Interface Circuity: AC Voltage Division

Sometimes the MEMS device is designed to produce a differential capacitance:

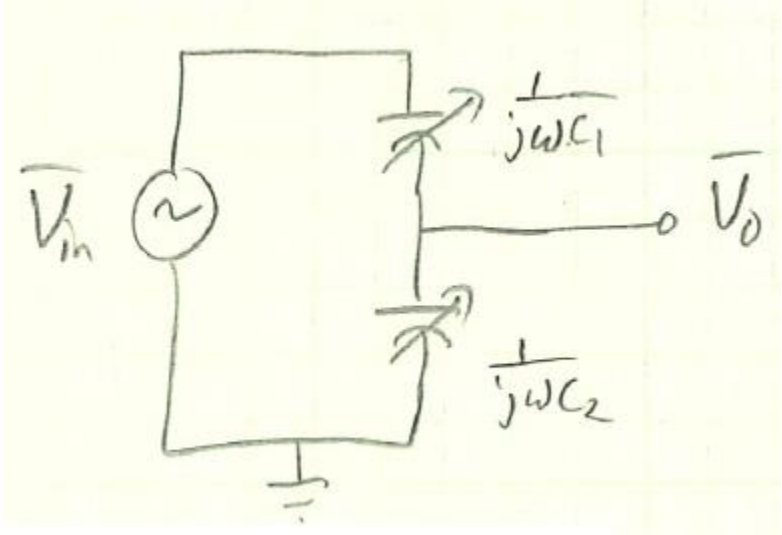



$$C_1 = \frac{\varepsilon_o \varepsilon_r A}{d_1} = \frac{\varepsilon_o \varepsilon_r A}{d_o + x(t)} \quad \text{and} \quad C_2 = \frac{\varepsilon_o \varepsilon_r A}{d_2} = \frac{\varepsilon_o \varepsilon_r A}{d_o - x(t)}$$

The circuit model is:




Consider the application of an AC voltage, $\bar{V}_{in}$:



$\frac{\bar{V}_o}{\bar{V}_{in}} = \frac{\frac{1}{j\omega C_2}}{\frac{1}{j\omega C_1}+\frac{1}{j\omega C_2}} = \frac{\frac{1}{C_2}}{\frac{1}{C_1}+\frac{1}{C_2}} = \frac{C_1}{C_2+C_1}$ → An AC voltage divider

Let $\bar{V}_{in} = V_1 \sin(\omega t)$

Therefore: $\bar{V}_o = V_1 \sin(\omega t)\left[\frac{C_1}{C_2+C_1}\right]$ → select ω >> $\omega_{MEMS}$

$$\frac{C_1}{C_2+C_1} = \frac{\frac{\varepsilon_o \varepsilon_r A}{d_o+x(t)}}{\frac{\varepsilon_o \varepsilon_r A}{d_o-x(t)}+\frac{\varepsilon_o \varepsilon_r A}{d_o+x(t)}}$$

$$= \frac{\frac{1}{d_o+x(t)}}{\frac{1}{d_o-x(t)}+\frac{1}{d_o+x(t)}}$$

$$= \frac{d_o-x(t)}{d_o+x(t)+d_o-x(t)}$$

$$= \frac{d_o-x(t)}{2d_o}$$

$$= 0.5\left(1-\frac{x(t)}{d_o}\right)$$

$$\therefore\ \bar{V}_o(t) = V_1 \sin(\omega t)\left[0.5\left(1-\frac{x(t)}{d_o}\right)\right]$$

The amplitude of $\bar{V}_o(t)$ is a linear function of x(t).

So, we need a way to recover the amplitude of $\bar{V}_o(t)$ …