1) "MOSFET" → Metal Oxide Semiconductor Field Effect Transistor

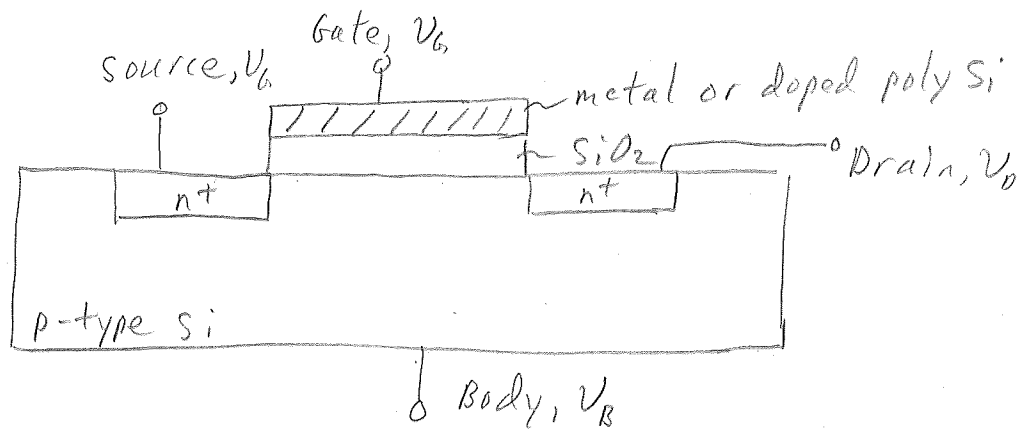
n-type and p-type MOSFETs

n-type: n-type source and drain in p-type substrate

p-type: p-type " " " " n-type "

a. Discussion on n-type MOSFET

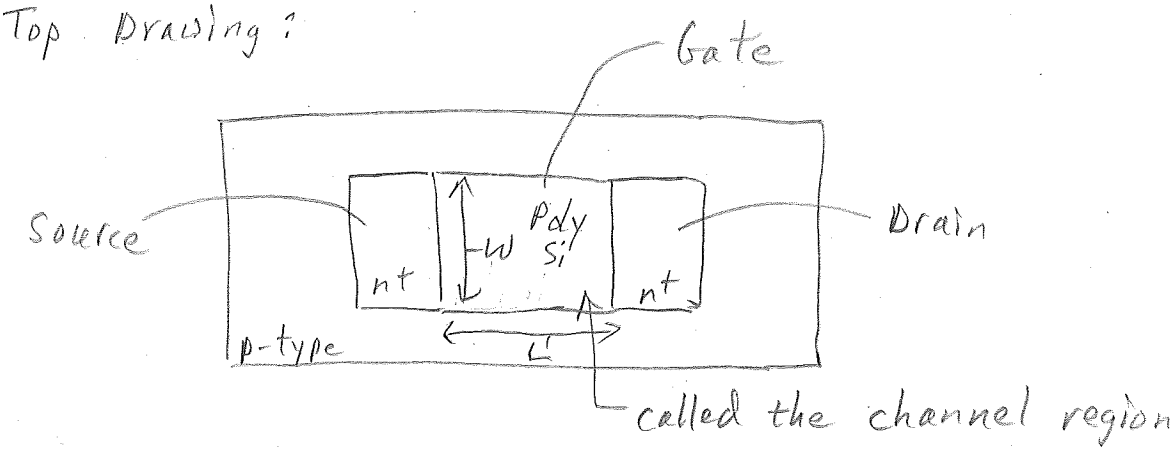
Cross-sectional Drawing:



note: metal contacts on source and drain not shown

$V_B \leq V_S$ and $V_D \geq V_S$

Top Drawing:



The channel region is defined by W and L. The designer defines W and L to taylor the MOSFET's characteristics. $\frac{W}{L}$ is an important MOSFET parameter

In this MOSFET device, applying v_{GS} enhances the conductivity of the channel → ∴ these are called Enhancement-Mode MOSFETs

Later, we will discuss Depletion-mode MOSFETs

Since the MOSFET is based on the MOS capacitor, i_G and i_B are 0A → DC currents

<u>Note</u>: AC currents will flow through a capacitor

$Z(j\omega) = \frac{1}{j\omega C}$ for a capacitor

∴ the current of interest is the current from Drain to Source, referred to as i_D

3 primary modes of operation

① Off

when $v_{GS} - V_{TN} < 0V$: $i_D = 0A$

② Linear or Triode Region of operation

$v_{GS} - V_{TN} \geq 0$ and $v_{GS} - V_{TN} \geq v_{DS}$

$$i_D = K_n' \frac{W}{L}\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right) v_{DS}$$

$$K_n' = \mu_n C_{ox}'' = \mu_n \frac{\varepsilon_{ox}}{T_{ox}} = \frac{\varepsilon_0 \varepsilon_r}{T_{ox}}$$

for Si, $\varepsilon_r = 3.9$

$\varepsilon_0 = 8.854\ pF/m$

μ_n = electron mobility

C_{ox}'' = oxide capacitance per unit area, in F/cm^2

$K_n = K_n' \frac{W}{L}$

K_n and K_n' → called transconductance parameters

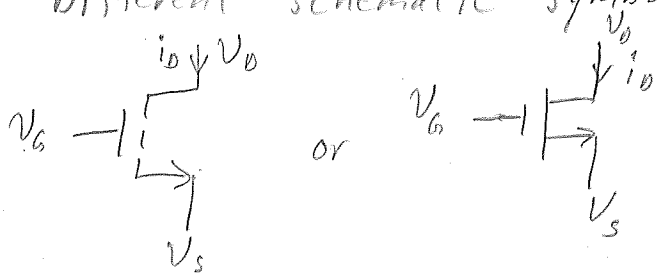
$[K_n] = [K_n'] = A/V^2$

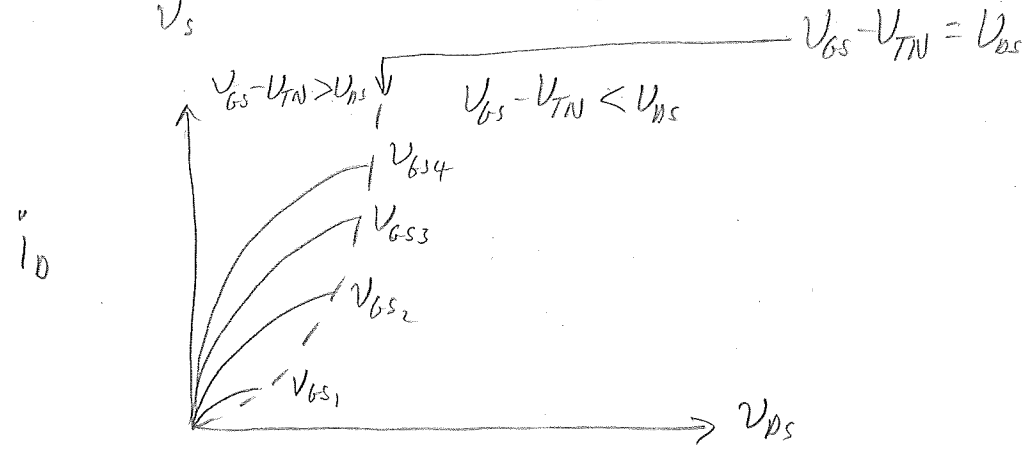
For $i_D = K_n (v_{GS} - V_{TN} - \frac{v_{DS}}{2}) v_{DS} = K_n' \frac{W}{L} (v_{GS} - V_{TN} - \frac{v_{DS}}{2}) v_{DS}$

→ The Designer gets to define $\frac{W}{L}$ in the design

Since v_B is often shorted to v_S → effectively 3 terminals in the NMOS Transistor: v_G, v_S, v_D

Different schematic symbols:





Plot of i_D vs. v_{DS} for different values of v_{GS} where $v_{GS4} > v_{GS3} > v_{GS2} > v_{GS1}$

ex: $v_{GS1} = 2V$, $v_{GS2} = 3V$, $v_{GS3} = 4V$, $v_{GS4} = 5V$ and $V_{TN} = 1V$

Typical value for $K_n = 25 \times 10^{-6} A/V^2$

③ Saturation or Pinch-Off Region

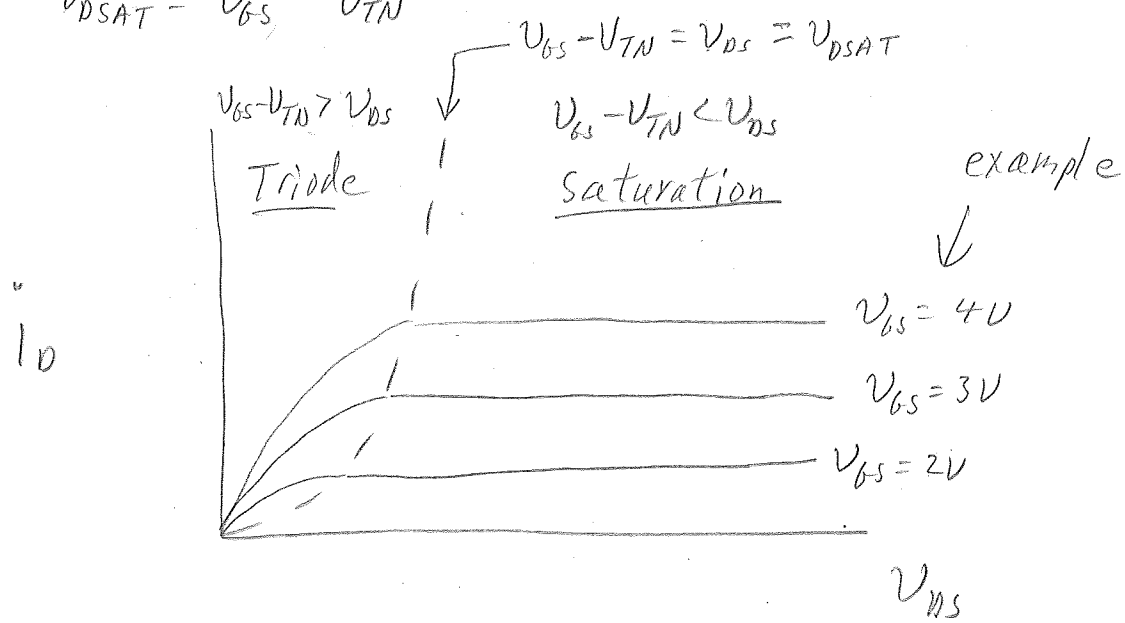
$v_{GS} - V_{TN} \geq 0$ and $v_{DS} \geq v_{GS} - V_{TN}$

→ by further increasing v_{DS} beyond the Triode Region, it "no longer" increases i_D

→ $i_D = \frac{K_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2$ → square law response

The channel is said to be "pinched-off"

$v_{DSAT} = v_{GS} - V_{TN}$



Triode Region: $i_D = f(v_{DS}$ and $v_{GS})$
Saturation : $i_D = f(v_{GS})$
} 1st order model for nMOS

<u>Region usage</u>

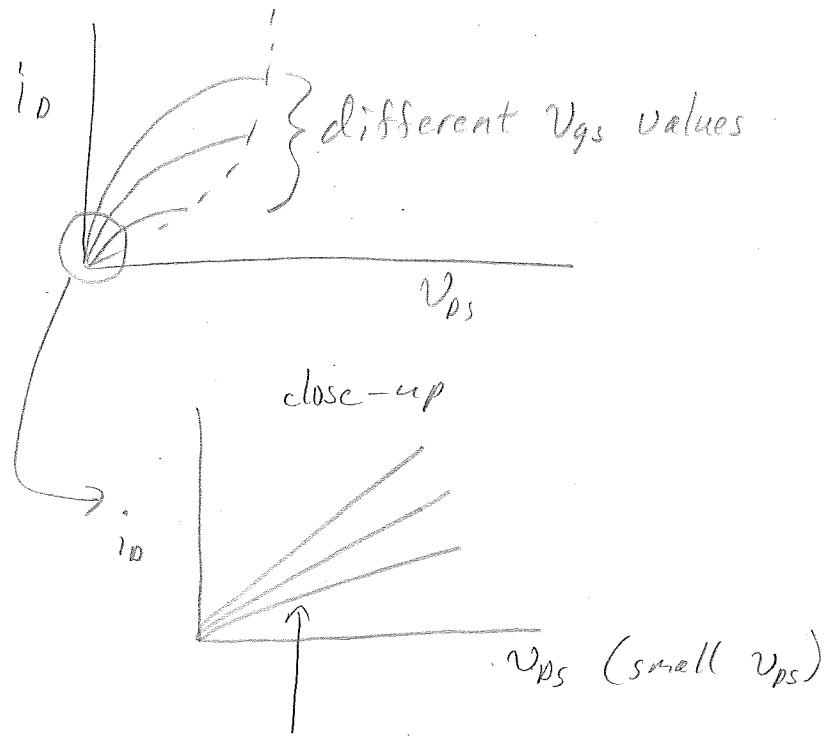
Triode → voltage controlled resistor, digital logic, analog switch

Saturation → amplifier

2. <u>More on Triode Region of operation</u>

→ "Triode" name → from similar operation to the triode vacuum tube

→ Also called the "Linear Region"



nearly linear inc in i_D w/ v_{DS} inc

∴ For small v_{DS} ($\frac{V_{DS}}{2} << v_{GS} - V_{TN}$)

→ $i_D \cong K_n'\left(\frac{W}{L}\right)(v_{gs} - V_{TN})\, v_{DS}$

∴ define $R_{on} = \left[\frac{\partial i_D}{\partial V_{DS}}\right]^{-1}_{v_{DS}\to 0} = \frac{1}{K_n'\left(\frac{W}{L}\right)(V_{GS} - V_{TN})}$

notice that as $v_{GS} \uparrow$: $R_{on} \downarrow$

→ The nMOS transistor can be used as a voltage controlled resistor, or as a resistive load by fixing v_{GS}

3. <u>Transconductance</u> : g_m

→ relates change in drain current to change in v_{GS} about the Q-point

→ useful in small-signal linear circuit model for MOSFET circuits

def: $g_m = \left.\dfrac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}}$ → note error in book, eq 4.17 p. 153

<u>Triode Region</u>

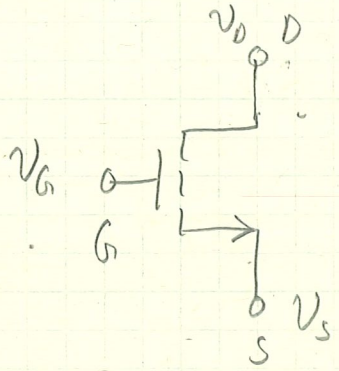
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = \left.\frac{\partial\left(K_n\left(v_{GS} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS}\right)}{\partial v_{GS}}\right|_{Q\text{-point}} = K_n \overset{\text{DC value}}{V_{DS}}$$

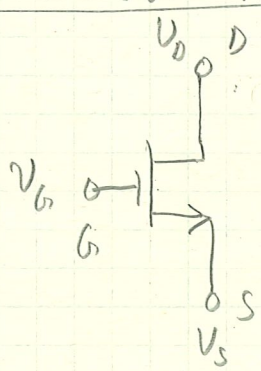
<u>Saturation Region</u>

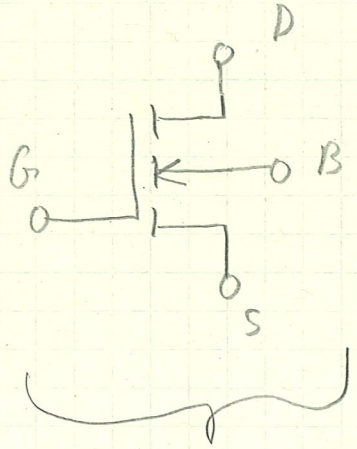
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{-point}} = \left.\frac{\partial\left(\frac{1}{2}K_n(V_{GS} - V_{TN})^2\right)}{\partial v_{GS}}\right|_{Q\text{-point}} = K_n(\overset{\text{DC value}}{V_{GS}} - V_{TN})$$

Since v_{gs} is often a small signal input voltage and i_d is the small signal output signal, g_m represents a measure of the signal gain possible with the transistor circuit.

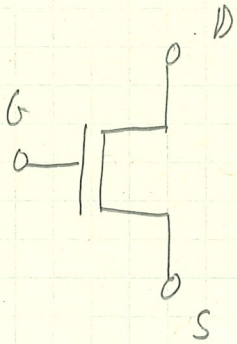
4) More schematic symbols for NMOS Transistors







here, the Body contact may or may not be tied to the Source



← Note: the circuit identifies S & D