Chapter 4 : Field-Effect Transistors (FETs)

1) Introduction

→ Begin our discussion on Transistors

from www : "Transistor" → from "Transconductance" or "Transfer" "Varistor" "Resistor" Show next page now →

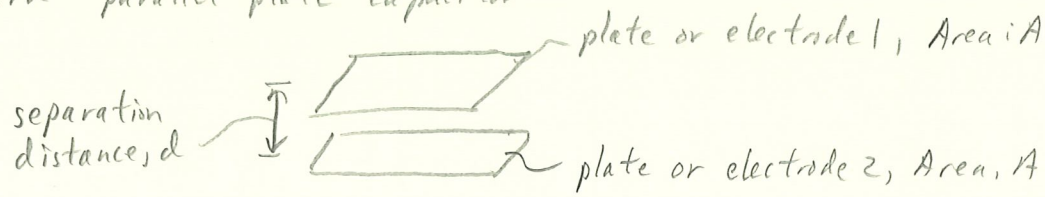
FETs → metal-oxide-semiconductor FETs (MOSFETs)

→ junction FETs (JFETs)

* Most of our discussion will be on MOSFETs

2) MOS Capacitor

a) standard parallel plate capacitor

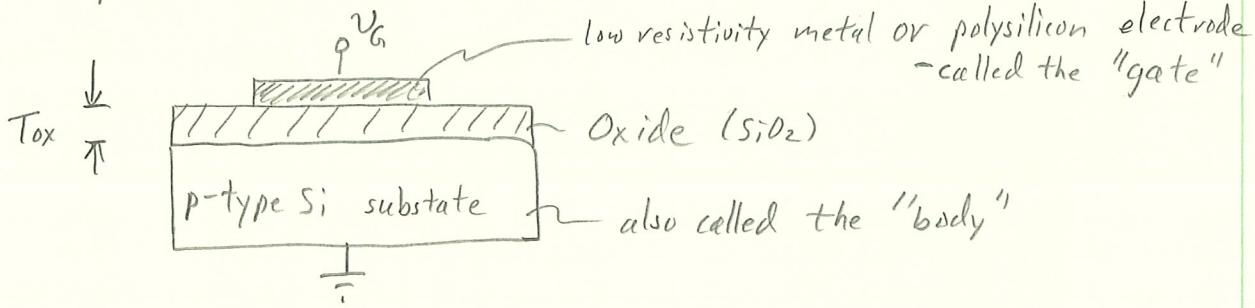


Insulating (dielectric) material in between the plates with relative permittivity ε_r, air/vacuum: $\varepsilon_r \approx 1$, SiO_2: $\varepsilon_r = 3.7$

$$\text{Capacitance} = C = \frac{\varepsilon_0 \varepsilon_r A}{d}, \quad \varepsilon_0 = \text{permittivity of free space} = 8.854 \text{ pF/m}$$

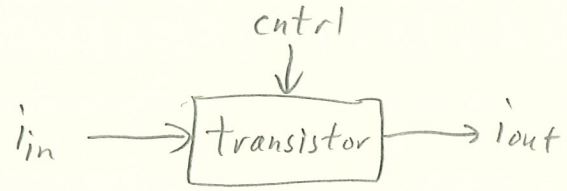
for $A \gg d^2$

b. MOS capacitor structure

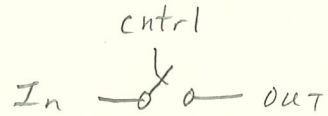


Semiconductor substrate → 2nd electrode

Transistor → basically a 3 terminal device

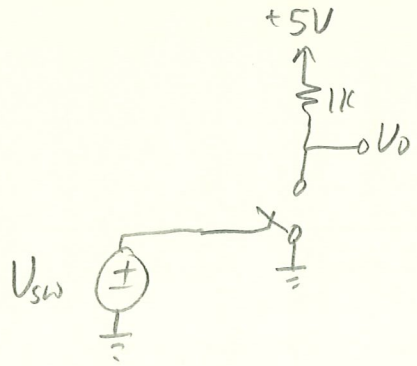


This course → Digital Electronics → mostly use transistor as a switch

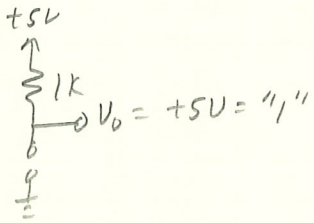


ex: Cntrl = 5V = "1" → switch closed → short circuit

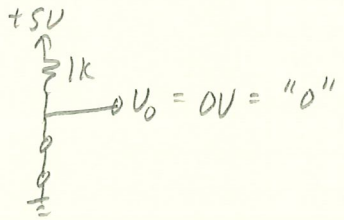
Cntrl = 0V = "0" → switch open → open circuit



if $V_{sw} = 0V$ →



if $V_{sw} = 5V$ →



Truth Table

V_{sw}	V_o
0	1
1	0

→ Inverter Logic Gate

Lets discuss how transistors operate

semiconductor substate → substantial resistivity with a limited supply of e^-'s and holes

Since the substate can be depleted of carriers, capacitance is a nonlinear function of voltage, v_G

∴ 3 different operation regions as $f(v_G)$

(1) Accumulation

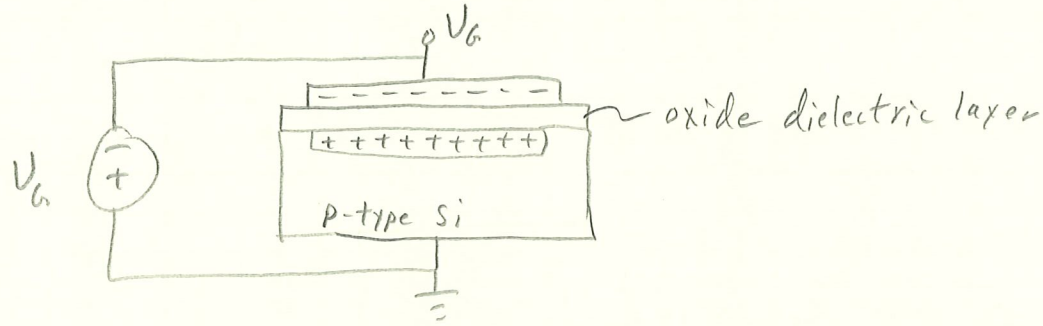
(2) Depletion

(3) Inversion

① <u>Accumulation Region</u>

Definition : $V_{TN} \equiv$ Threshold Voltage

Accumulation Region : $V_G \ll V_{TN}$ and $V_G < 0V$

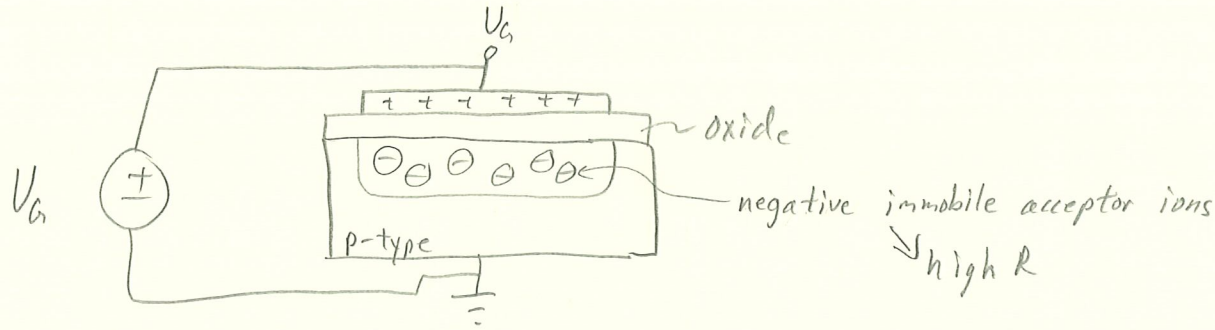


large negative charge on metallic gate balanced by a thin layer of positively charged holes in the p-type Si directly under the SiO_2 under the gate metallization

The hole density at the surface exceeds that of the original p-type substrate → the surface is said to be in accumulation or in the accumulation region

② Depletion Region

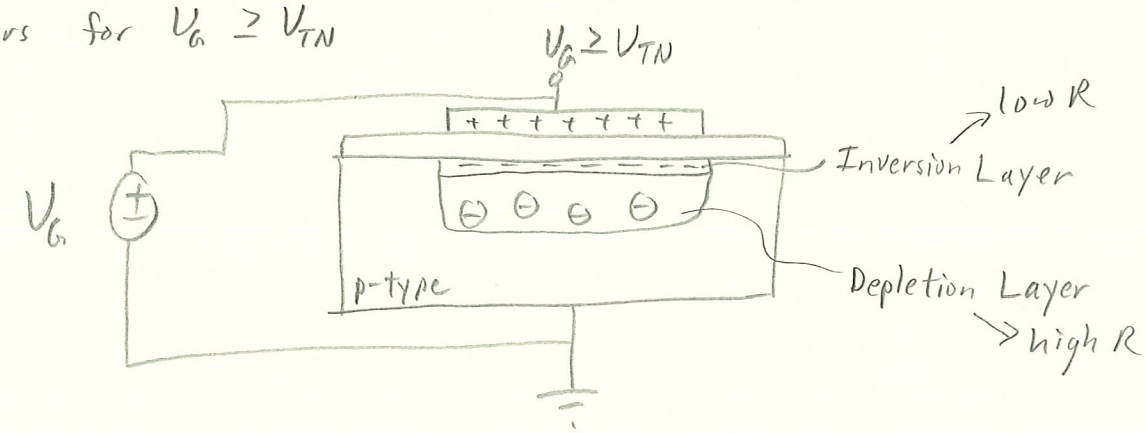
slowly increase V_G, but $V_G < V_{TN}$



As V_G is increased, holes are repelled in the semiconductor beneath the gate electrode, leaving the negative immobile acceptor ions. It is ∴ depleted of free carriers → hence it is called the Depletion Region

③ Inversion Region

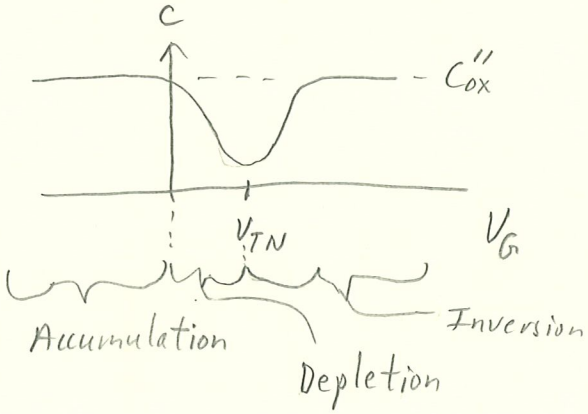
V_G is further increased, attracting electrons to the semiconductor area under the gate electrode. At some point, the e^- density at the surface exceeds the hole density. Then the p-type Si layer has "inverted" to an n-type inversion layer or region directly under the gate electrode → thin layer. This occurs for $V_G \geq V_{TN}$



Very important in understanding how FETs work

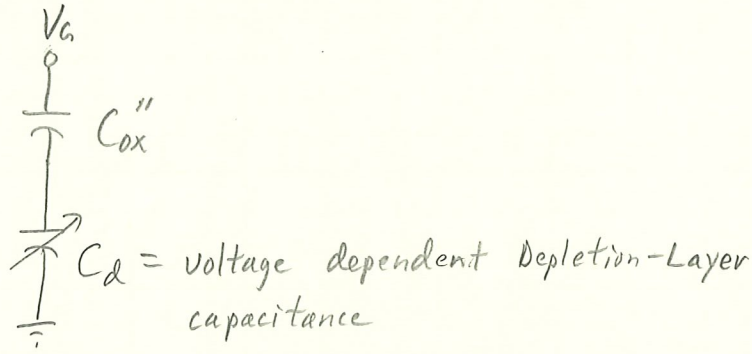
④ Effects on Capacitance

→ The Depletion Region increases the effective electrode separation distance, while the Inversion Region reduces it back to the oxide thickness



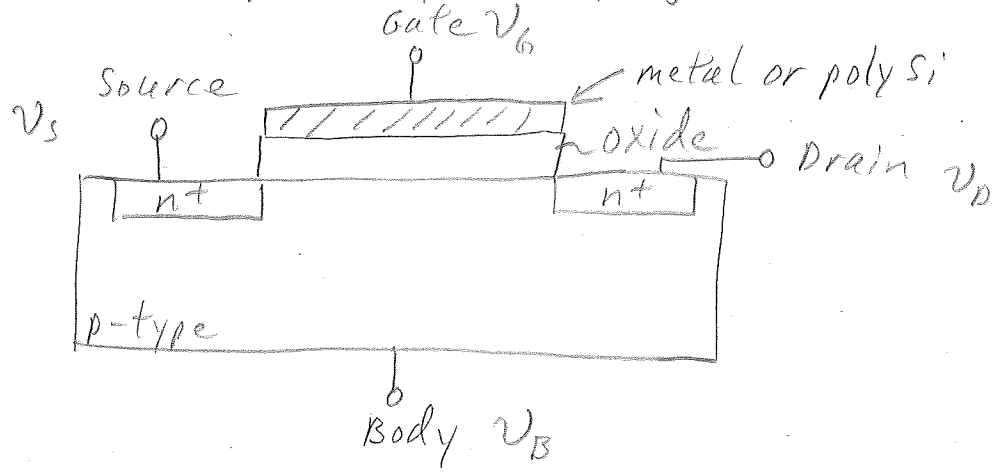
C_{ox}'' → capacitance between gate electrode and substrate due to oxide layer dielectric

Capacitance Model:



<u>Note</u>: The MOS capacitor can be used as an ionizing radiation sensor. The radiation results in charge being trapped in the SiO_2 layer, which changes V_{TN}. The MOS capacitor ∴ records the radiation event.

Add 2 terminals in the p-type substrate at the ends of the gate by n^+ doping these regions



4 voltages: v_S, v_G, v_D, v_B

make $v_B \leq v_S$ after $v_B = v_S$ → keep p-type : n^+ pn junction reverse biased

$v_{GS} = v_G - v_S$, $v_{DS} = v_D - v_S$

For $v_{GS} \geq V_{TN}$ → Inversion Region

and $v_{DS} > 0$ → current flows through inversion layer from drain to source