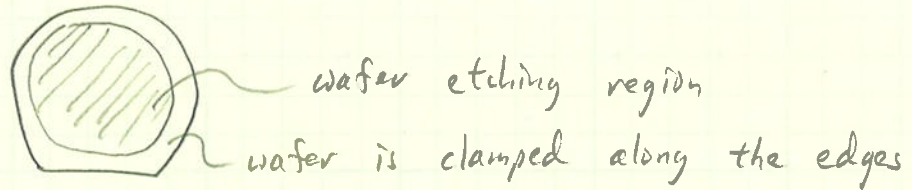
1) DRIE Design Constraints

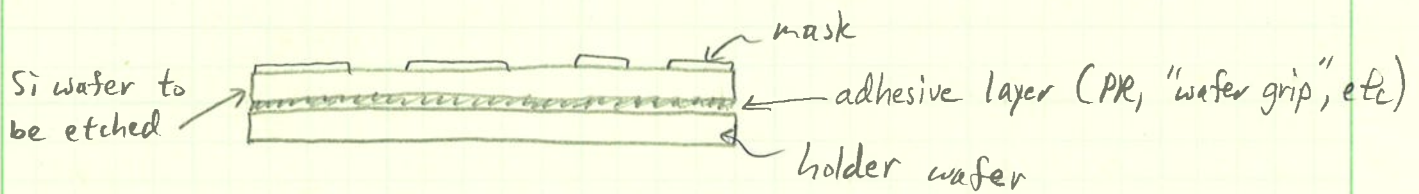
① Confine regions to be etched to the interior of the wafer →



→ wafer may not etch correctly at the edge

→ wafer could break in the etcher → bad

② Cannot etch all the way through the wafer unless it is mounted on a "holder wafer" with an adhesive material that is a sufficient conductor of heat



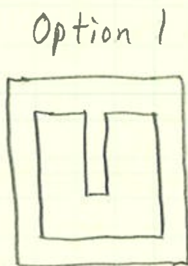
③ Minimize the surface area on the wafer to be etched

→ better etching uniformity

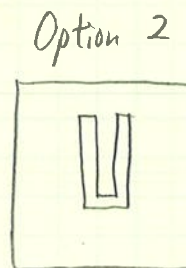
→ faster etching time

ex: desire simple cantilever for motion normal to wafer's surface

Option 1



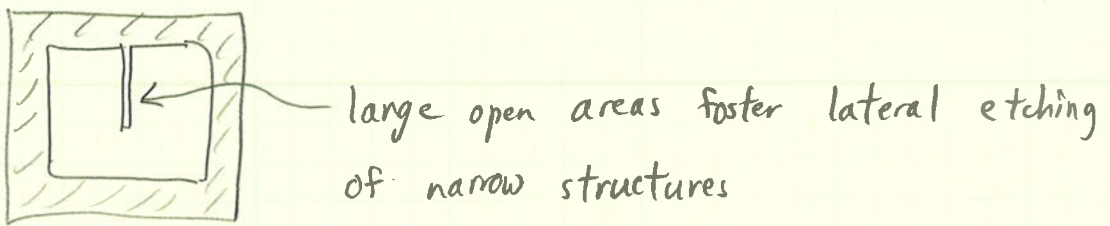
Option 2



← better choice

less bulk Si to remove

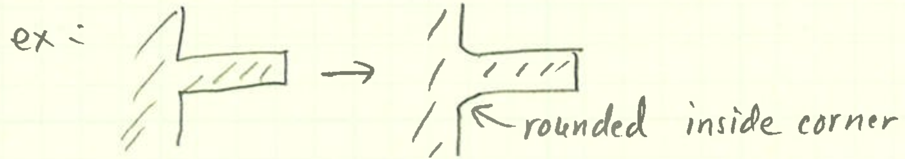
④ Avoid large open areas next to thin features



⑤ Across the wafer, try to use similar size (width) features and open areas → for more uniform etch rate across the wafer

⑥ Check etch progress often to avoid over/under etching
(1) optically
(2) with a <u>profilometer</u>

⑦ round inside corners on high stress members (springs, etc.)

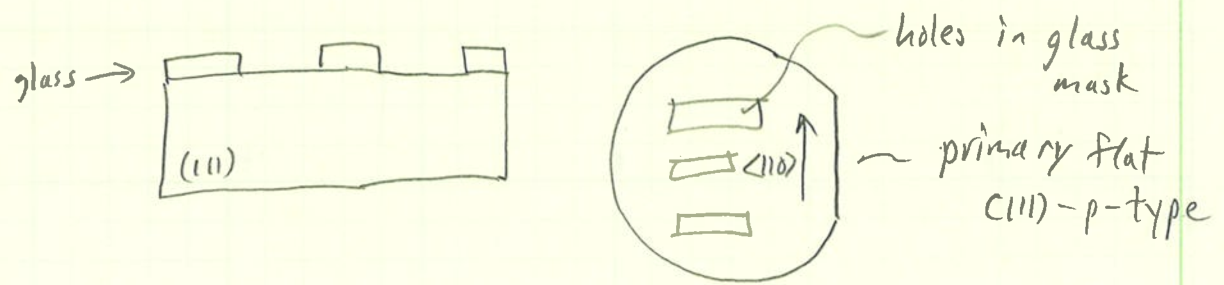
ex:


helps prevent breakage along crystal planes at high stress points

2) <u>Modified and Hybrid Processes</u>
→ several have been developed

a. Consider the BELST process

① start with (111) wafer → thermal oxidation process
→ Photolithography and pattern glass layer (wet or dry etch SiO_2)



use undoped or lightly doped (111) wafer