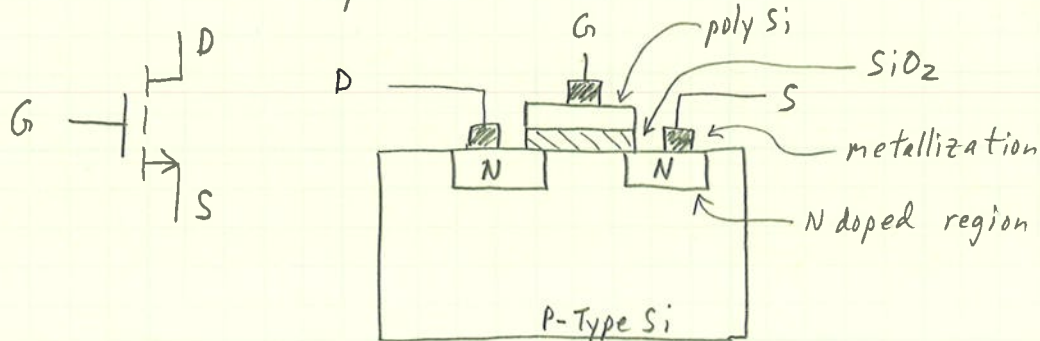


## 1) Intro to MEMS Fabrication

→ first a review of IC microfabrication

→ Consider a simple NMOS transistor



\* Refer to Figure 2.2, p.31 in textbook (old textbook)

Step 1.0 → start with bare Si wafer → thoroughly cleaned

Step 2.0 → layer of SiO<sub>2</sub> grown on both sides of the wafer

2.1 → layer of PR deposited on front side by spin coating

2.2 → PR layer patterned through photolithography → Mask 1

2.3 → exposed SiO<sub>2</sub> is removed (etched)

Step 3.0 → PR mask is chemically removed with organic solvents

3.1 → a layer of Si dopant (N-type or P-type) is deposited.

The patterned SiO<sub>2</sub> serves as a dopant mask.

3.2 → wafer is thermally treated so that the dopant diffuses into the exposed Si.

3.3 → remaining dopant source layer is removed

Step 4.0 → Patterned SiO<sub>2</sub> is removed

4.1 → another SiO<sub>2</sub> layer is grown

4.2 → a PR layer is applied

4.3 → PR layer is patterned with photolithography → Mask 2

4.4 → the SiO<sub>2</sub> layer is patterned using the PR mask

Step 5.0 → Remaining PR mask is removed

5.1 → Using the patterned  $\text{SiO}_2$  as a mask, a thin high quality  $\text{SiO}_2$  layer is grown to form the gate oxide

5.2 → a PR layer is deposited

5.3 → photolithography is performed → Mask 3

5.4 → using the PR mask the gate oxide is selectively etched

Step 6.0 → Remaining PR mask is removed

6.1 → a layer of doped poly Si is deposited

6.2 → a layer of PR is deposited

6.3 → Photolithography is performed → Mask 4

6.4 → using the PR mask, the poly Si layer is patterned, to realize the gate electrode

Step 7.0 → Remaining PR mask is removed

7.1 → a thin layer of metal is deposited

7.2 → a layer of PR is deposited

7.3 → Photolithography → Mask 5

7.4 → using the PR mask, the metal layer is patterned to realize the electrical contacts to S, D and G, and electrical traces

Step 8.0 → Remaining PR is removed

other processes:

Step 9.0 → passivation layer to protect device, PR, photolith (mask 6), patterning

step 10 → dicing, cleaning

step 11 → attach die in package, wire bond, attach lid to package

Typical IC run  $\rightarrow$   $\sim$  3 months and 20 to 40 Masks

2) Intro to Si Micromachining

$\rightarrow$  2 fundamental types of Si micromachining

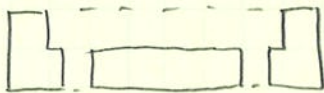
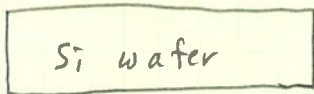
1) Bulk Micromachining

$\rightarrow$  selectively removing "bulk" portions of the Si substrate to realize the MEMS structure or device

2) Surface Micromachining

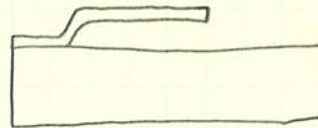
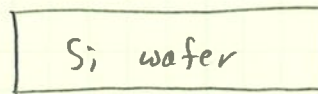
$\rightarrow$  using the Si substrate as a holder, freestanding micromechanical structures are fabricated on the substrate surface through the addition (deposition) and subtraction (etching) of thin films, using sacrificial layers

Bulk Micromachining



Vacuum Manifold

Surface Micromachining



Vibrating Cantilever

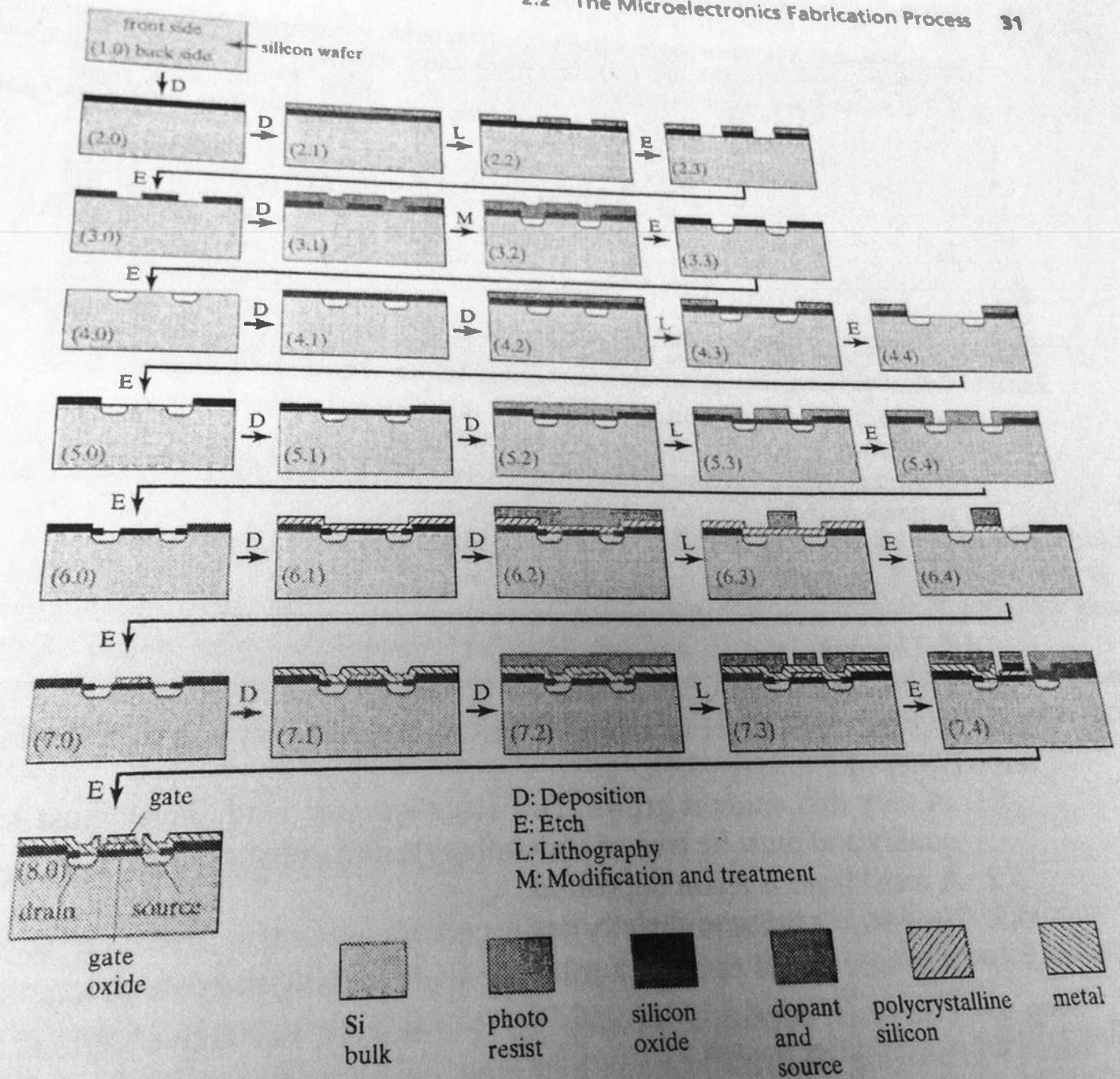


FIGURE 2.2