Thursday 3/23/23

Implementing the logistics map in circuitry

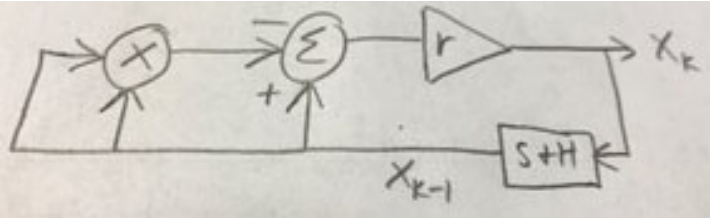
Recall: $x_{k+1} = rx_k(1 - x_k)$

Rewrite as: $x_k = r(x_{k-1} - x_{k-1}^2)$

This is a nonlinear difference equation.

It could be implemented in a simulation tool such as MATLAB, in software on a microcontroller, in digital logic circuitry, or in analog circuitry.

Consider this analog circuit implementation block diagram:



S&H is a Sample-and-Hold circuit.

Consider the Analog Devices AD783 Sample-and-Hold Amplifier chip,

We have already discussed multiplier and summer circuits.

The amplifier gain has a value or r.

In a circuit implementation, noise will be present in the circuit, which will change the output compared to that of a digital simulation. Show simulation results.

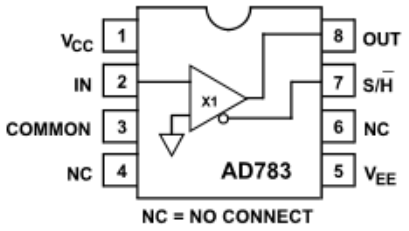
Complete Very High Speed Sample-and-Hold Amplifier

AD783

FEATURES

Acquisition Time to 0.01%: 250 ns Typical
Low Power Dissipation: 95 mW
Low Droop Rate: 0.02 μV/μs
Fully Specified and Tested Hold Mode Distortion
Total Harmonic Distortion: –85 dB
Aperture Jitter: 50 ps Maximum
Internal Hold Capacitor
Self-Correcting Architecture
8-Pin Mini Cerdip and SOIC Packages

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

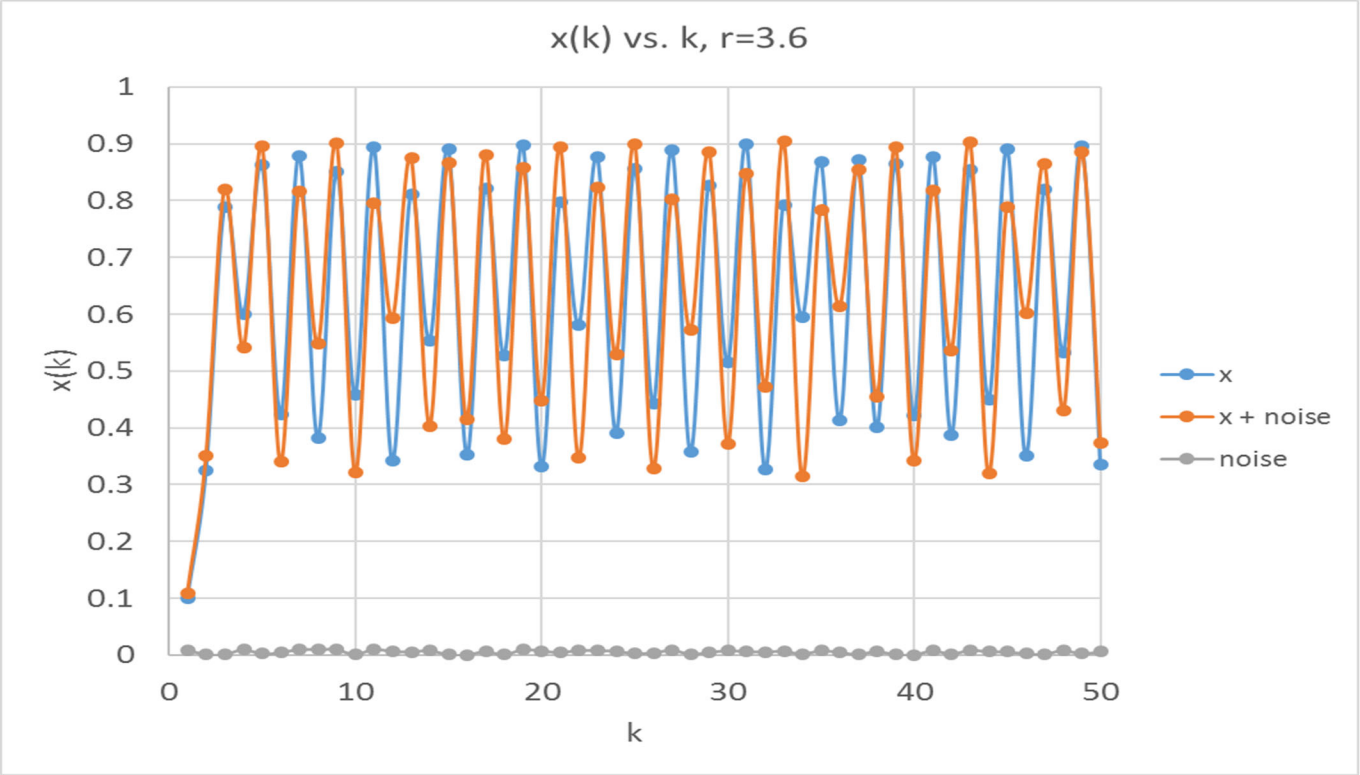
The AD783 is a high speed, monolithic sample-and-hold amplifier (SHA). The AD783 offers a typical acquisition time of 250 ns to 0.01%. The AD783 is specified and tested for hold mode total harmonic distortion with input frequencies up to 100 kHz. The AD783 is configured as a unity gain amplifier and uses a patented self-correcting architecture that minimizes hold mode errors and ensures accuracy over temperature. The AD783 is self-contained and requires no external components or adjustments.

The AD783 retains the held value with a droop rate of 0.02 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD783 ideal for high speed 12- and 14-bit analog-to-digital converters.

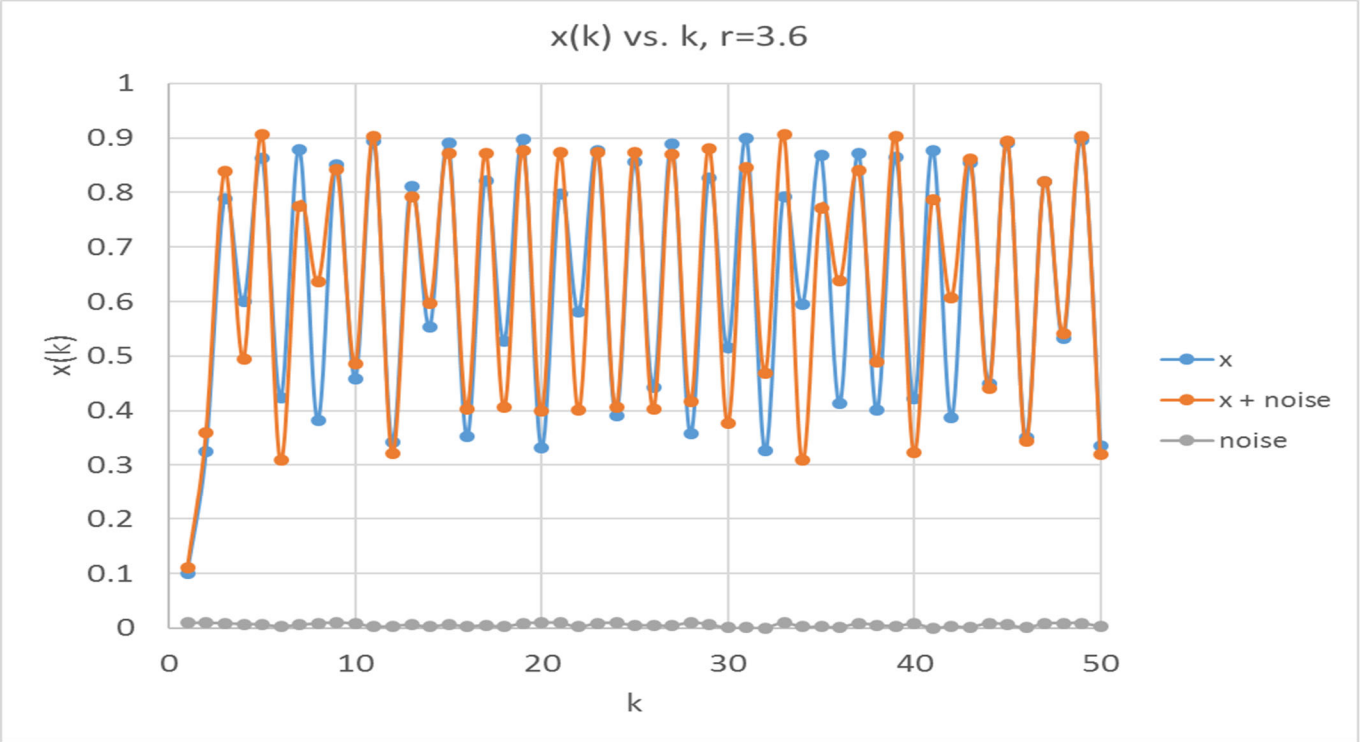
The AD783 is manufactured on Analog Devices' ABCMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

PRODUCT HIGHLIGHTS

1. Fast acquisition time (250 ns), low aperture jitter (20 ps) and fully specified hold mode distortion make the AD783 an ideal SHA for sampling systems.
2. Low droop (0.02 μV/μs) and internally compensated hold mode error result in superior system accuracy.
3. Low power (95 mW typical), complete functionality and small size make the AD783 an ideal choice for a variety of high performance applications.
4. The AD783 requires no external components or adjustments.
5. The AD783 is an excellent choice as a front-end SHA for high speed analog-to-digital converters such as the AD671, AD7586, AD674B, AD774B, AD7572 and AD7672.
6. Fully specified and tested hold mode distortion guarantees the performance of the SHA in sampled data systems.



Run first time

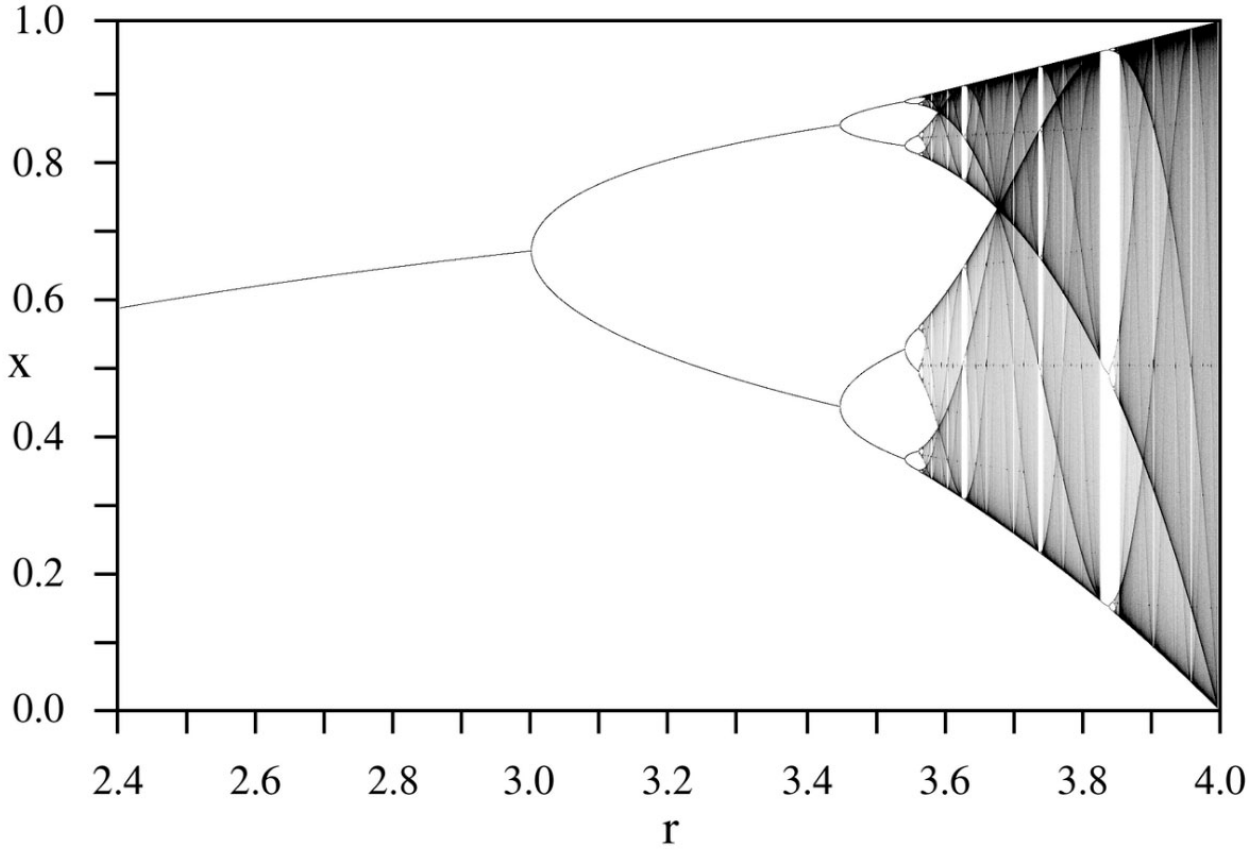


Run second time (only random noise values changed)

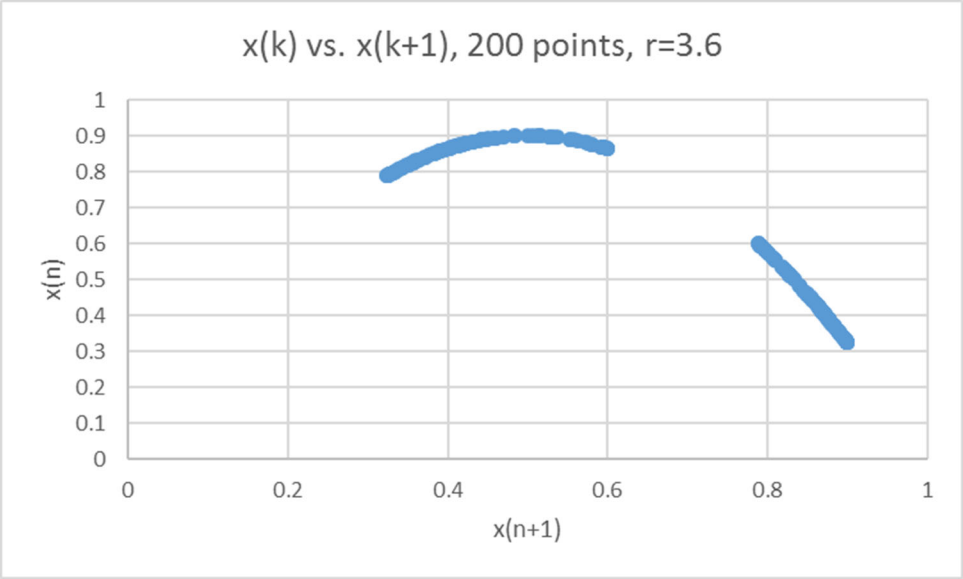
More on the Logistics Map

Recall: $x_{k+1} = r x_k (1 - x_k)$

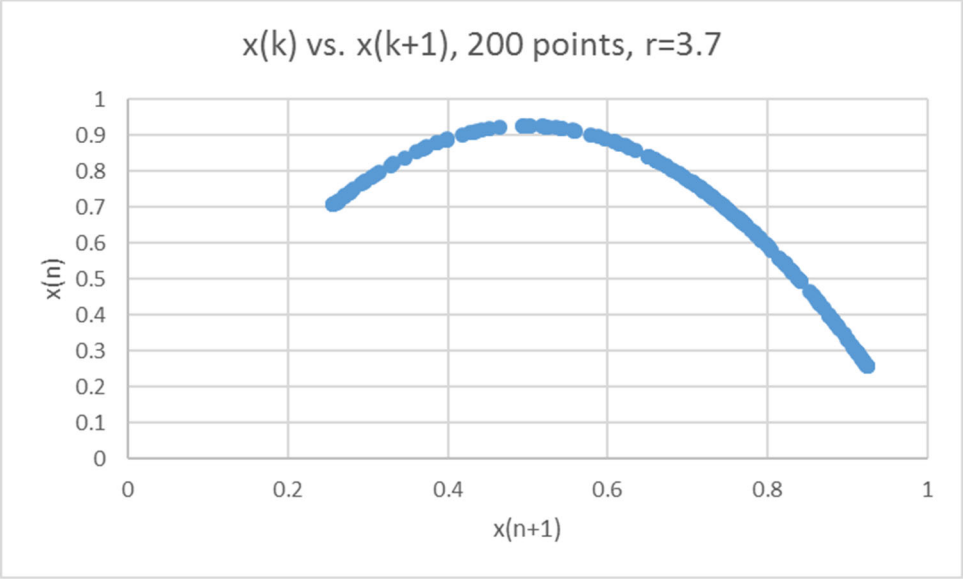
Consider a comparison of the bifurcation diagram with plots of x_k vs. x_{k+1} (phase diagrams for this system)



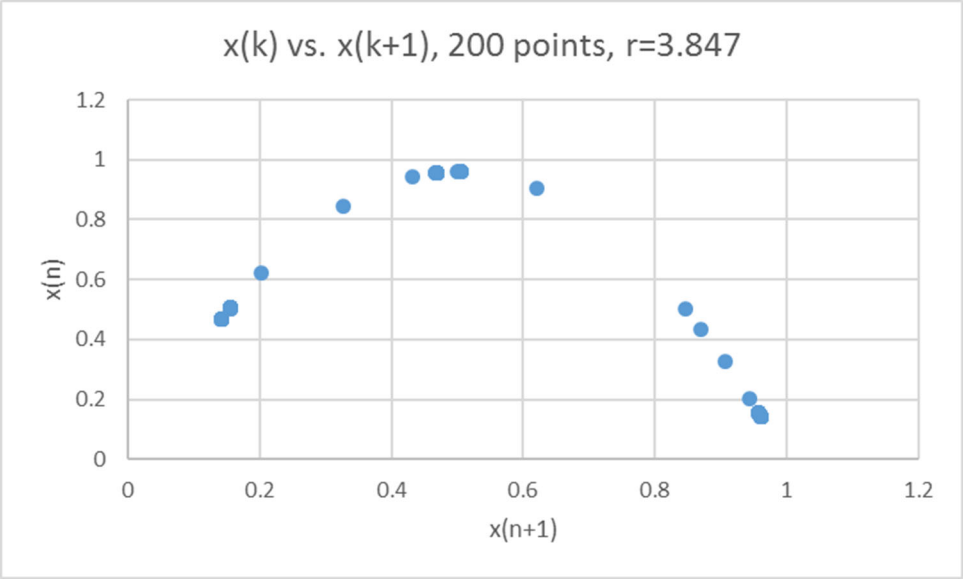
Bifurcation diagram for this system.



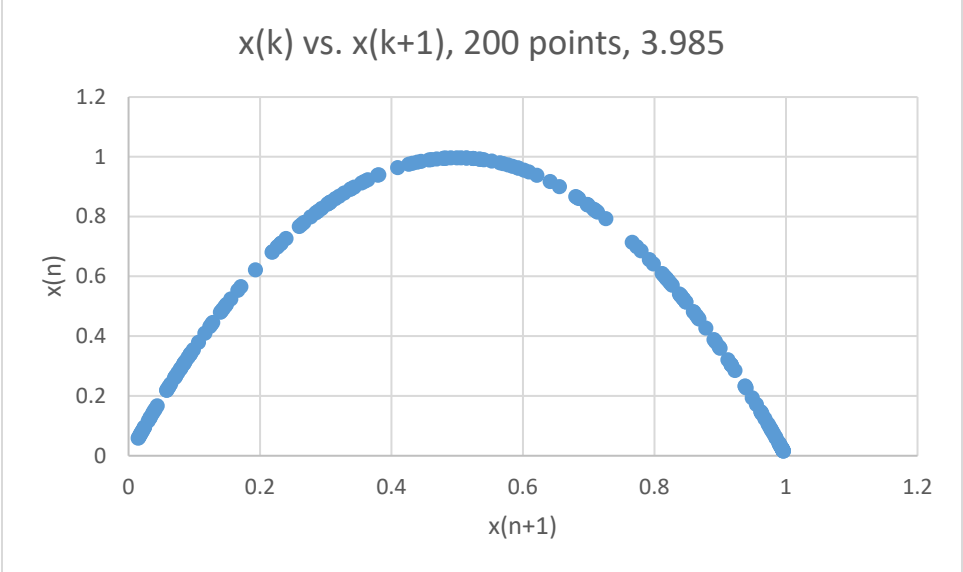
Phase diagram plot for r = 3.6



Phase diagram plot for r = 3.7, with a fuller region than when r = 3.6.



A sparse region.



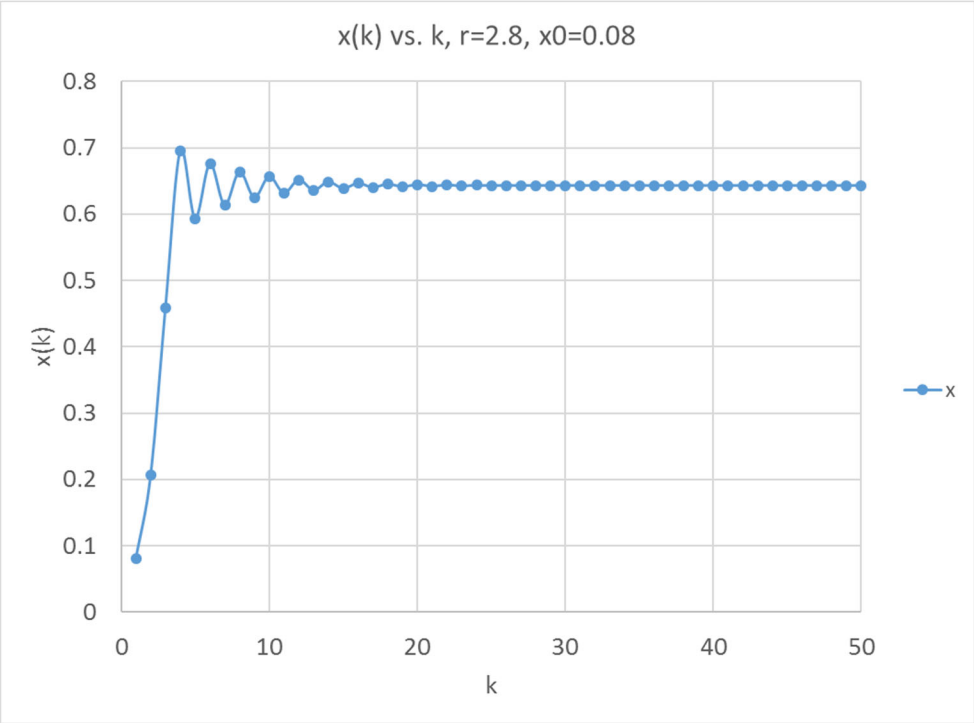
A dense region.

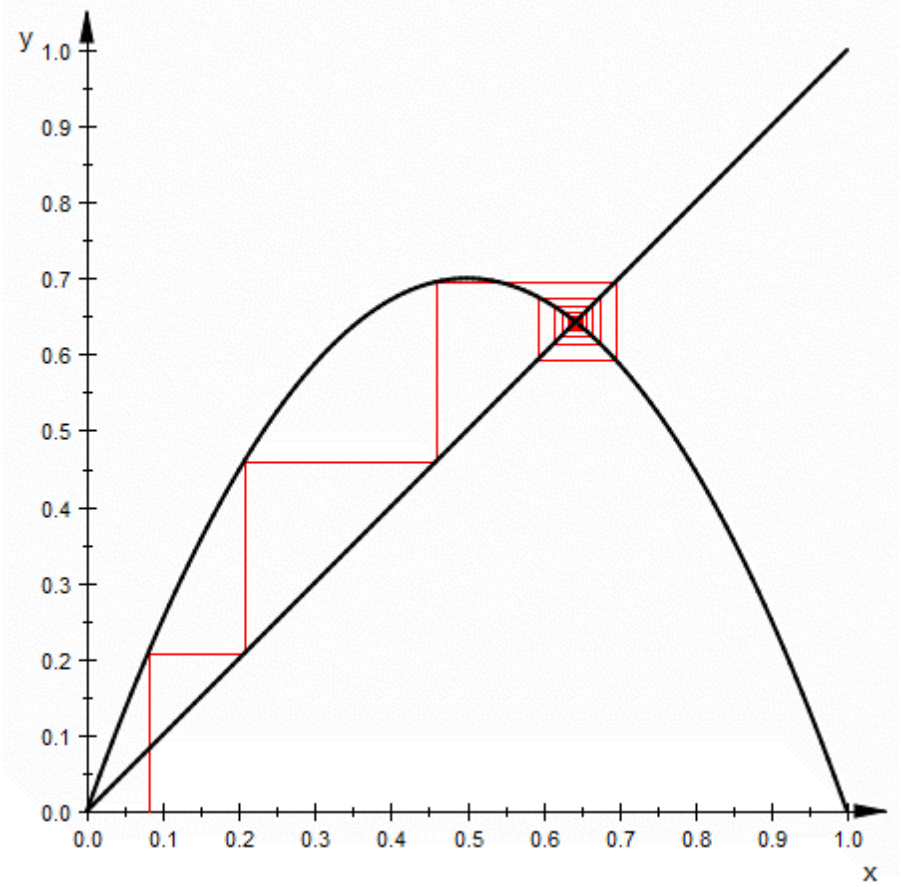
Another qualitative technique for analyzing dynamical systems is to use a "cobweb plot." Here, f(x) = y is plotted versus x, along with the straight line f(x) = y = x. Then other lines link the discrete values of x_k to $f(x_k) = x_{k+1}$. The plot of f(x) vs. x is a curve called the function graph, and the straight line is called the diagonal.

The intersections for y = f(x) and y = x are called "fixed points." Stable fixed points (inward spirals) are attractors (as shown in first cobweb plot below). Unstable fixed points (outward spirals) are repellers. Stable fixed points can also be attractors in a weaker sense, where they are referred to as having "asymptotic stability." The center of spirals will occur at fixed points, i.e. where the diagonal and the function graph cross. If the system is chaotic, a region of the plot will get filled in, indicating an infinite number of non-repeating values.

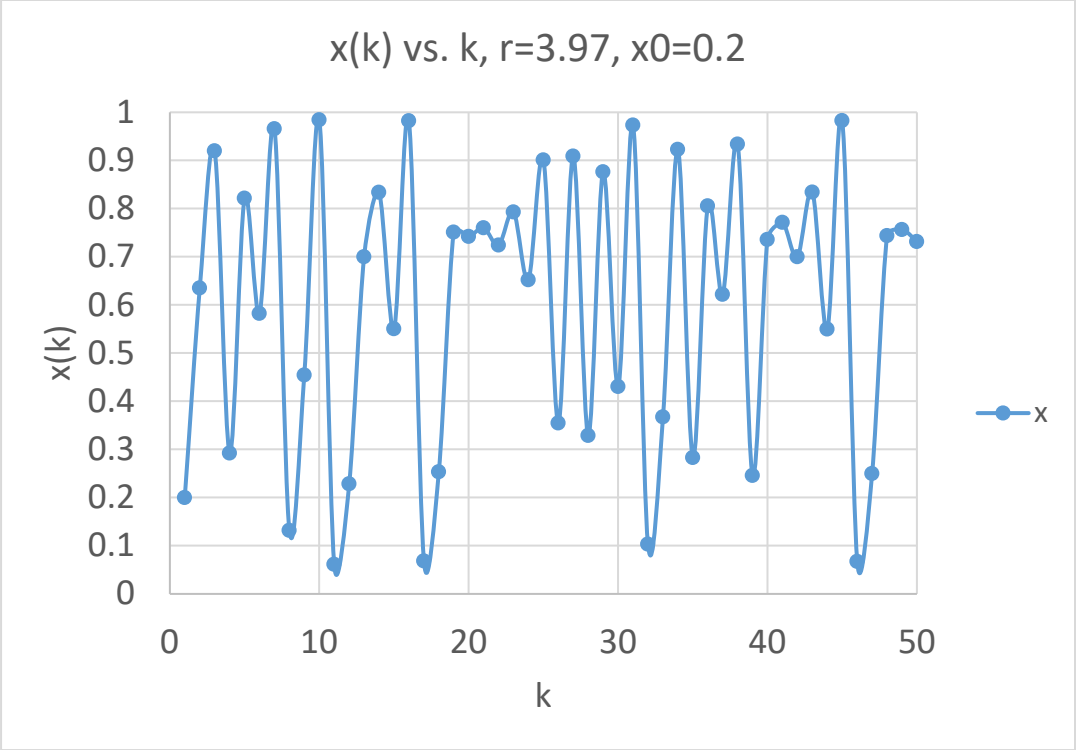
Animated cobweb plot of the logistics map:
https://en.wikipedia.org/wiki/Cobweb_plot#/media/File:LogisticCobwebChaos.gif

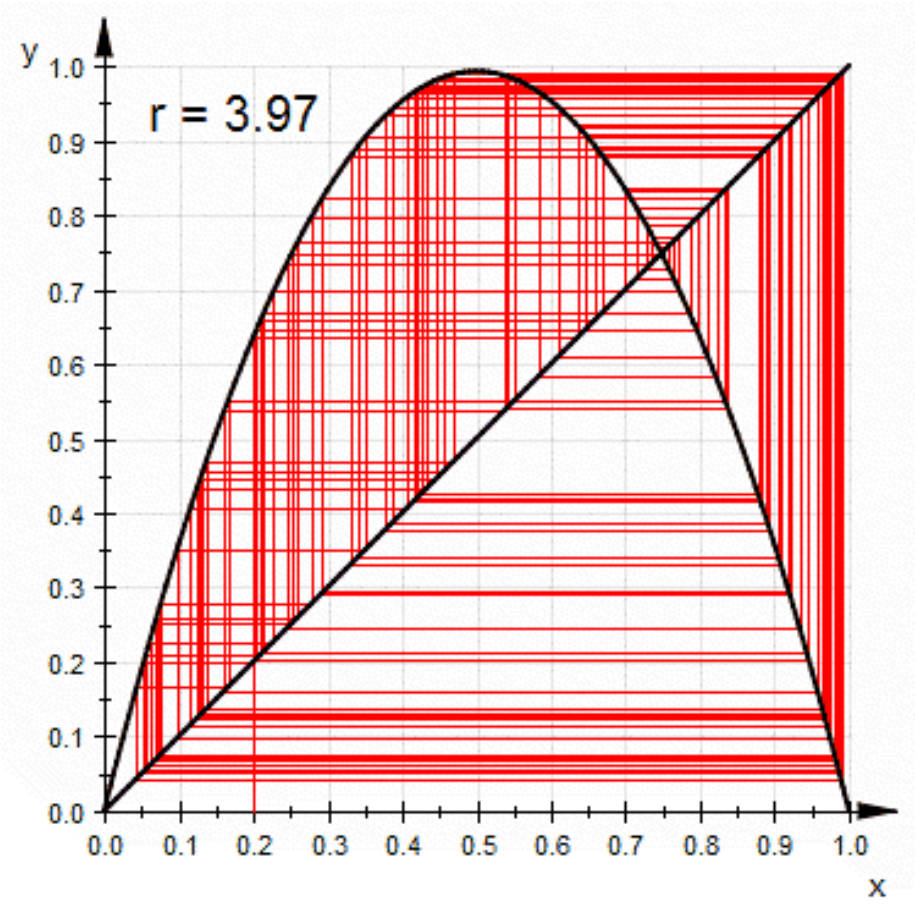
Cobweb Plot Illustration





Cobweb plot for r=2.8





Cobweb plot in chaotic region.

Chaos in Continuous Dissipative Systems

This section deals <primarily> with the types of chaotic systems usually encountered in electronics circuitry ("mostly" analog with nonzero losses).

Linear dissipative and oscillatory (limit cycles) systems can exist in 2nd order or 2-D systems. Examples:

$m\ddot{x} + c\dot{x} + kx = 0$ - Dissipative

$\ddot{x} + ax = 0$ - Oscillatory

$\ddot{x} + (x^2 - 1)\dot{x} + x = 0$ - Limit Cycle

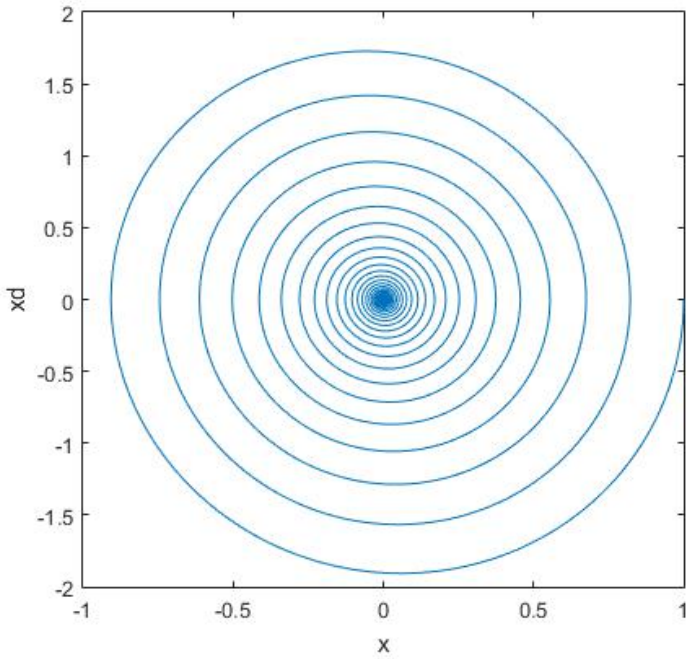
In these systems, since the dimension is only 2, the phase plot "flows" or streamlines" cannot cross (except at an unstable equilibrium point called an X-point (also called a saddle point)).

Under a chaos condition, the streamlines have to cross. To do this, the system must (under most circumstances) be a higher order system (3 states or more). This is formalized in the "Poincaré-Bendixson Theorem".

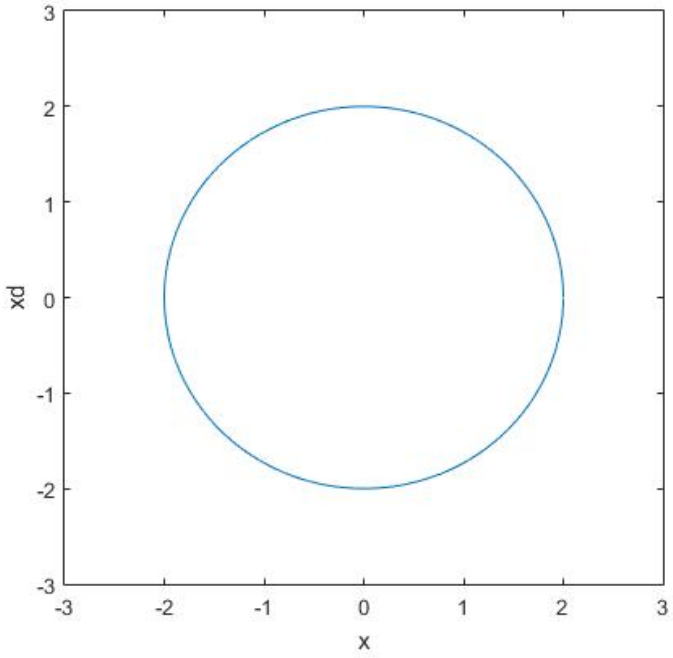
Consider again the Lorenz chaotic system:

$$\dot{x} = \sigma(y - x)$$
$$\dot{y} = -xz + rx - y$$
$$\dot{z} = xy - bz$$

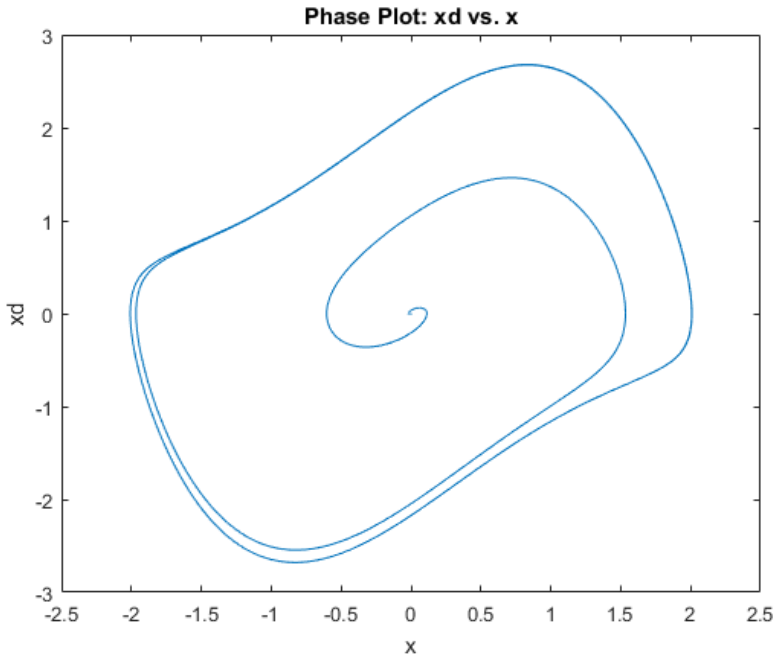
Observe that the strange attractors do not lie solely in the x-y, the x-z or the y-z planes. For a three dimensional chaotic system, the strange attractors possess a non-integer dimension of greater than 2 and less than 3. This way the streamlines can cross each other (when displayed in 2D space) without actually touching each other.



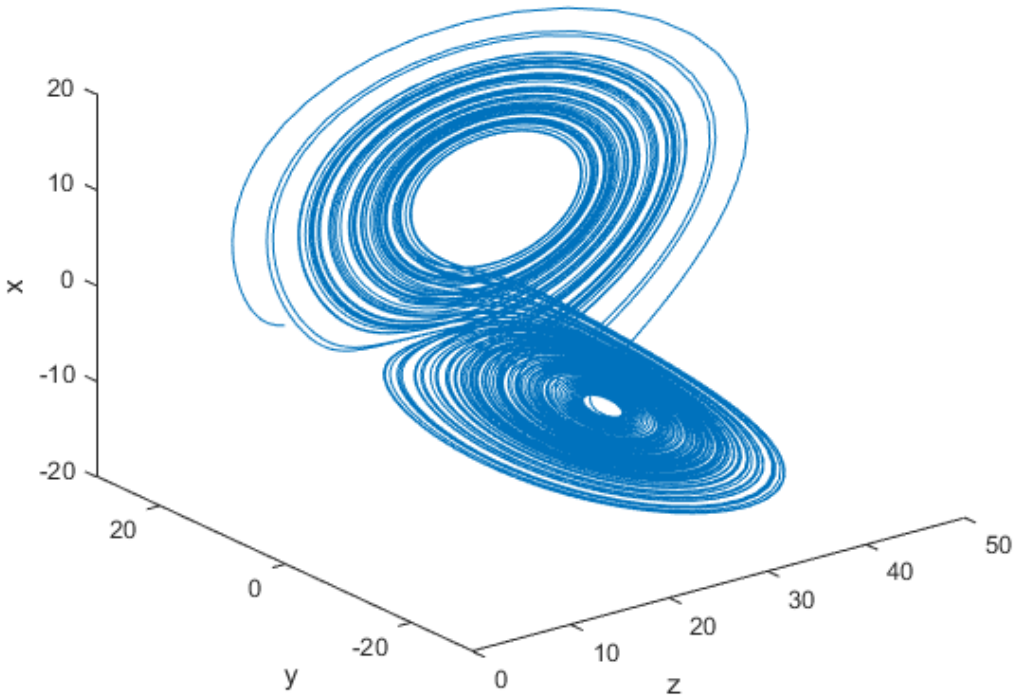
Phase plot for the dissipative case (with a nonzero initial condition).



Phase plot for the oscillatory case (with a nonzero initial condition)



Phase plot of the limit cycle case.



3D Lorenz system phase plot