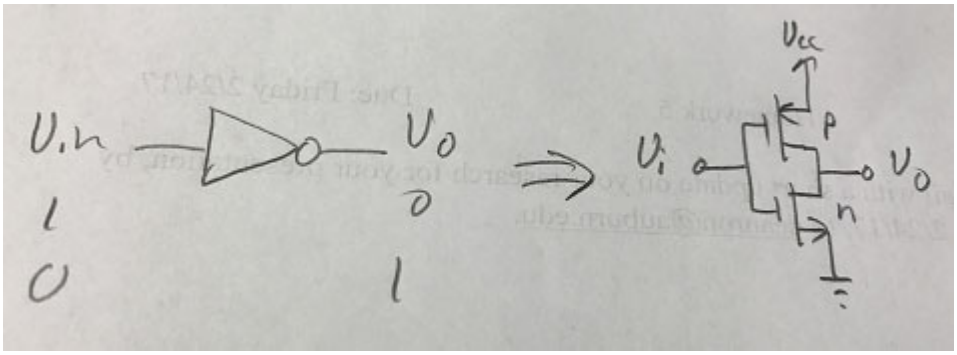
Thursday 2/23/23

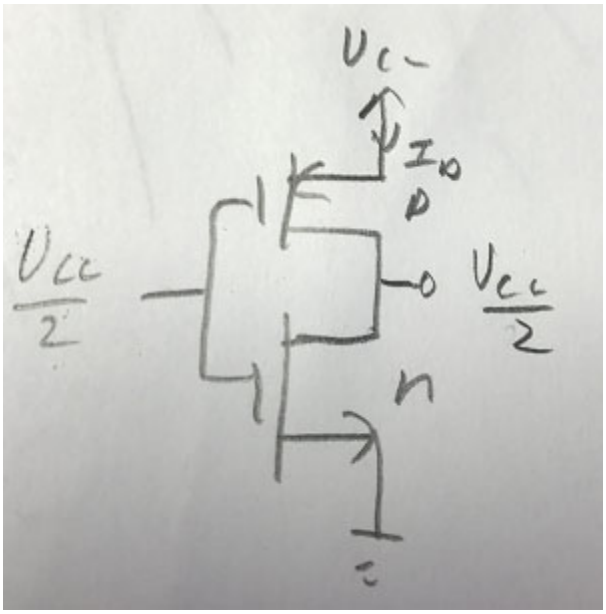
CMOS Inverter Oscillators



When $V_i=V_{cc}$, NMOS is on, PMOS is off, $V_o=0V$, $I_D=0A$.

When $V_i=0V$, PMOS is on, NMOS is off, $V_o= V_{cc}$, $I_D=0A$.

What if $V_i=V_o=V_{cc}/2$? Therefore $I_D \neq 0A$.



The V_{GS}-V_{TN} = $V_{CC}/2 – V_{TN} < V_{DS} = V_{cc}/2$ for the NMOS.

A similar statement is valid for the PMOS.

Both MOS transistors are operating in the saturation region.

Therefore: $I_D = \frac{\beta_n}{2}\left(V_{GS_N} - V_{TN}\right)^2 = \frac{\beta_p}{2}\left(V_{SG_P} - |V_{TP}|\right)^2$

$$\frac{\beta_n}{2}\left(\frac{V_{cc}}{2} - V_{TN}\right)^2 = \frac{\beta_p}{2}\left(\frac{V_{cc}}{2} - |V_{TP}|\right)^2$$

Assuming that $V_{TN} \approx |V_{TP}|$, then:

$\beta_n = \beta_p$

or: $k'_n\left(\frac{W}{L}\right)_n = k'_p\left(\frac{W}{L}\right)_p$

leading to: $\frac{k'_n}{k'_p} = \frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n}$

Consider the SPICE parameters for MOSIS 2 μm CMOS process <next page>

$k'_n = k_{p_{nmos}} = 5.06x01^{-5}$ A/V^2

$k'_p = k_{p_{pmos}} = 1.69x01^{-5}$ A/V^2

Therefore, : $\frac{k'_n}{k'_p} = 2.994 \sim 3$

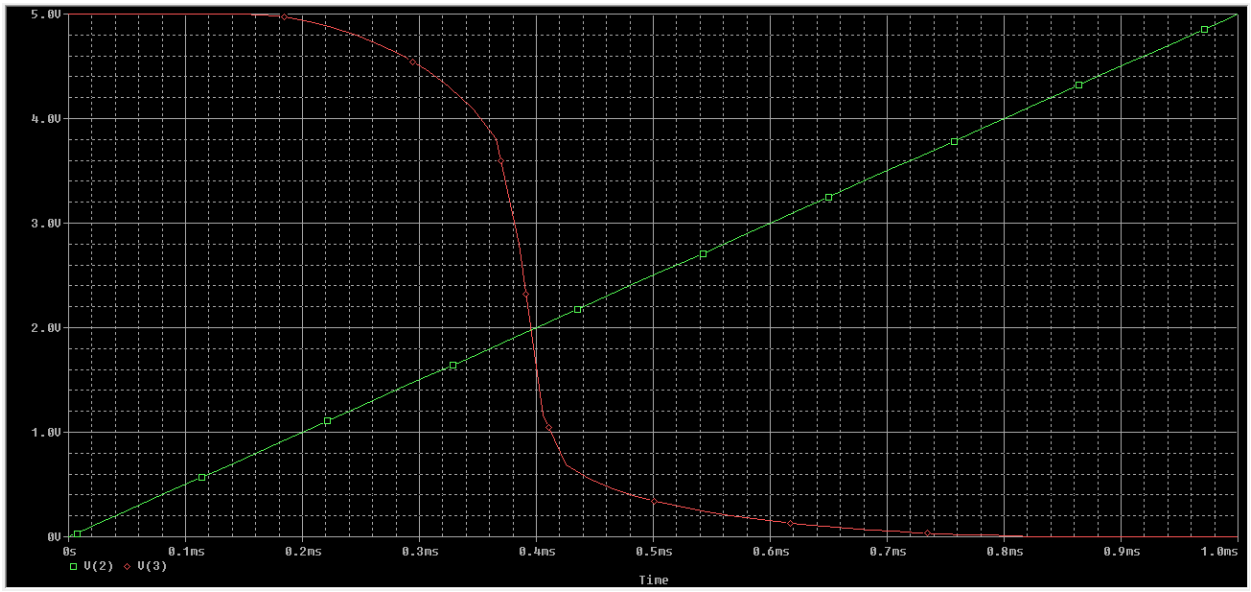
Therefore, the PMOS transistor's channel width needs to be about 3 times larger than the NMOS transistor's channel width to achieve V_o=V_{in} at V_{cc}/2 for the CMOS inverter.

Examples shown below:

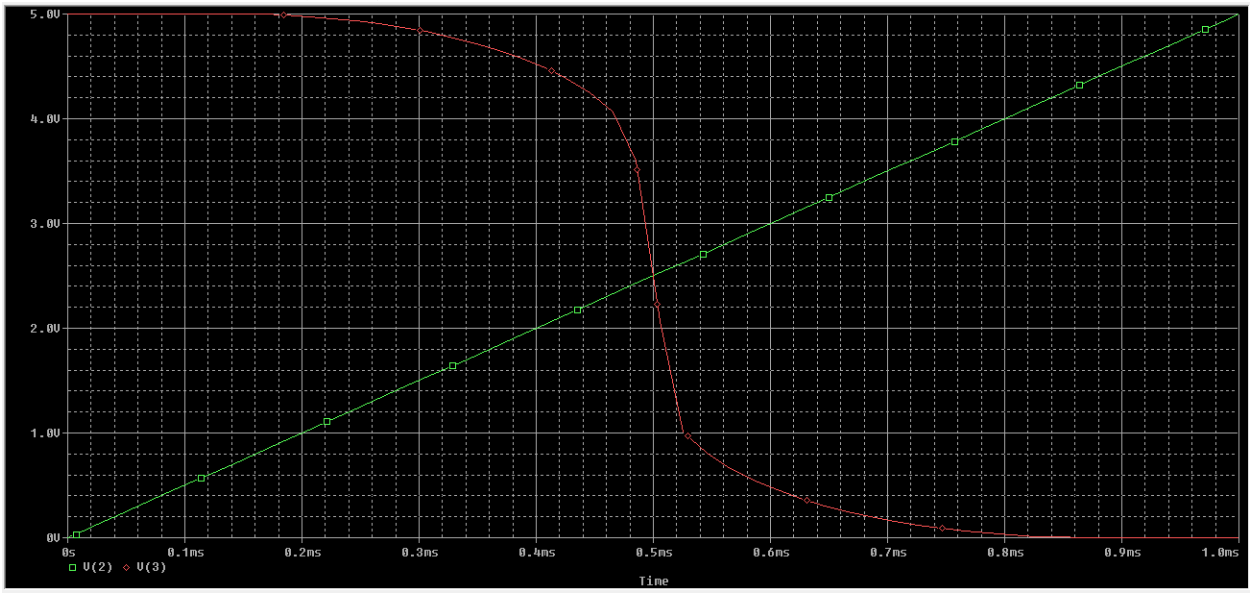
1990 MOSIS 2μm CMOS process SPICE parameters:

.MODEL TYPEN NMOS (LEVEL=2 LD=.12737U TOX=430.000002E-10 NSUB=1.40118E15 VTO=.788864 KP=5.06E-5 GAMMA=.269 PHI=.6 UO=630 UEXP=.169017 UCRIT=30875.9 DELTA=2.68865 VMAX=61343.6 XJ=.25U LAMBDA=.0298011 NFS=1E11 NEFF=1 NSS=1E12 TPG=1 RSH=39.000002 CGDO=1.02281E-10 CGSO=1.02281E-10 CGBO=2.00756E-10 CJ=.0001487 MJ=.65 CJSW=5.673E-10 MJSW=.3 PB=.56)

.MODEL TYPEP PMOS (LEVEL=2 LD=.1U TOX=430.000002E-10 NSUB=6.04791E15 VTO=-.715528 KP=1.69E-5 GAMMA=.558 PHI=.6 UO=210 UEXP=.130255 UCRIT=6966.18 DELTA=.983911 VMAX=22889.2 XJ=.25U LAMBDA=.0662518 NFS=5.63794E11 NEFF=1.001 NSS=1E12 TPG=-1 RSH=132.000009 CGDO=8.03023E-11 CGSO=8.03023E-11 CGBO=8.03023E-11 CJ=.0002688 MJ=.6 CJSW=1.79E-10 MJSW=.26 PB=.6)



V_o vs. V_{in} for same (W/L) ratios.



V_o vs. V_{in} for $(W/L)_p = 3(W/L)_n$ ratios.

The gate structure of a MOS transistor is a capacitor of area W*L. The impedance looking into a CMOS inverter is two MOS capacitors in parallel.

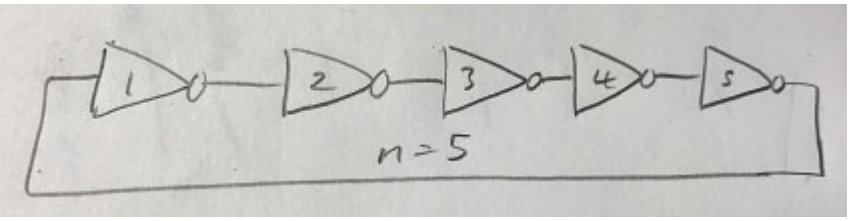
The output impedance of a CMOS inverter is resistive.

Therefore a propagation delay occurs in a CMOS inverter proportional to R_o*2C_{gate}.

A string of n-inverters will have a total propagation delay approximately equal to $n(R_o*2C_{gate})$.

Let τ_{inv} be the total propagation delay through a CMOS inverter. Then an n-inverter chain will have a total propagation delay of $n(\tau_{inv})$. Show example.

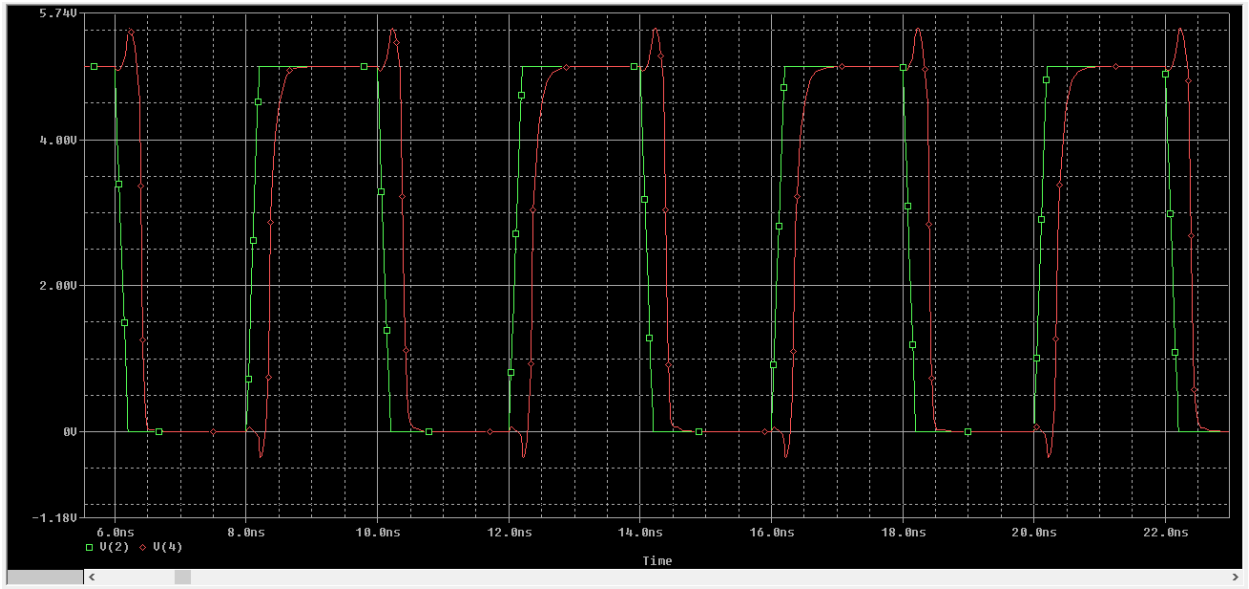
A previously stated, a ring oscillator is an odd number of CMOS inverters connected in an unbroken chain:



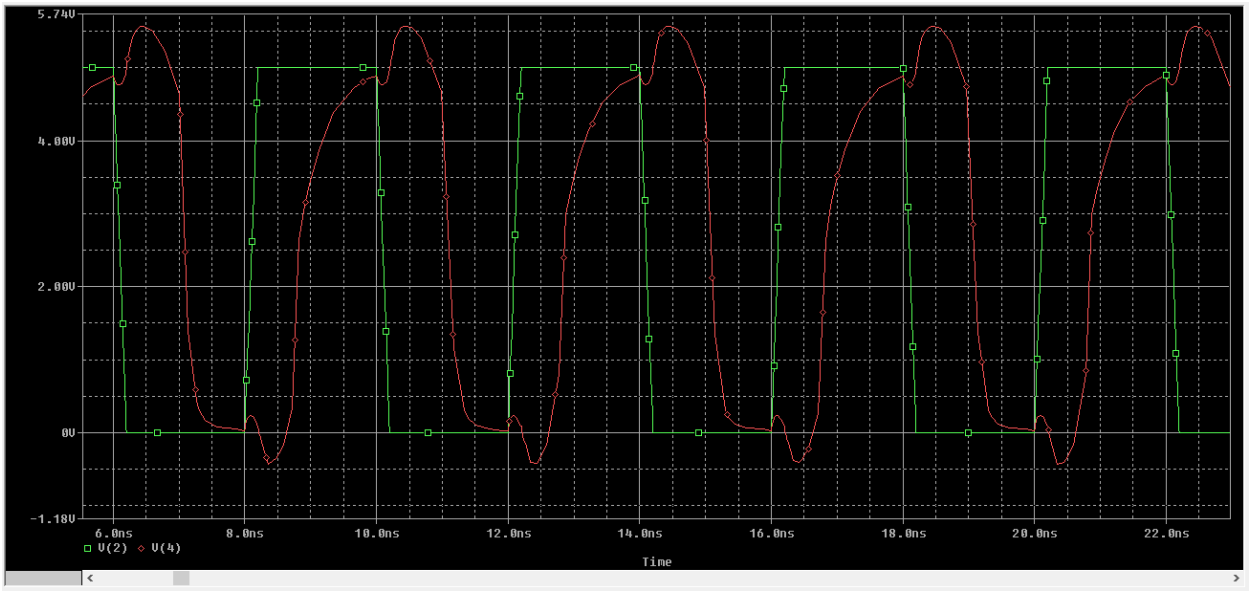
Show PSPICE simulation <below>.

Notice that for small n, the output is not a square wave.

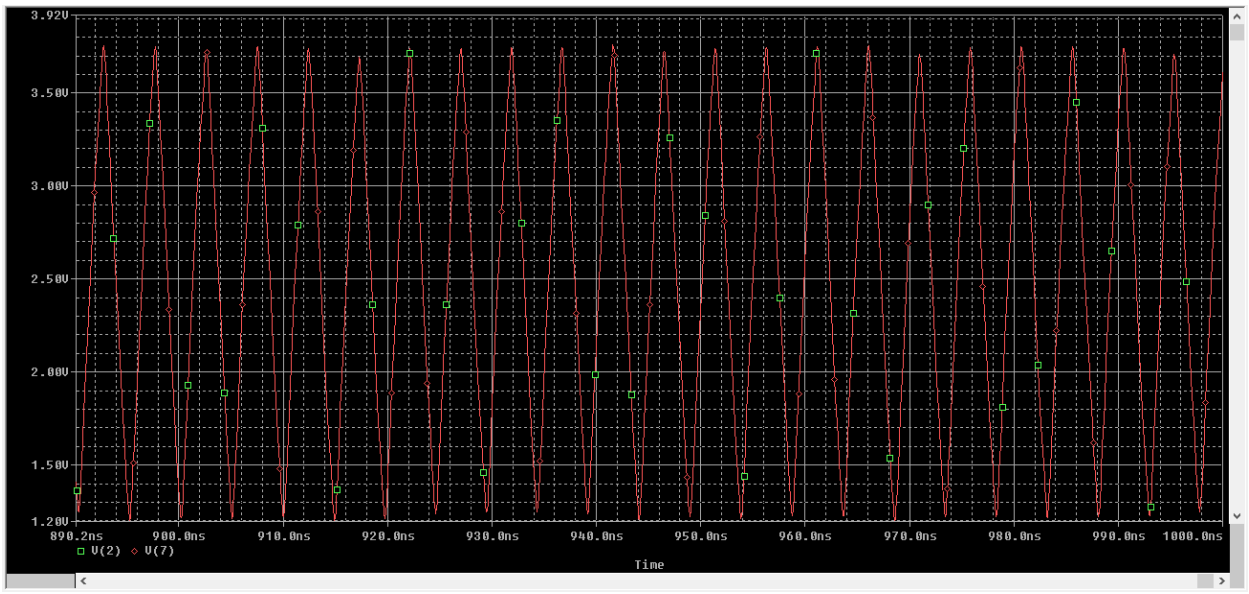
Adding a discrete RC stage between 2 inverters can lower the frequency and square up the output signal



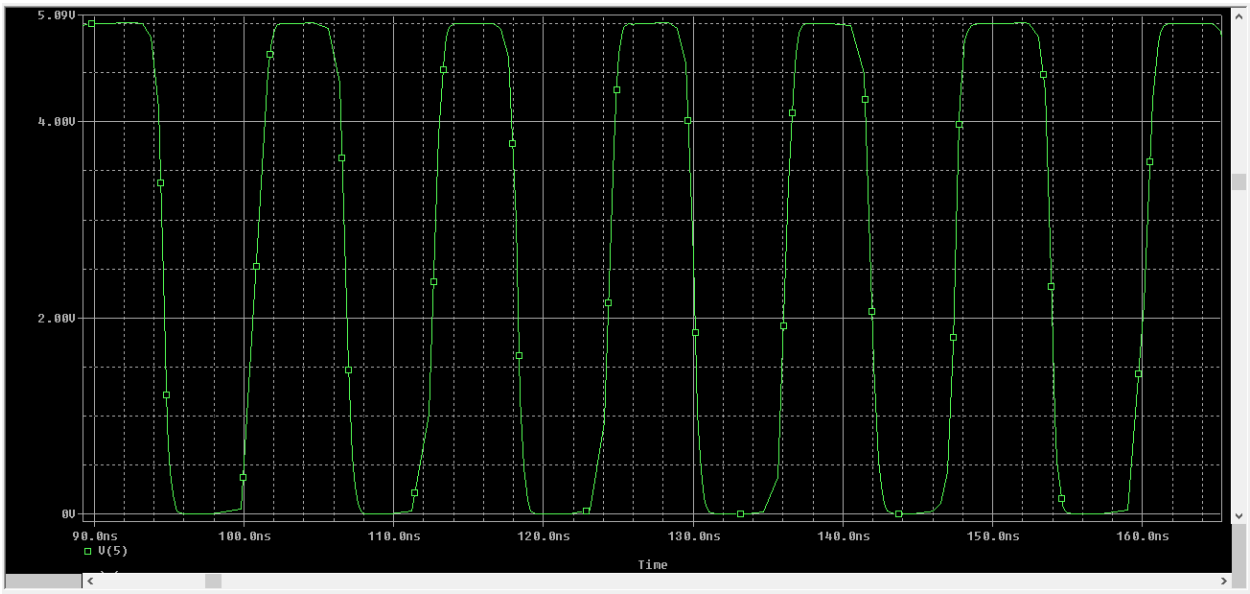
V_{in} and V_o for 2 CMOS inverter chain with input 250 MHz square wave.



V_{in} and V_o for 2 CMOS inverter chain with input 250 MHz square wave, with the gate areas of the transistors doubled. Propagation delay increased, and the quality of output square wave decreased.



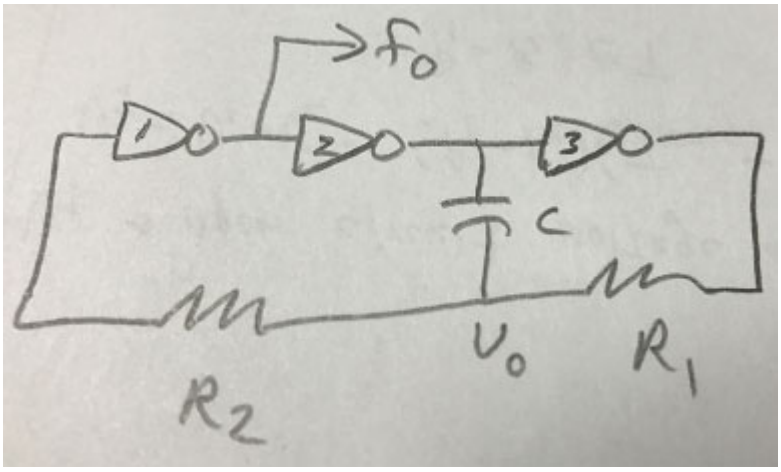
Output from the 5 inverter CMOS ring oscillator. Note, add very small RC stage (1 mΩ – 1 pF) between two inverters to place an initial condition across the C to initiate oscillation in PSPICE.



Same output from 5 inverter CMOS ring oscillator with 10 kΩ – 10 pF RC stage in between 2 inverters. This lowered the frequency of oscillation.

CMOS Inverter Relaxation Oscillators

Consider this circuit:



If C was not present and both resistors were shorts, this circuit would just be a 3 inverter CMOS ring oscillator.

However, let $R_1 = R_2 = R$.

Also, let the RC time constant be very large compared to the propagation delay through an inverter (i.e. the inverters switch very "fast"). As part of this, let C be much greater than the input capacitance looking into an inverter.

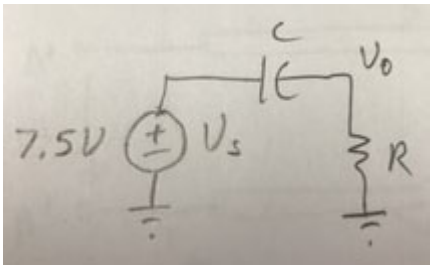
Finally, assume that each inverter is balanced so that the trip voltage is equal to $V_{cc}/2$.

To analyze the circuit let's let $V_{cc} = 5$ V. Realize that when V_o reaches $V_{cc}/2$ (the inverter trip voltage: 2.5 V), the system will change states.

Assume that C is initially fully discharged, and Inv 2's output is 0 V while Inv 3's output is 5 V. C will charge up through R_1 until $V_o = 2.5$ V. Then the three inverters will change states. Now the output of Inv 2 is 5 V and the output of Inv 3 is 0 V.

Since the voltage across a capacitor cannot change instantaneously, v_o becomes 5 V + 2.5 V = 7.5 V. C will now discharge down to 2.5 V, triggering another

system state change. So use this circuit model to determine how long until the next state change:



$$\frac{V_o}{V_s} = \frac{R}{R + \frac{1}{sC}} = \frac{s}{s + \frac{1}{RC}}$$

$$V_s(s) = \frac{7.5}{s}$$

$$V_o(s) = V_s(s)\left(\frac{s}{s + \frac{1}{RC}}\right) = \frac{7.5}{s + \frac{1}{RC}}$$

$$v_o(t) = 7.5e^{-\frac{t}{RC}}$$

We want to evaluate t when $v_o(t) = 2.5$ V

$$2.5 = 7.5e^{-\frac{t}{RC}}$$

Solving for t: $t = -RCln\left(\frac{2.5}{7.5}\right) = 1.0986RC$

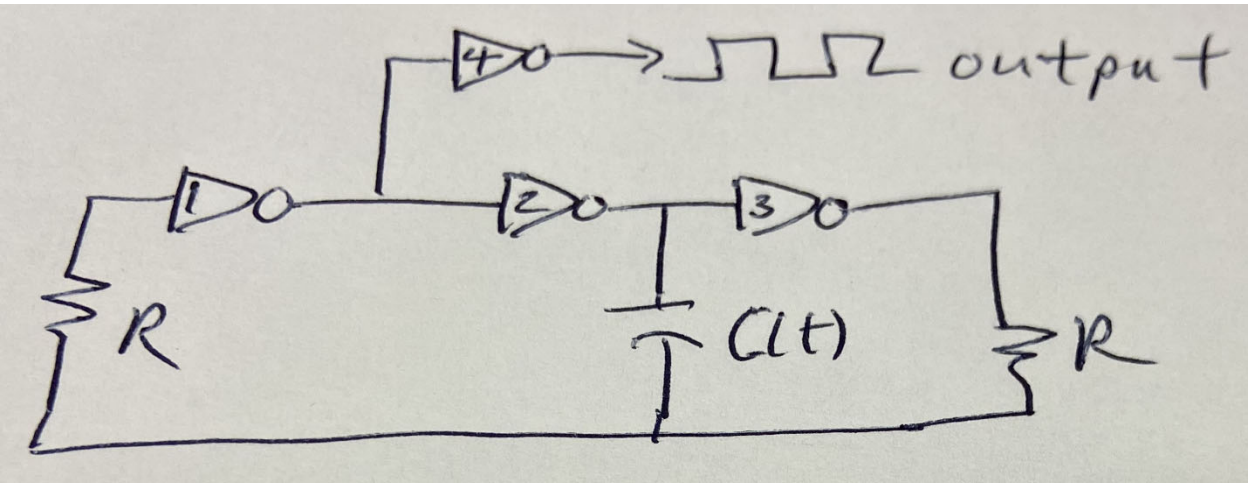
For the square wave output: T = 2t and f = 1/T.

Therefore: $f = \frac{0.455}{RC}$

For an actual circuit, the equation for f will be slightly different due to the analysis assumptions we made. But for low frequency square waves, it should be close.

Note, when the voltage into an inverter is between Vcc – V_{tp} and V_{tn}, both transistors are on and dissipating energy as heat. So this circuit puts a little stress on the CMOS circuitry each cycle. This could possibly be a problem and lead to thermal failure of the inverter IC, particularly if the background air temperature is hot. But experimentally, failures are rare.

This circuit can be used as a sensor interface circuit where the sensor produces either R(t) with a fixed C in the circuit, or C(t) with a fixed R in the circuit. R(t) or C(t) are proportional to the measurand being detected by the sensor. In this case, the period of the square wave output, T, is proportional to R(t) or C(t). Below is a practical interface circuit for a capacitive sensor, C(t):

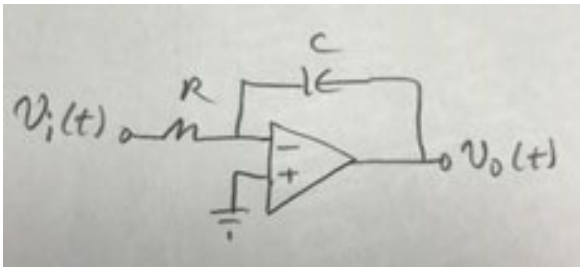


Inverter 4 (6 inverters typically in the IC package) prevents the attached circuit from loading down the oscillator and affecting its fundamental frequency.

Note: We ignored the effects of the R on the left with the input capacitance of Inv 1. If R on the left is particularly small compared to the R on the right, this can affect the equation we derived for the oscillation frequency.

Op Amp Based Relaxation Oscillators

Op amps can also be used to construct relaxation oscillators. They often use an op amp integrator to determine the oscillator time constant:



$$V_o(s) = -V_i(s)\frac{1}{sRC}$$

$$v_o(t) = \frac{-1}{RC}\int_0^t v_i(t)dt$$

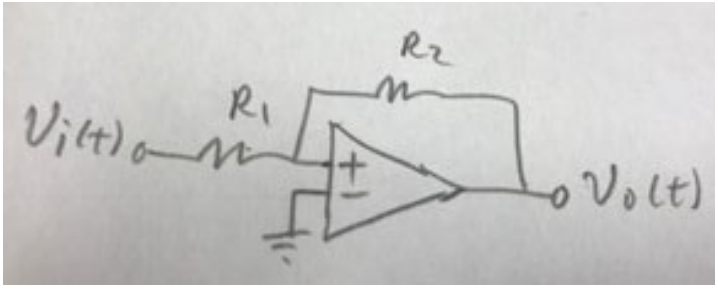
If $v_i(t)$ is a constant, V_i, then:

$v_o(t) = -\frac{V_i}{RC}t$, if the capacitor is initially discharged.

If the capacitor is initially charged, i.e. $v_o(t) = V_{o1}$ at t = 0s, then:

$v_o(t) = V_{o1} - \frac{V_i}{RC}t$ for $t \geq 0$s

Consider the positive feedback amplifier circuit:



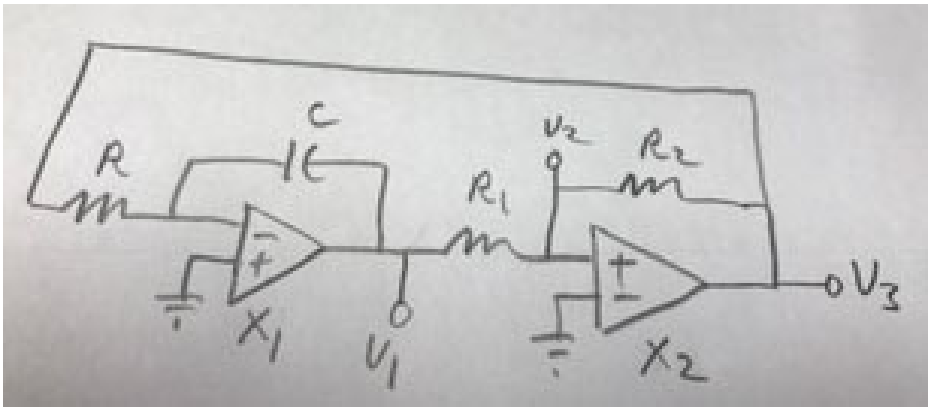
If the positive input's voltage is greater than the negative input's voltage, $v_o(t)$ will go to the positive rail, V+. For the opposite situation, $v_o(t)$ will go to the negative rail, V-.

For an initial condition of $v_o(t)$, either V+ or V-, the current voltage at the positive input port, v_{pos}, can be determined from:

$$v_{pos} = v_i + (v_o - v_i)\frac{R_1}{R_1 + R_2}$$

Changing $v_i(t)$ sufficiently will cause the amplifier to "change states": V+→V- or V-→V+.

Combined Circuit:



For analysis purposes, assume V_3 can only be V+ or V-.

At t = 0-, assume that $V_2 = 0V\uparrow$ and V_3 = V-.

Therefore: $0 = V\_ + (V_1 - V\_)\frac{R_2}{R_1+R_2}$

Simplifying: $0 = V\_(R_1 + R_2) + (V_1 - V\_)R_2$

And: $0 = V\_R_1 + V_1R_2$

Finally: $V_1 = -V_- \frac{R_1}{R_2}$

This is then the initial condition on the integrator at t = 0+, when V_3 switches to V+.

Therefore: $V_1 = -V_- \frac{R_1}{R_2} - \frac{V_+ t}{RC}$

And: $V_2 = V_1 + (V_+ - V_1) \frac{R_1}{R_1 + R_2}$

We want to find how long until V_2 = 0V.

Therefore: $0 = V_1 + (V_+ - V_1) \frac{R_1}{R_1 + R_2}$

Simplifying to: $0 = V_1 R_2 + V_+ R_1$

$$0 = \left(-V_- \frac{R_1}{R_2} - \frac{V_+ t}{RC}\right) R_2 + V_+ R_1$$

Assume that V+ = -V-

Therefore: $0 = -\frac{V_+ t}{RC} R_2 + 2V_+ R_1$

Leading to: $t = \frac{2R_1 RC}{R_2}$

One period of oscillation: $T = 2t = \frac{4R_1 RC}{R_2}$

Oscillation frequency: $f = \frac{1}{T} = \frac{R_2}{4R_1 RC}$

Output waveforms: