1. <u>Si Heterojunction PV Technology</u>

→ PIN structure

I → intrinsic layer is lightly n-doped single crystal Si

P → p-layer is p-doped aSi(H) } very thin layers

N → n-layer is n-doped aSi(H) }

SCS → $E_G \sim 1.2 eV$

aSi(H) → $E_G \sim 1.8 eV$

SCS → low defect density, high carrier mobility, minimizes bulk recombination

aSi(H) → thin and ∴ easy to dope, better photon absorption than SCS, higher bandgap results in a lower loss metallic contact than SCS (less recombination)

a. <u>structure</u>

→ Show images on next page

I → n-type <100> SCS, made by float zone (FZ) process, ~300 μm thick

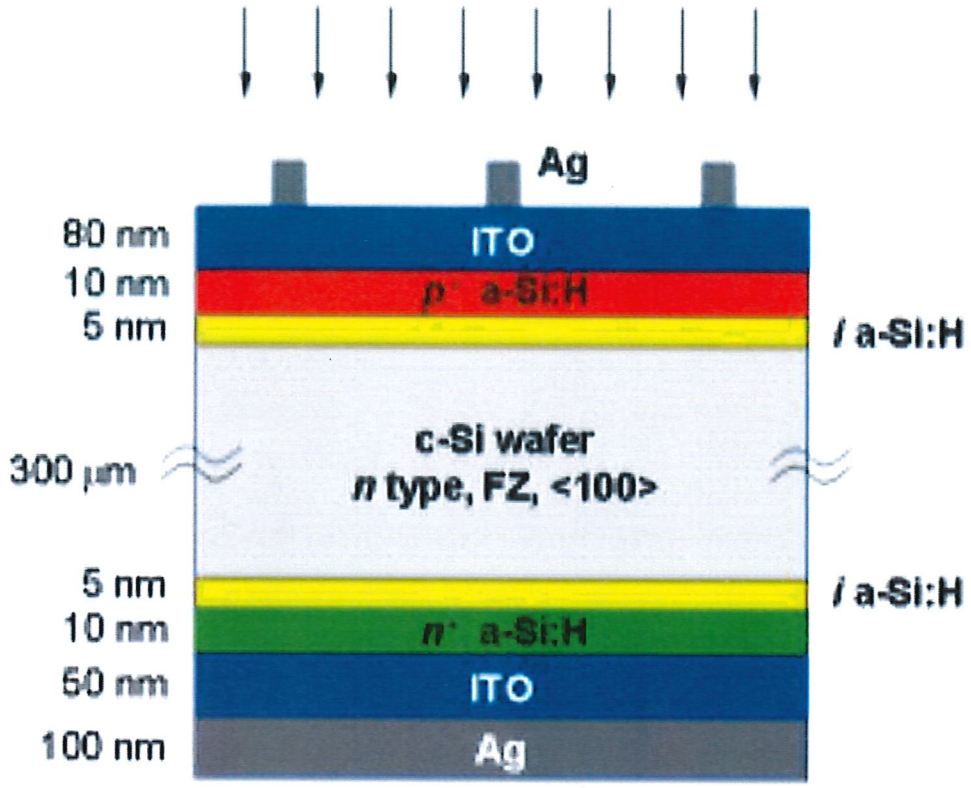
→ part of I is ~5nm thick aSi(H) on both sides

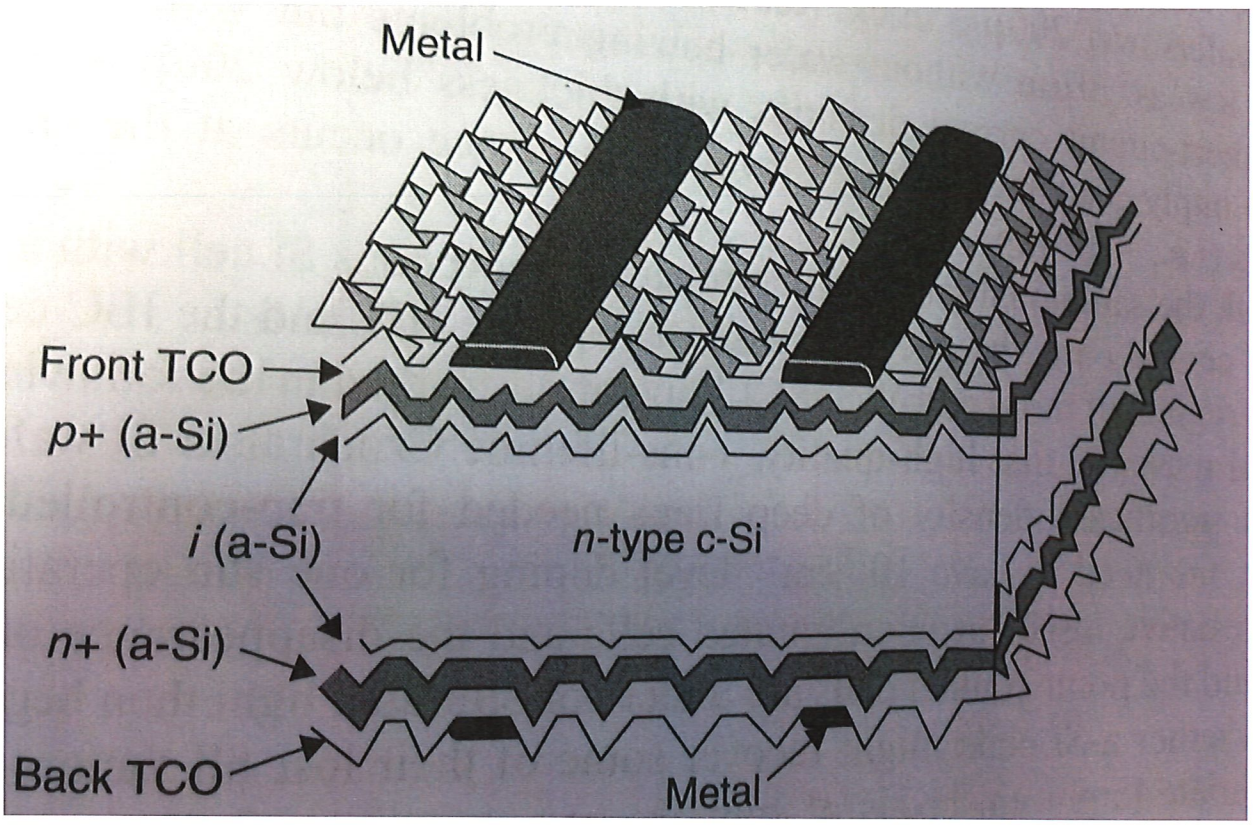
P → ~10nm thick p-type aSi(H)

N → ~10nm thick n-type aSi(H)

Top ITO (TCO - Transparent Conductive Oxide)

↳ serves as the ARC, conductive contact to aSi(H) layer, and a passivation layer


Ag
80 nm
ITO
10 nm
p+ a-Si:H
5 nm
i a-Si:H
300 μm
c-Si wafer
n type, FZ, <100>
5 nm
i a-Si:H
10 nm
n+ a-Si:H
50 nm
ITO
100 nm
Ag


Metal
Front TCO
p+ (a-Si)
i (a-Si)
n-type c-Si
n+ (a-Si)
Back TCO
Metal

Back ITO → backside aSi(H) passivation and conductive contact layer, and BSF layer

Ag → metal contacts on top and bottom

Textured Surfaces → reduces reflection losses and increases photon path length in the cell

b. <u>More Information</u>

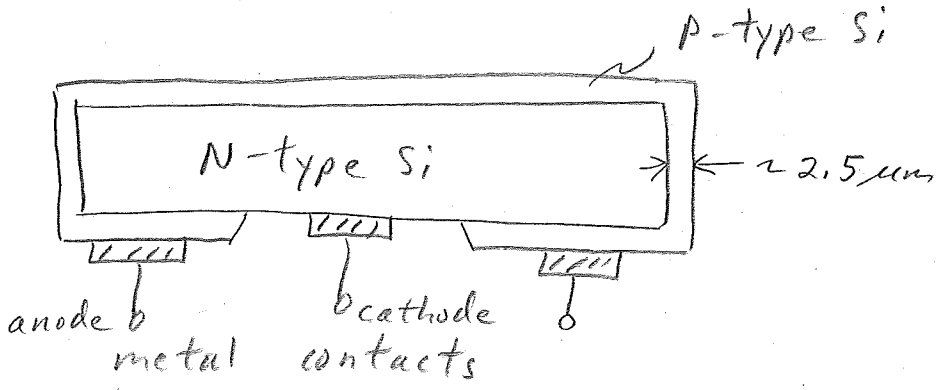
→ Also called a HIT cell and Si-HJT ↔ T ≡ Technology

"HIT" → heterojunction with intrinsic thin-layer

→ large area devices (>100cm²) built with efficiencies ~23% have been reported

→ mass produced devices : 21.8% efficiency with $V_{oc} = 0.718V$

→ Compare complexity of 21.8% efficiency HIT cell with 6% efficiency 1954 Si cell



$V_{OUT} \sim 0.5V$