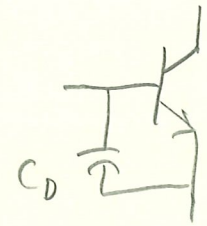
c. C_D - diffusion capacitance

placed in parallel with the forward-biased BE diode

ex:



$$C_D = \frac{I_C}{V_T} \tau_F$$

d. Frequency dependence of the common emitter current gain

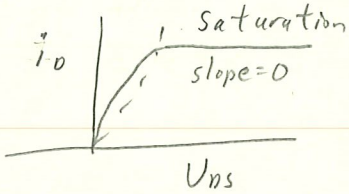
$$\beta(f) = \frac{\beta_F}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

where f_β is freq where $\beta(f) = 1 \rightarrow$ "β-cutoff frequency"

$f_\beta = \frac{f_T}{\beta_F}$ and $f_T \equiv$ unity gain frequency

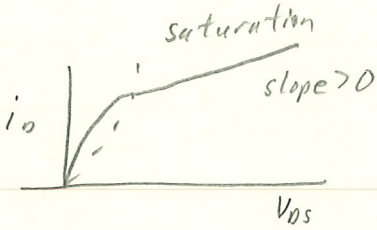
e. Early Effect & the Early Voltage

Remember



$$i_D = \frac{1}{2} k_n (v_{GS} - V_{TN})^2$$

but actually:

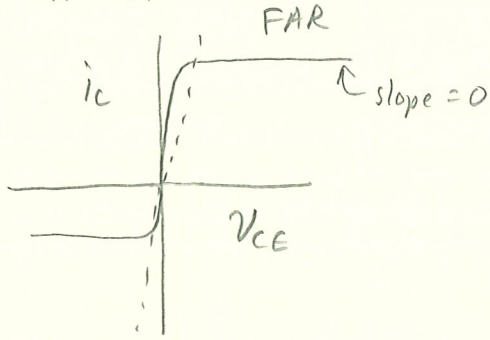


$$i_D = \frac{1}{2} k_n (v_{GS} - V_{TN})^2 (1 + \lambda v_{GS})$$

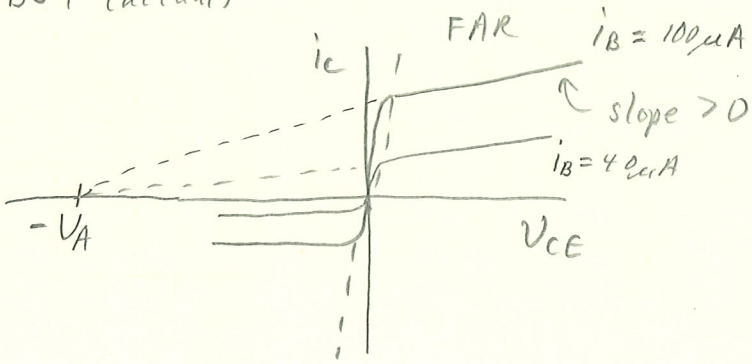
$\lambda \equiv$ channel-length modulation parameter

similar effect in BJT's

BJT (ideal)



BJT (actual)



$V_A \equiv$ Early Voltage, typically: $15V \leq V_A \leq 150V$

Cause → modulation of the base width (W_B) by the collector-base voltage

↓

collector-base space charge region inc. as V_{CB} inc.

↑ "(BSCR)

and as CBSCR ↑, W_B ↓

→ Early effect reduces BJT output resistance and effects performance as an amplifier

2. Transconductance (g_m)

BJT → relates changes in i_c to changes in v_{BE}

definition : $g_m = \left.\frac{di_c}{dv_{BE}}\right|_{Q\text{-point}} = \frac{I_c}{V_T}$, $[g_m] = \Omega^{-1}$

→ very important in amplifier circuits

MOSFET: $g_m = \left.\frac{di_D}{dv_{GS}}\right|_{Q\text{-point}} = k_n' \frac{W}{L}(V_{GS} - V_{TN}) = \frac{2I_D}{V_{GS} - V_{TN}}$

* $g_{m_{BJT}} >> g_{m_{FET}}$

∴ BJT's amplifiers can have higher gain than equiv. MOSFET amp

Finding g_m

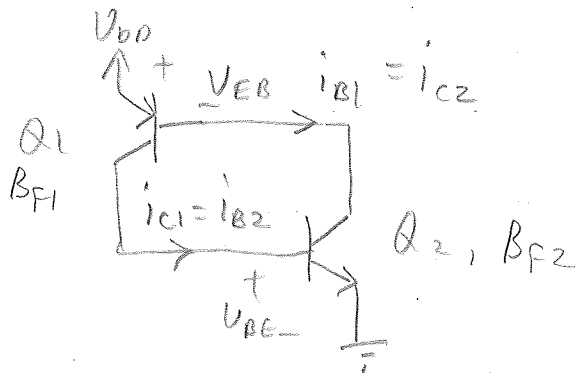
① Find T Q-point

② Calculate g_m

3. Latchup in CMOS circuits

- A potentially catastrophic issue

a. Consider this circuit:



Condition called "Latchup"

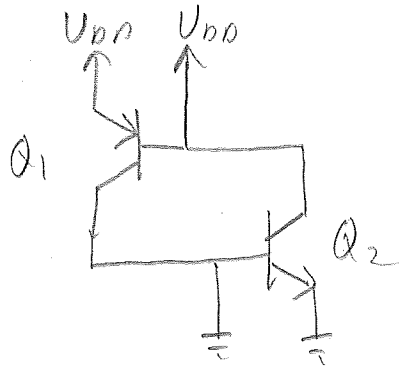
Assuming Q_1 and Q_2 in saturation

$i_{C2} = \beta_{F2} i_{C1} = \beta_{F1}\beta_{F2} i_{B1} = \beta_{F1}\beta_{F2} i_{C2}$

if $\beta_{F1}\beta_{F2} > 1$, i_{C1} and i_{C2} grow until the circuit fails from overheating, or the external circuit (V_{DD} here) limits $i_{C_{max}}$

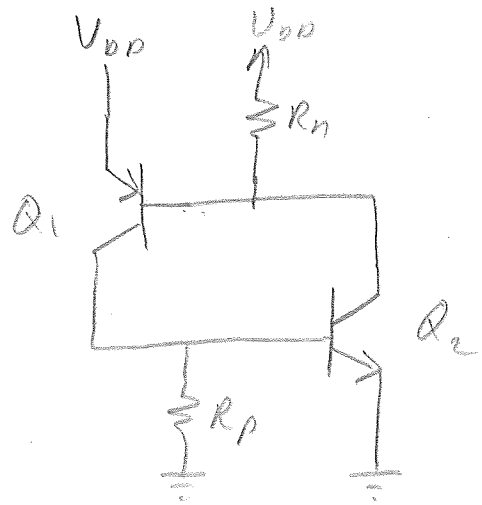
This circuit is unstable

Consider this



$V_{EB1} = V_{BE2} = 0V$; Q_1 + Q_2 off

Consider this



if R_n & R_p are big enough, latchup can occur.

if R_n & R_p are small enough, latchup does not occur

Latchup in CMOS

→ Parasitic Bipolar Transistors exist in CMOS processes → latchup potential delays widespread adoption of CMOS. Show Fig 7.42 (text p. 399)

→ Modern CMOS processes work to minimize R_n & R_p (shunting resistors)

several things can initiate latchup:

① an external fault or transient where one of the source or drain diffusions momentarily exceeds the power supply voltage levels

② exposure to ionizing radiation

③ exposure to intense light

4. The FinFET → textbook pp. 400–402