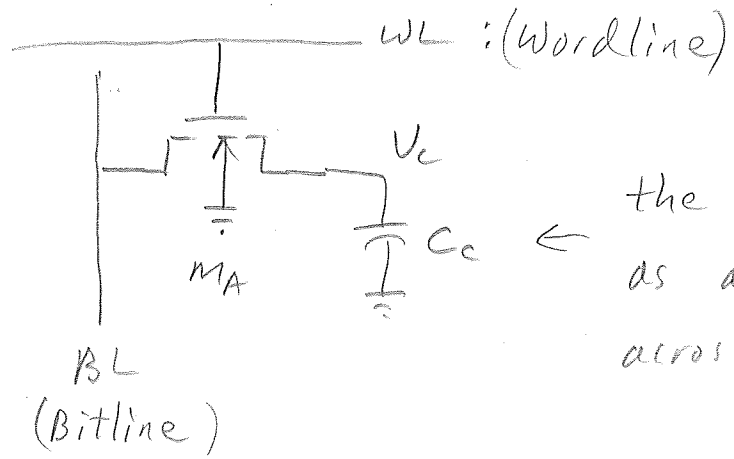
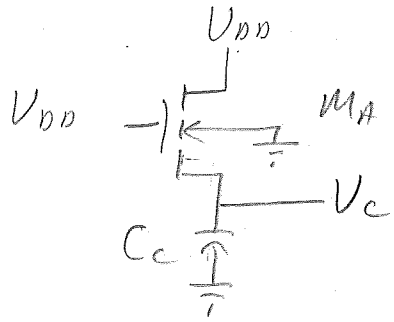
1. DRAM 1T-Cell Memory Cell



← the "1" or "0" is stored as an analog voltage across C

Storing a "0" → BL → 0V and WL → V_{DD} : $V_c \to 0V$

Storing a "1" → BL → V_{DD} and WL → V_{DD} : $V_c \to V_{DD} - V_{TN}$



C_c charges up until M_A turns off: $V_{GS} - V_{TN} = 0V$

$\therefore V_c\big|_{final} = V_{DD} - V_{TN}$

Due to Body Effect: $V_{TN} = V_{T0} + \gamma\left(\sqrt{V_c + 2\phi_F} - \sqrt{2\phi_F}\right)$

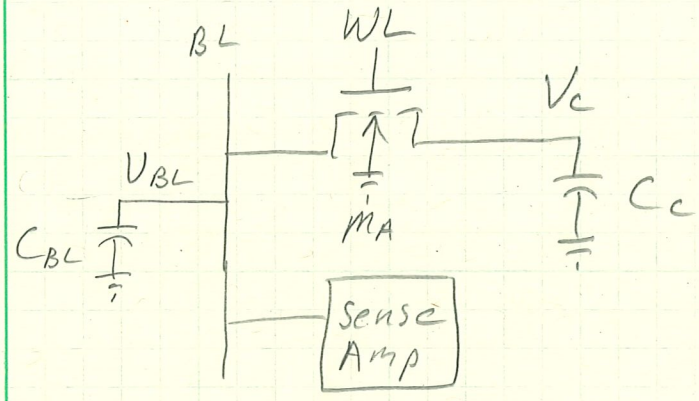
$\therefore V_{TN} > V_{T0}$

For example, if $V_{DD} = 3V$, $V_c\big|_{final} \approx 1.8V$ {Textbook p. 426}

Notice that $V_c\big|_{final}$ is not much above $\frac{V_{DD}}{2}$!

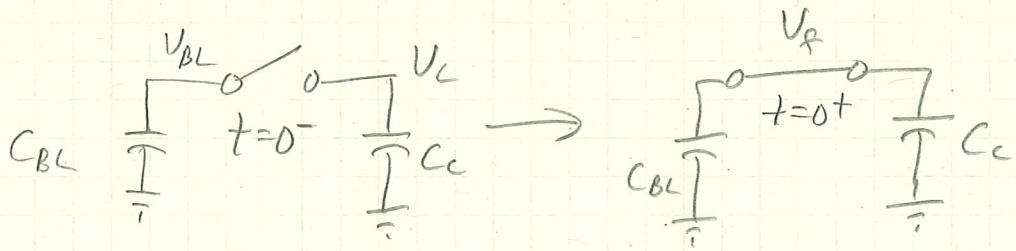
Also, Q will leak in or out of C_c over time, changing V_c when M_A is off

a. DRAM 1T-Cell Read Operation



To do a read, V_{BL} is placed on BL and $WL \rightarrow V_{DD}$. Then the voltage on V_{BL}, V_f, is read by the Sense Amplifier

How does this work?



charge is conserved

$\therefore Q_1 = V_{BL} C_{BL}$ and $Q_2 = V_c C_c$ at $t = 0^-$

and at $t = 0^+$: $Q = Q_1 + Q_2 = V_f C_{BL} + V_f C_c = V_f (C_{BL} + C_c)$

$$\therefore V_f = \frac{Q}{C_{BL} + C_c} = \frac{Q_1 + Q_2}{C_{BL} + C_c} = \frac{V_{BL} C_{BL} + V_c C_c}{C_{BL} + C_c}$$

The Sense Amp will detect a change in the voltage on BL: $\Delta V = V_{BL} - V_f$

If $\Delta V > 0$, a "1" is stored

If $\Delta V < 0$, a "0" is stored

$$\Delta V = V_F - V_{BL} = \frac{C_{BL}V_{BL} + C_c V_c}{C_{BL} + C_c} - V_{BL}$$

$$= \frac{C_{BL}V_{BL} + C_c V_c}{C_{BL} + C_c} - \frac{V_{BL}(C_{BL} + C_c)}{C_{BL} + C_c}$$

$$= \frac{C_c(V_c - V_{BL})}{C_{BL} + C_c}$$

$$= \frac{V_c - V_{BL}}{\frac{C_{BL}}{C_c} + 1}$$

However, $C_{BL} >> C_c$ {due to many cells on BL line}

$\therefore$ ΔV is very small

and $V_F \approx V_{BL}$

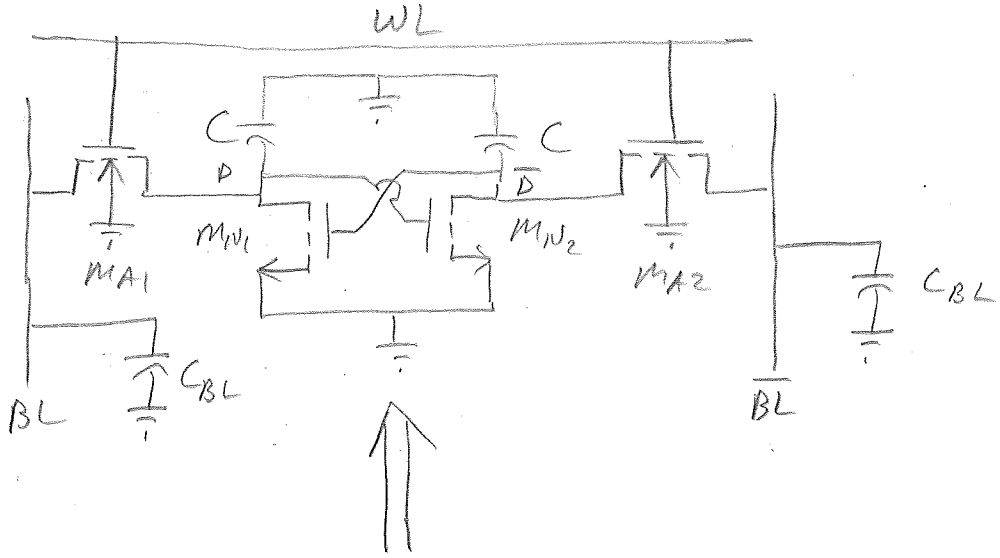
<u>Results</u>: (1) Sense Amp has to accurately detect ΔV.

(2) V_c gets destroyed each read cycle, requiring the data to be rewritten after each read.

(3) M_A has a non-zero Ron: it takes time for V_F to stabilize, limiting how fast the cell can be read.

2. DRAM 4-T Cell

Sort of a hybrid between the 6-T SRAM cell and the 1-T DRAM cell



PMOS T's in 6-Cell replaced with capacitors C and C

Each data bit is stored as D and $\bar{D}$: 1 & 0 or 0 & 1.

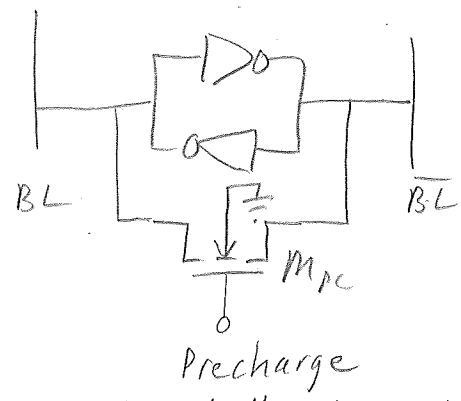
BL and $\overline{BL}$ give differential voltages for the Sense Amp to work with → reduces Sense Amp requirements.

M_{N1} and M_{N2} provide high current for sensing, compared to the 1-T cell, and decrease write times

Similar read and write operations as with 6-T cell.

3. Sense Amplifiers

The simplest Sense Amp. is the 2-invertor latch with a precharge transistor:



When Precharge is "1", M_{pc} is on and shorts out two inverters, forcing $V_{BL} \approx V_{\overline{BL}} \approx V_{trip}$

If the two inverters are symmetrical, $V_{trip} \approx \frac{V_{DD}}{2}$

For a Read Operation:

1. Precharge set to "1"
2. V_{BL} and $V_{\overline{BL}}$ equalize to approx V_{trip} of the inv's
3. Precharge is turned off and WL is set high
4. The memory cell's contents cause a small imbalance in BL and $\overline{BL}$
5. Positive feedback in the 2-inv. latch drives BL and $\overline{BL}$ to fully opposite states: 1+0 or 0+1

→ Other Sense Amp circuits exist