1) <u>RAM Capacity</u> : N - address lines and m - bit wide data

Storage Capacity $= m\,2^N$

Example : $N=8$, $m=8$

$m2^N = 2048$ bits $= 2$ Kbits of memory

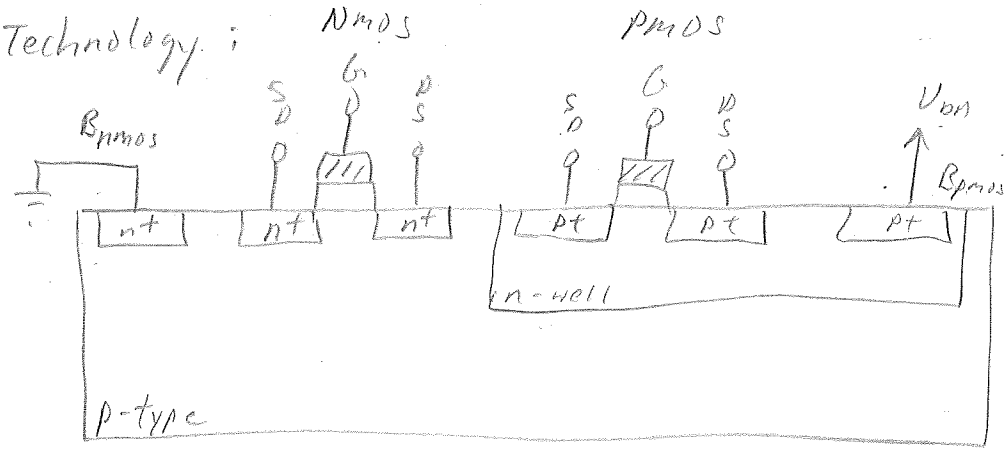
2) <u>Decoder Architecture Comparison</u>

# inputs	NAND Logic Circuit # T's	Tran. NAND-Equivalent # T's
2	$4 + 4(4) + 4(2) = 28$	$2(4) + 4 + 4(2) + 4(2) = 28$
3	$6 + 8(6) + 8(2) = 70$	$3(4) + 8 + 8(3) + 8(2) = 60$
4	$8 + 16(8) + 16(2) = 168$	$4(4) + 16 + 16(4) + 16(2) = 128$
5	$10 + 32(10) + 32(2) = 394$	$5(4) + 32 + 32(5) + 32(2) = 276$

As N increases, the transistor NAND-Equivalent Decoder requires a lot fewer T's than the NAND Logic Circuit Decoder

Bidirectional Operation of the MOSFET

CMOS Technology:

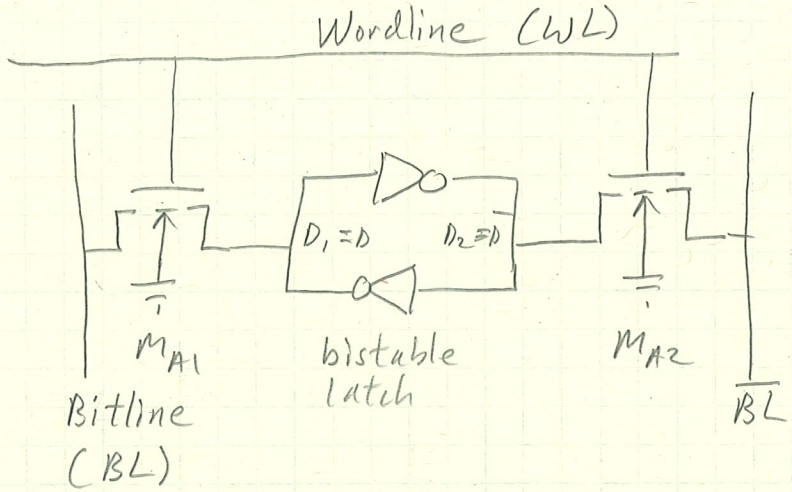


With the Body contacts properly connected: $B_p \to 0V$, $B_n \to V_{DD}$
current can flow either way between non-bate NMOS & PMOS terminals for $0V \le V \le V_{DD}$.
Relative votages determine which is S and D.

<u>Note</u>: Body effect increases V_{TN} and $|V_{Tp}|$ if S is not connected to same voltage as B for that transistor

→ This is used in Read and Write operations with memory cells

Standard SRAM Memory Cell → 6-T Cell



M_{A1} & M_{A2} → NMOS T's → used as low R switches

D = stored data value

stored 0 (D=0) : $D_1 = 0$, $D_2 = 1$

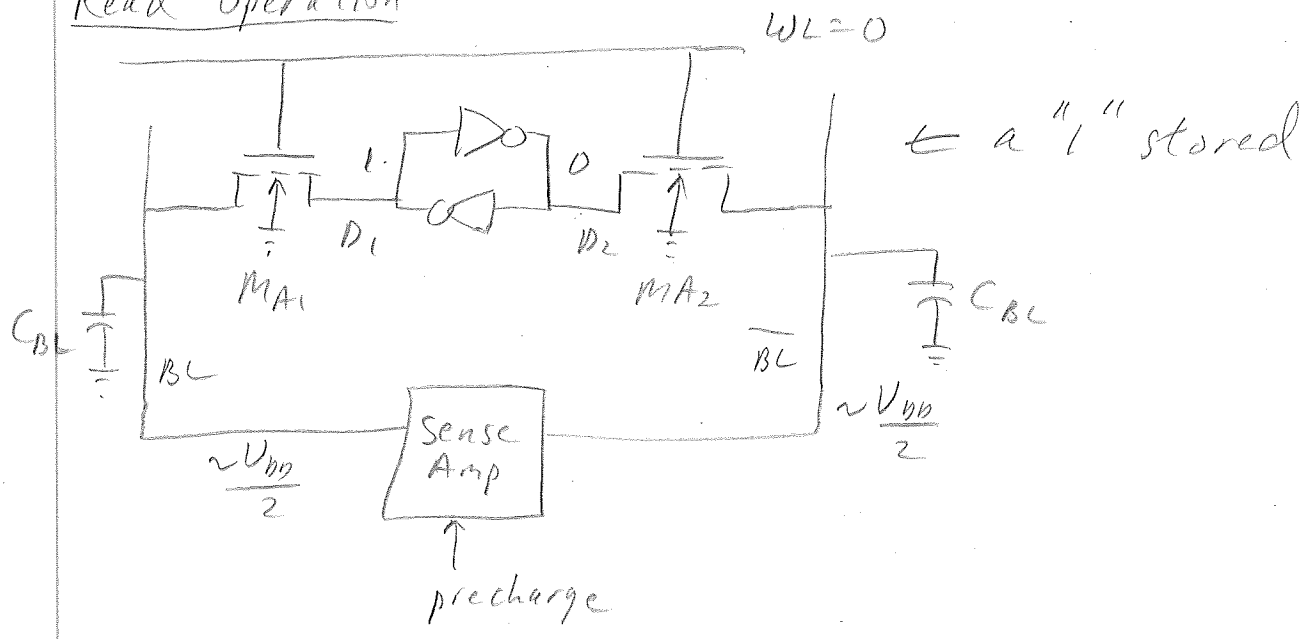
stored 1 (D=1) : $D_1 = 1$, $D_2 = 0$

WL=0 → bistable latch unaffected

WL=1 → M_{A1} & M_{A2} on → connects bistable latch to BL and $\overline{BL}$ to read the value stored in the bistable latch or to write a value (1 or 0) to it.

M_{A1} and M_{A2} take advantage of the bidirectional operation of MOSFETs

Read Operation



With WL off (WL=0), BL + $\overline{BL}$ charged up to approximately $V_{DD}/2$.

C_{BL} → parasitic capacitance on the BL + $\overline{BL}$ line

→ when WL goes high : $D_1 = V_{DD}$ pulls BL higher, and $D_2 = 0V$ pulls $\overline{BL}$ lower.

→ The sense Amp detects this and amplifies the effect → pushing BL → V_{DD} and $\overline{BL}$ → GND

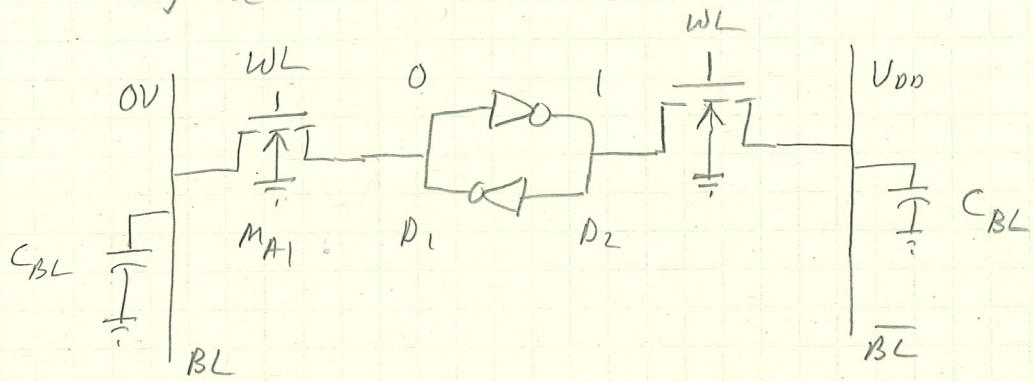
→ The oposite happens when a "0" is stored

→ The result is detected as a stored "1" or "0" by the Sense Amp

→ Since neither side of the bistable latch experiences it's voltage crossing V_{trip}, the stored state does not change

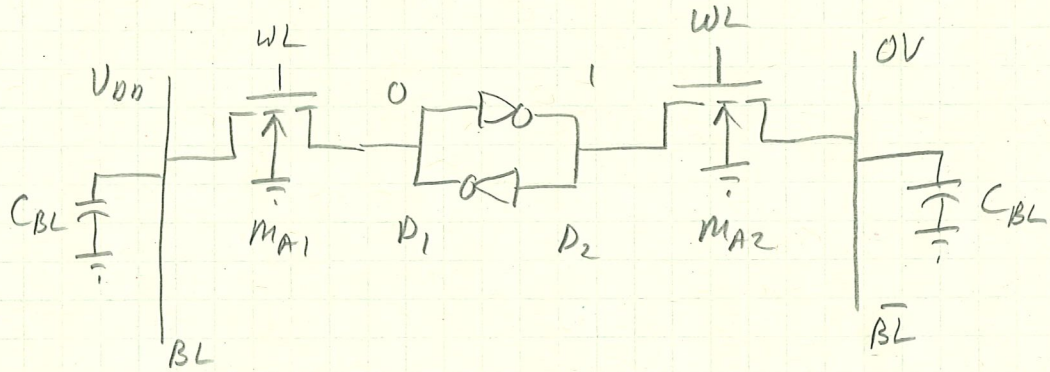
Write Operation

Writing a "0" to a stored "0"



When $WL \rightarrow V_{DD}$, M_{A1} and M_{A2} turn on. But since $BL = D_1 = 0V$ and $\overline{BL} = D_2 = V_{DD}$, no change to the Bistable Latch occurs

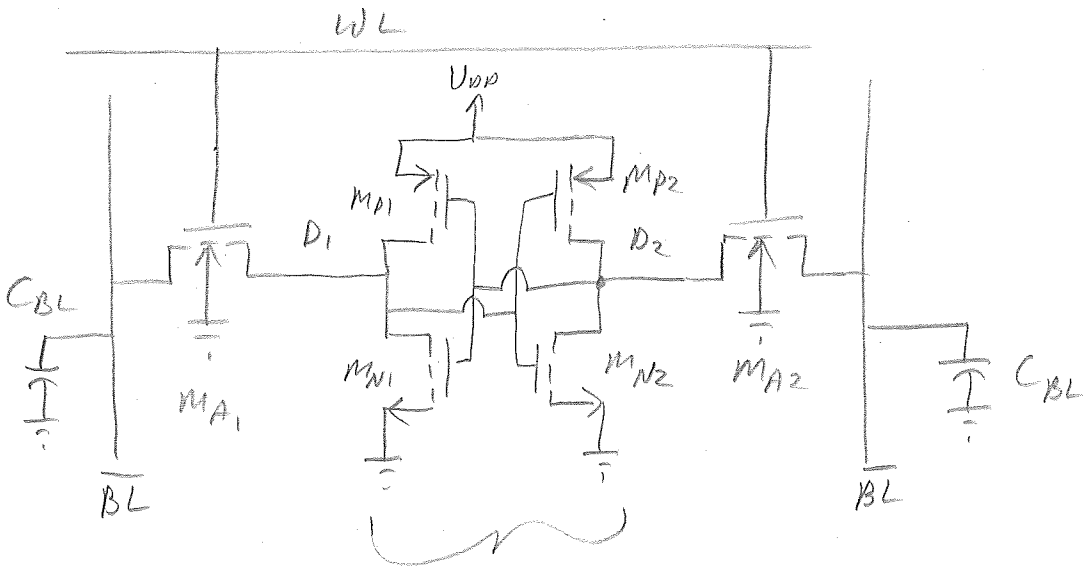
Writing a "1" to a stored "0"



When $WL \rightarrow V_{DD}$ and M_{A1} and M_{A2} turn on, D_1 is connected to BL at V_{DD} and D_2 is connected to $\overline{BL}$ at 0V. This is enough to cause the voltages at D_1 and D_2 to cross the inverter trip voltages. Then positive feedback in the bistable latch moves D_1 to V_{DD} and D_2 to 0V.

The opposite happens when writing a "0" to the bistable latch with a previously stored "1"

Transistor Schematic of the 6-T Cell



Bistable Latch

Observe cross-coupled connections

In steady state: M_{N1} and M_{P2} on and M_{P1} and M_{N2} off

<u>or</u> M_{N1} and M_{P2} off and M_{P1} and M_{N2} on