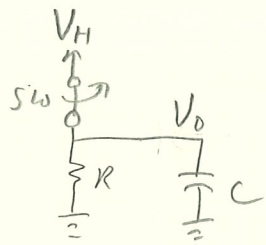
1) More on propagation delay in a CMOS logic gate

$\tau_{PLH} \rightarrow$ propagation delay : low to high

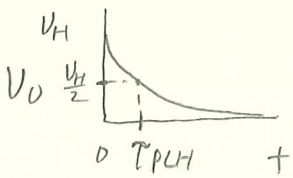
↳ from when $V_{in} = 50\% V_H$ until $V_O = 50\% V_L$

Simple Model :



SW opens at $t=0$

$t \leq 0 : V_O = V_H$



$$V_O = V_H e^{-t/RC}$$

or $0.5 V_H = V_H (e^{-\tau_{PHL}/RC})$

$$0.5 = e^{-\tau_{PHL}/RC}$$

$$\tau_{PHL} = -RC \ln(0.5) = 0.69 RC$$

If $\tau_{PHL} = \tau_{PLH} \rightarrow \tau_p = 0.69 RC$

a. <u>Rise and Fall Time</u>

t_f = time for $V_O = 0.9 V_H$ until $V_O = 0.1 V_H$, t_r is the opposite

$\therefore 0.9 V_H = V_H (e^{-t_{90\%}/RC})$ (1)

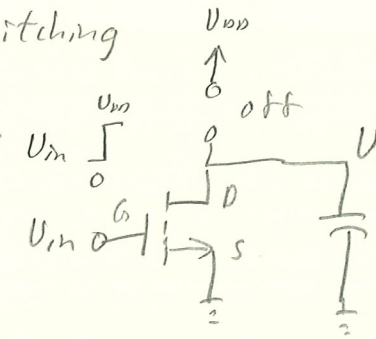
$0.1 V_H = V_H (e^{-t_{10\%}/RC})$ (2)

solve for $t_{90\%}$ and $t_{10\%}$

$\therefore t_f = t_{90\%} - t_{10\%} = 2.2 RC$

For CMOS Inverter switching

at $t=0$: V_{in}



$V_O = V_H$ at $t=0$

at $t=0$: $V_{DS} = V_H$, $V_{GS} = V_H - V_{TN}$

$\therefore$ nmos in saturation

As $V_O \to 0$: NMOS goes into triode region

$\therefore$ R_{nmos} varies as $V_O \to 0$

$\therefore$ model R_{nmos} as $R_{eff} \approx 1.7 R_{on}$

where $R_{on_N} = \dfrac{1}{K_n(V_H - V_{TN})}$ $\Rightarrow$ derived for Triode region

For a symmetrical inverter: $R_{on_p} \approx R_{on_N}$

where $R_{on_p} = \dfrac{1}{K_p|V_{GS} - V_{TP}|}$

$$\therefore \tau_{PHL} = \tau_{PLH} = 0.69 R_{eff} C = \tau_p$$
$$= 0.69(1.7) R_{on_N} C$$
$$\approx 1.2 R_{on_N} C$$
$$\approx \frac{1.2 C}{K_n(V_H - V_{TN})}$$

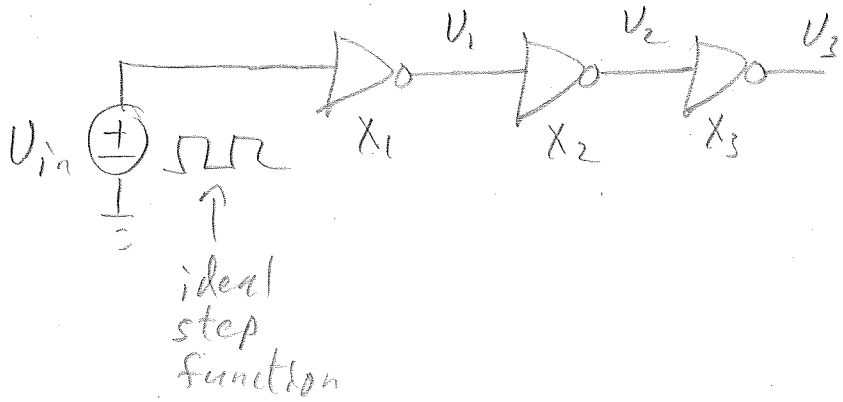
$\therefore$ τ_p for symmetrical inverter:

$$\tau_p \approx \frac{1.2C}{K_n(V_H - V_{TN})}$$

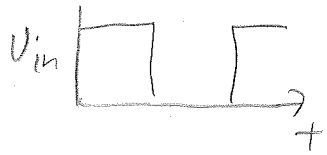
ex: $C = 1pF$, $K_n = 1mA/V^2$, $V_H = 5V$, $V_{TN} = 1V$

$\rightarrow \tau_p \approx 0.3ns$

Driving a chain of inverters (identical & symmetric)



The delay to V_1 is $\tau_p \approx \frac{1.2C}{K_n(V_H - V_{TN})} = 1.2CR_{on}$



$\rightarrow f(t) = 1 \;:\; \mathcal{L}[f(t)] = \frac{1}{s}$

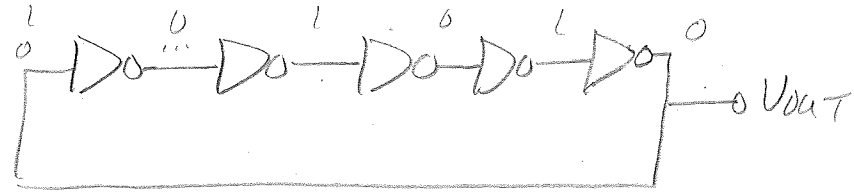
$\rightarrow f(t) = 1 - e^{-at} \rightarrow \mathcal{L}[f(t)] = \frac{1}{s} - \frac{1}{s+a}$

Notice V_1 driving X_2 is <u>not</u> an ideal step function

→ This increases the delay through $X_2, X_3, \ldots$

→ This approximately doubles the delay through each subsequent inverter → $\tau_p \approx 2.4CR_{on}$ there

Consider the Ring Oscillator, consisting of a loop of an odd number, N, of inverters where $N \geq 3$



Unstable → oscillates

oscillation period, T, $T = 2N\tau_p = 2N(2.4CR_{on})$

and $f = \frac{1}{T} = \frac{1}{2N(2.4CR_{on})}$

If N is big, V_{OUT} approaches a squarewave

If N is small, V_{out} is more of a distorted sinewave with a $0.5V_{DD}$ bias

Consider a symmetrical inverter with $L_p = L_n$

$$CR_{on} \approx \frac{C_{ox}'' WL}{\mu_n C_{ox}''(\frac{W}{L})(V_{DD} - V_{TN})} = \frac{L^2}{\mu_n (V_{DD} - V_{TN})}$$

and $f = \frac{\mu_n (V_{DD} - V_{TN})}{4.8 N L^2}$

The PCB designer can choose V_{DD} (some choice) and N
The IC desiger can choose V_{DD}, N, and L
} to set f

Uses: (1) Generating a clock signal on chip
(2) Evaluating an IC process
(3) Monitoring V_{DD}, such as for battery operated systems