

Symmetric CMOS Inverter

→ book derives equations for Noise Margin

$$NM_H = \frac{V_{DD} - V_{TN} - 3V_{TP}}{4}$$

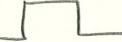
$$NM_L = \frac{V_{DD} + 3V_{TN} + V_{TP}}{4}$$

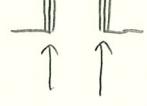
for $V_{DD} = +2.5V$, $V_{TN} = +0.6V$, $V_{TP} = -0.6V$

$$NM_H = NM_L = 0.93V$$

∴ the device can tolerate a noise voltage up to 0.93V on top of our desired signal and still generate the correct output signal

2. Jitter - "noise" - unwanted variation in switching time

ideal: 

with jitter: 

pulse train: pulse width / switching time
varies from pulse to pulse

→ another type of noise encountered in digital systems

→ may or may not be important

$$K_R = \frac{K_n}{K_p}$$

Note: For the case where

$K_n = K_p$. see Fig 7.9, p. 366

otherwise

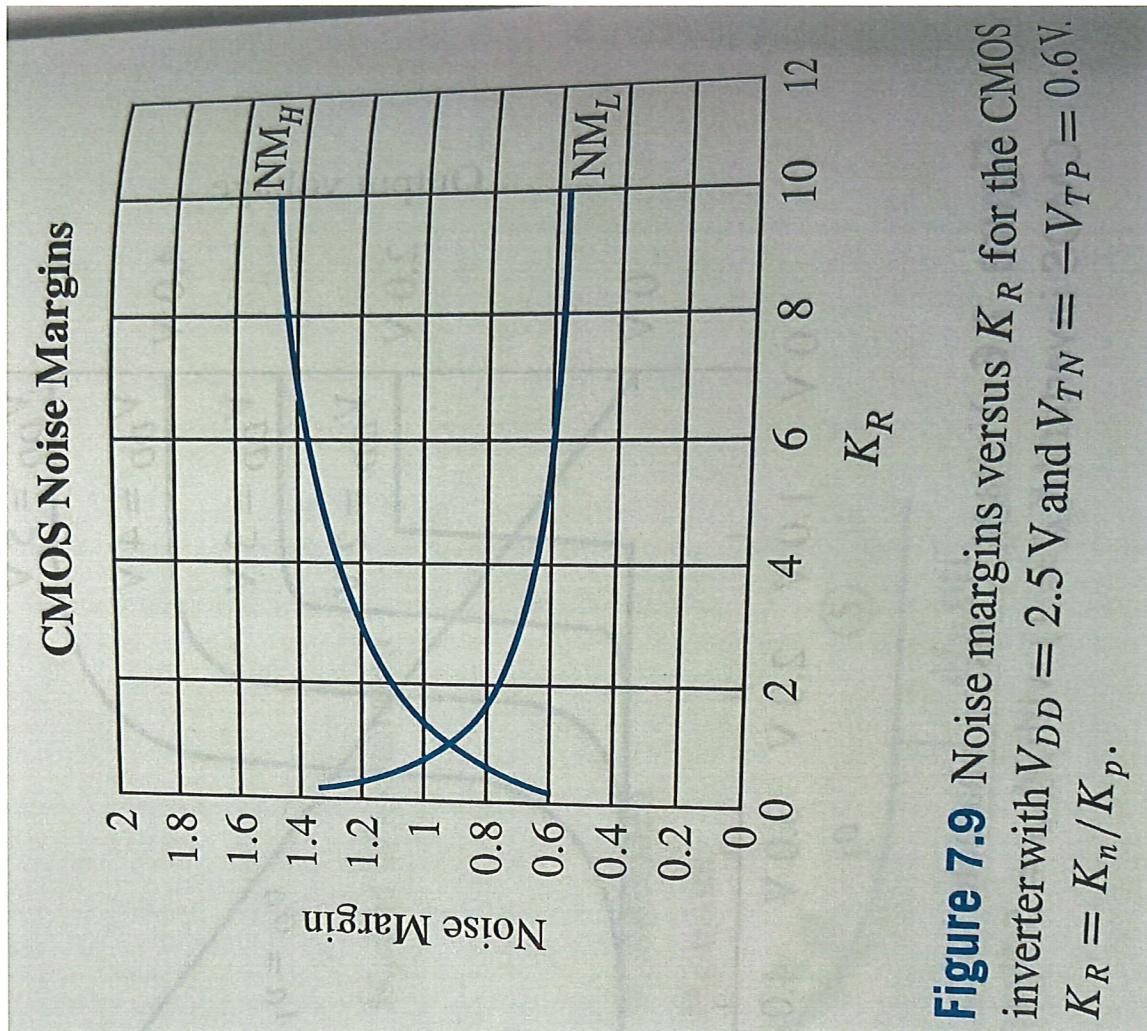
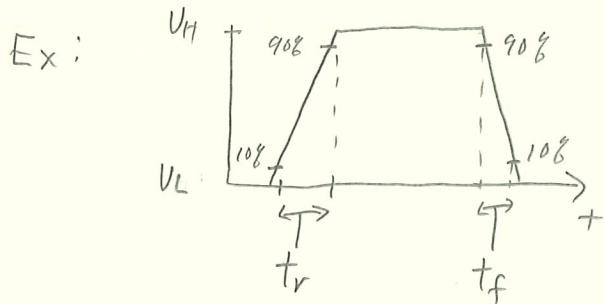


Figure 7.9 Noise margins versus K_R for the CMOS inverter with $V_{DD} = 2.5\text{ V}$ and $V_{TN} = -V_{TP} = 0.6\text{ V}$.
 $K_R = K_n/K_p$.

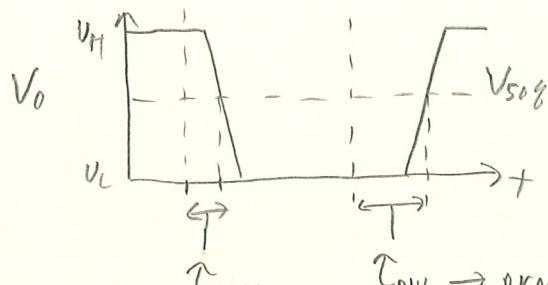
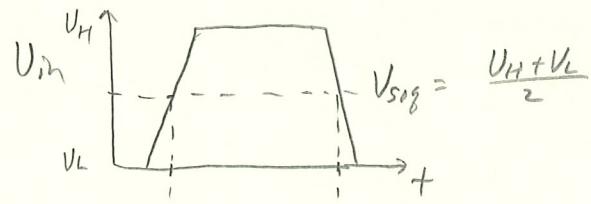
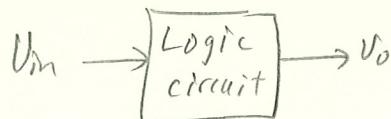
2. Rise and Fall Times

t_r = rise time : time required for signal to transition from 10% to 90% point

t_f = fall time : time required for 90% to 10% transition



a) Propagation Delay

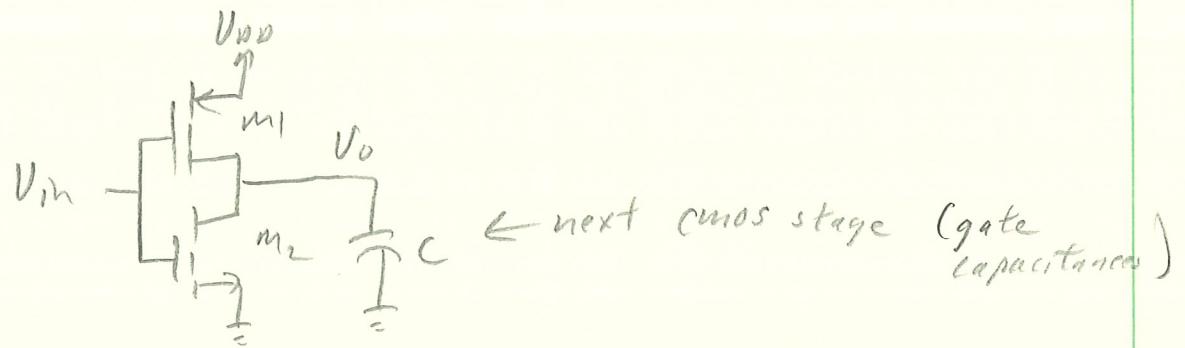


τ_{PLH} \rightarrow propagation delay : high to low

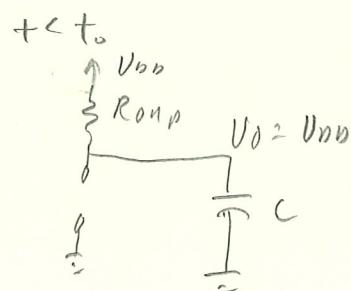
$\tau_{propagation\ delay}$: low to high

$$\text{Propagation Delay} = \tau_p = \frac{\tau_{PLH} + \tau_{PHL}}{2}$$

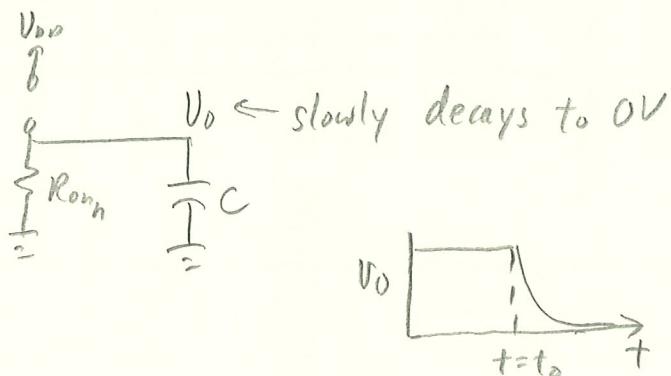
inverter



if V_{in} is 0V and switches to +5V at $t = t_0$



$+ \geq t_0$



$$R_{on} = \frac{1}{k(V_{ds} - V_T)}$$

note: R_{on} approximates R for the RC circuit

for $T \rightarrow k^2 C' \left(\frac{w}{l}\right) \rightarrow \left(\frac{w}{l}\right)^2 \downarrow, R_{on} \downarrow, \text{RC time const} \downarrow$

\therefore bigger $T \rightarrow$ smaller propagation delay

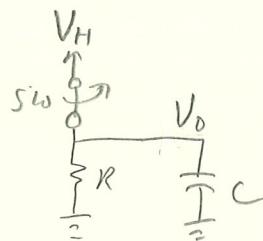
but, bigger $\frac{w}{l} \rightarrow$ gate cap in next stage goes up too

1) More on propagation delay in a CMOS logic gate

$\tau_{PLH} \rightarrow$ propagation delay : low to high

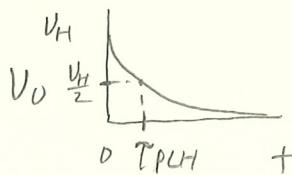
\hookrightarrow from when $V_o = 50\% V_H$ until $V_o = 50\% V_L$

Simple Model :



SW opens at $t=0$

$$t \leq 0: V_o = V_H$$



$$V_o = V_H e^{-t/RC}$$

$$\text{or } 0.5V_H = V_H(1 - e^{-T_{PLH}/RC})$$

$$0.5 = 1 - e^{-T_{PLH}/RC}$$

$$T_{PLH} = -RC \ln(0.5) = 0.69RC$$

$$\text{If } T_{PLH} = \tau_{PLH} \rightarrow \tau_p = 0.69RC$$

a. Rise and Fall Time

$t_f =$ time for $V_o = 0.9V_H$ until $V_o = 0.1V_H$

$$\therefore 0.9V_H = V_H(1 - e^{-t_{90\%}/RC}) \quad (1)$$

$$0.1V_H = V_H(1 - e^{-t_{10\%}/RC}) \quad (2)$$

solve for $t_{90\%}$ and $t_{10\%}$

$$\therefore t_f = t_{90\%} - t_{10\%} = 2.2RC$$