

Typical CMOS Transistor Parameters (Table 7.1, p. 361)

<u>Parameter</u>	<u>NMOS</u>	<u>PMOS</u>
V_{TO}	0.6V	-0.6V
γ	$0.5V^{1/2}$	$0.75V^{1/2}$
$2\phi_F$	0.6V	0.7V
K'	$100\mu A/V^2$	$40\mu A/V^2$

Note: $V_{TN} = V_{TON} + \gamma_N (\sqrt{V_{SBN} + 2\phi_{FN}} - \sqrt{2\phi_{FN}})$ } Body effect
 $V_{TP} = V_{TOP} - \gamma_p (\sqrt{V_{SBP} + 2\phi_{FP}} - \sqrt{2\phi_{FP}})$ }

if $V_{SB} = 0 \rightarrow$ PMOS S+B $\rightarrow V_{DD}$, NMOS S+B \rightarrow gnd

then $V_{TN} = V_{TON}$

$V_{TP} = V_{TOP}$

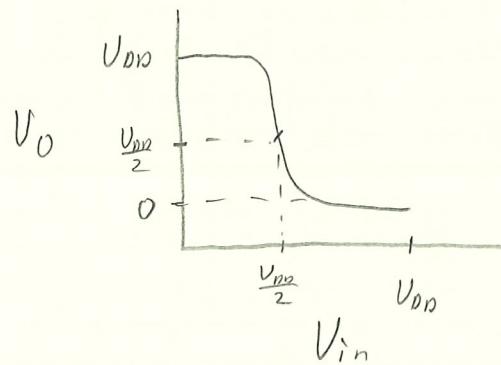
Note: $k'_n \approx 2.5k'_p$

$K_n = \mu_n C_{ox}''$ and $K_p = \mu_p C_{ox}''$

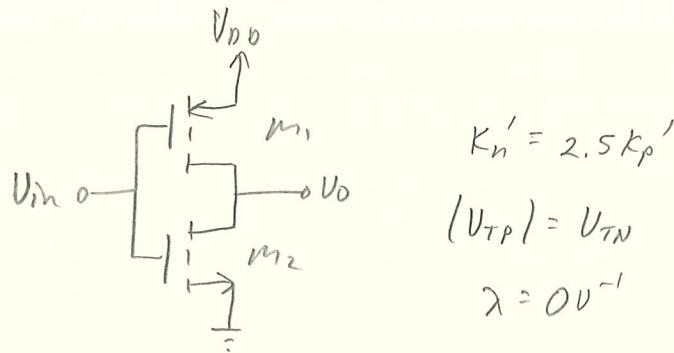
$\mu_n \approx 2.5\mu_p$

because e⁻ mobility > hole mobility

For a symmetrical inverter: $V_{trip} = \frac{V_{DD}}{2}$



at V_{trip} : $V_{in} = V_o$



$$K_n' = 2.5 k_p'$$

$$(V_{TP}) = V_{TN}$$

$$\lambda = 0 \text{ V}^{-1}$$

for symmetrical device: $V_{trip} = \frac{V_{DD}}{2}$

$$\text{at } V_{in} = V_0 \rightarrow V_{GS} = V_{DS}$$

$$|V_{DS}| \geq |V_{GS} - V_T| \geq 0 \rightarrow \text{saturation at } V_{trip}$$

$$I_D = 0.5 K' \left(\frac{w}{l}\right) (V_{GS} - V_T)^2$$

$$M_1 : I_D = 0.5 K'_p \left(\frac{w}{l}\right)_p (V_{GS1} - V_{TP})^2$$

$$M_2 : I_D = 0.5 K'_n \left(\frac{w}{l}\right)_n (V_{GS2} - V_{TN})^2$$

$$\text{note: } (V_{GS1} - V_{TP})^2 = (V_{GS2} - V_{TN})^2$$

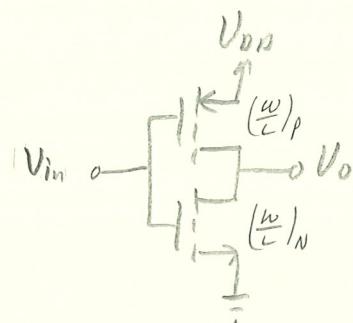
$$I_{Dm_1} = I_{Dm_2}$$

$$\therefore K'_p \left(\frac{w}{l}\right)_p = K'_n \left(\frac{w}{l}\right)_n$$

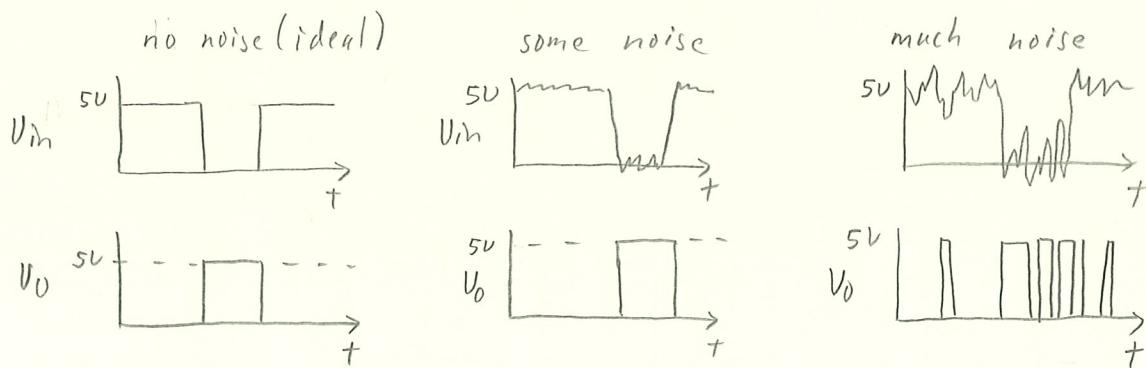
$$\frac{\left(\frac{w}{l}\right)_p}{\left(\frac{w}{l}\right)_n} = \frac{K'_n}{K'_p} = \frac{2.5}{1}$$

ex: select $w_n = 1 \mu m$, $L_n = 1 \mu m$ } results in a
 $w_p = 5 \mu m$, $L_p = 2 \mu m$ } symmetrical inverter

More on the Symmetrical CMOS inverter

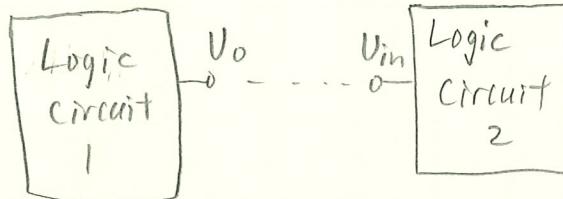


II Noise Margins in CMOS logic devices



Noise margin \rightarrow acceptable range of voltage variation on V_{in}
while still getting to correct V_o

Definition:



$$NM_H = V_{O_{H1}} - V_{I_{H2}}$$

$\uparrow_{\min \text{ high}}$ $\uparrow_{\text{min high input voltage}}$
 high
 output voltage

$$NM_L = V_{I_{L2}} - V_{O_{L1}}$$

$\uparrow_{\max \text{ input}}$ $\uparrow_{\text{max low output voltage}}$
 low
 voltage

Noise \rightarrow adds to our "desired" electrical signal

a. Sources : (1) internal

\rightarrow noise inherent in electronics devices: thermal noise,

shot noise, 1/f noise

\rightarrow interference from other circuitry in same system

(2) external

\rightarrow Nearby electronics

- i. noise on power supply lines (power and ground lines)

ii. electromagnetic interference

\rightarrow Mechanical vibrations

\rightarrow RF: nearby by radio/TV stations, cell phones, TVs, etc.

* Dynetech RF power meter story 200kHz to 2GHz

\rightarrow solar/cosmic radiation

\rightarrow stray cap from nearby motion

* HMX2000 high R testing story

* Dump truck story

b. characteristics

\rightarrow voltage or current noise sources

\rightarrow at specific frequencies or wide bandwidth

\rightarrow random or nonrandom

\rightarrow temporary or always present