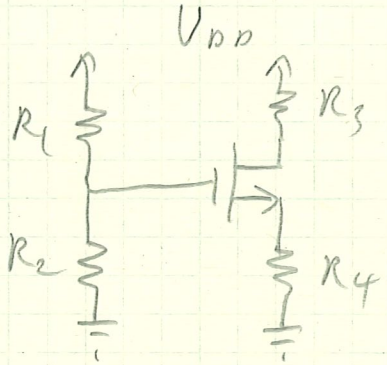
1) 4 Resistor Bias Network for NMOS (and other transistors)



Find operating point, V_{GS}, V_{DS}, I_D

① Technique 1

Since $I_G = 0$, $V_G = \frac{V_{DD} R_2}{R_1 + R_2}$

$V_D = V_{DD} - I_D R_3$ ①

$V_S = I_D R_4$ ②

Select Saturation or Triode mode and solve

Saturation : $I_D = 0.5 K_n' \left(\frac{W}{L}\right)(V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$

$I_D = 0.5 K_n' \left(\frac{W}{L}\right)(V_G - V_S - V_{TN})^2 (1 + \lambda (V_D - V_S))$ ③

Plug ① and ② into ③

solve quadratic equation for I_D if $\lambda = 0\, V^{-1}$

or cubic equation for I_D if $\lambda \neq 0\, V^{-1}$

Then use ① and ② to determine V_D and V_S

Then compute V_{GS} and V_{DS}

See if in Saturation mode

Triode : $I_D = K_n'(\frac{W}{L})(V_{GS} - V_{TN} - 0.5V_{DS})V_{DS}$

$= K_n'(\frac{W}{L})(V_G - V_{TN} - 0.5(V_D - V_S))(V_D - V_S)$ ③

Plug ① and ② into ③, and solve for I_D

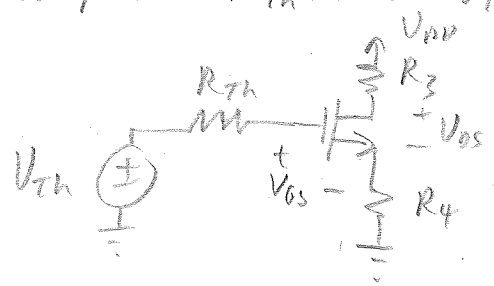
Then use ① and ② to solve for V_S and V_D

Compute V_{GS} and V_{DS}

Verify Triode mode.

2) Technique 2

Compute R_{Th} and V_{Th} at the Gate



$V_{Th} - I_G R_{Th} - V_{GS} - I_S R_4 = 0$ ①

Note : I_G pos into G, I_S pos out of S, and I_D pos into D

$V_{DD} = I_S R_4 + V_{DS} + I_D R_3$ ②

Select a mode and use and I_D EQ, with $I_G = 0$, $I_S = I_D$

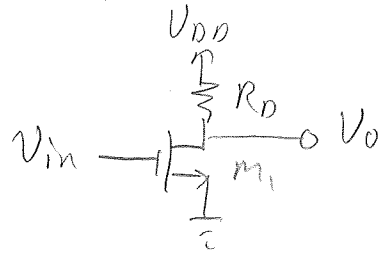
Sat: $I_D = \frac{1}{2}K_n'(\frac{W}{L})(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$ ③

Triode: $I_D = K_n'(\frac{W}{L})(V_{GS} - V_{TN} - 0.5V_{DS})V_{DS}$ ③

Plug ① and ② into ③, solve for I_D

This technique works with BJT's : $I_B \neq 0A$

2. Load resistor for NMOS inverter



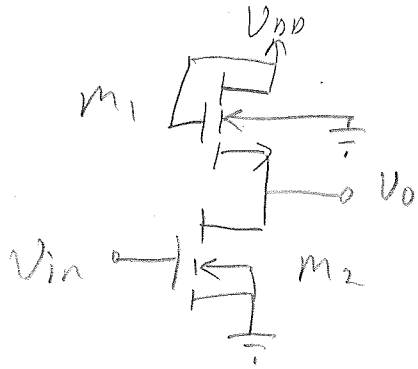
For discrete circuits, not a problem

But for IC implementations, realizing R is problematic

If $R \approx 20-30\,K\Omega$, R could be 1000 larger than NMOS Transistor

$\therefore$ Other options are needed.

a. Consider this:



M_1 is a load

For M_1: $V_{GS} = V_{DS} \rightarrow \therefore$ in Saturation

However, $V_{SB} \neq 0V$

$$\therefore V_{TN_{M_1}} = V_{TNL} = V_{T0} + \underbrace{\gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)}_{\text{due to body effect}}$$

$$I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right)(V_{GS} - V_{TNL})^2 \qquad \{\text{assuming } \lambda = 0V^{-1}\}$$

here $V_{TNL} > V_{TN}$

When $V_{in} = 0V$, M_2 is off. How high is V_{out}?

For M_1, $V_{DS} = V_{GS} = V_{DD} - V_O$

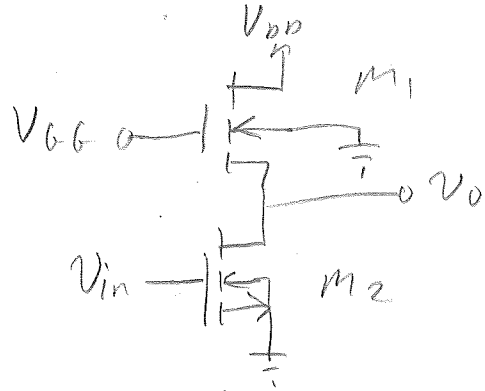
For M_1 to be on: $V_{GS} - V_{TNL} \geq 0$

$\therefore$ the limit is $V_O = V_{DD} - V_{TNL}$

$$V_{TNL} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) > V_{TN}$$

So, $V_{O_L} > 0V$ and $V_{O_H} < V_{DD}$ → a disadvantage

b. "Linear Load" Technique



For M_1: $V_{GG} \geq V_{DD} + V_{TNL}$

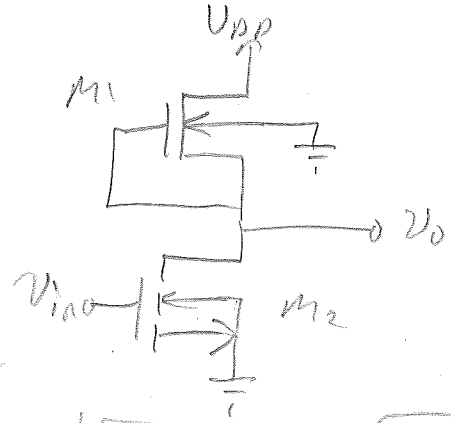
$\therefore$ M_1 does not turn off and $V_{O_H} = V_{DD}$

→ Disadvantage: 2nd power supply needed, more complicated wiring in-chip

$\therefore$ this is rarely used

c. Depletion mode NMOS for Load

↳ $V_{TN} < 0$; $v_{GS} = 0V \rightarrow I_D > 0A$



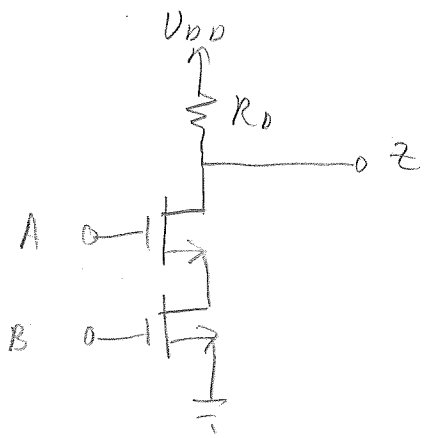
$v_{O_H} = V_{DD}$

$v_{O_L} > 0V$

negative

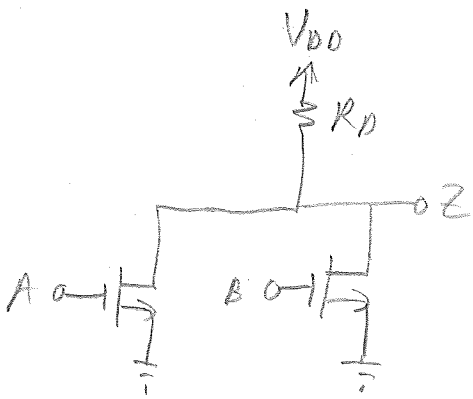
$$V_{TNL} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

3. <u>More Complex Logic Gates</u>



NAND Gate

$Z = \overline{AB}$



NOR Gate

$Z = \overline{A+B}$