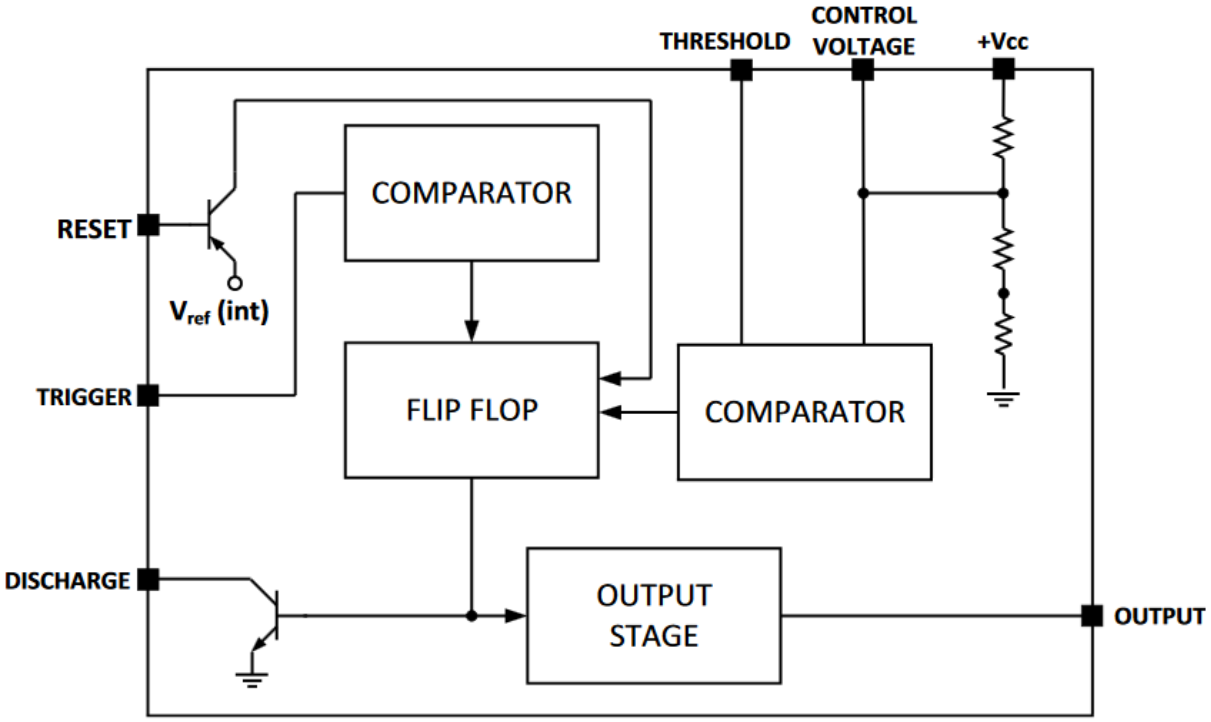
Thursday 10/2/25

555 Timer Chip

This is a very popular 8-pin IC for generating time delays and oscillating signals. The original 555 timer chip was released in 1972 by a company called Signetics, in an 8-pin DIP package and an 8-pin SIP package. Signetics (**Sig**nal **Net**work Electron**ics**) was founded in 1961, and was sold to Philips in 1975, which is now NXP.

Functional block diagram:

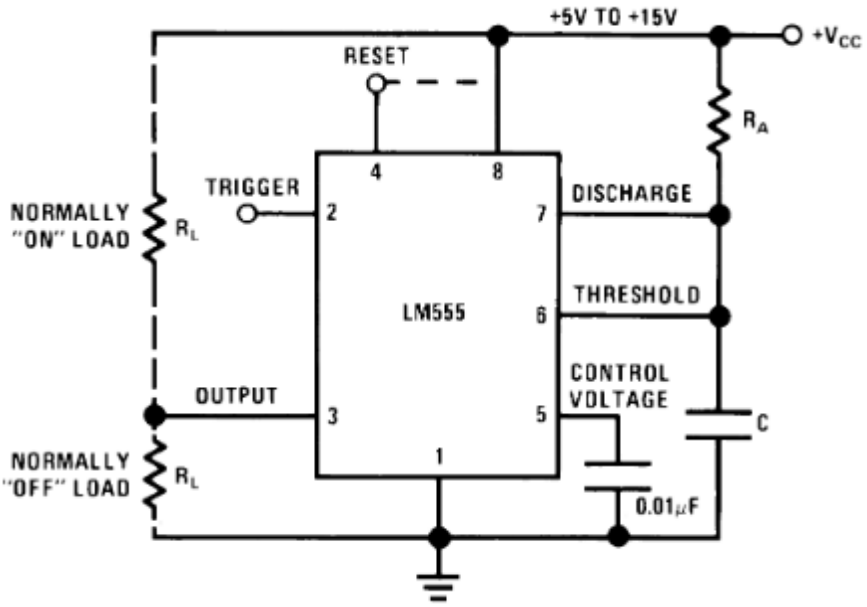


From http://www.ti.com/lit/ds/symlink/lm555.pdf, one of Texas Instruments' versions of the 555

It has two modes of operation: monostable (a one-shot), and astable (oscillating).

Monostable Mode

In the monostable mode, the output signal is a single high-level pulse (with R_L tied to ground) that you trigger, and the external passive components determine the pulse length. The pulse length can range from μs to hours.

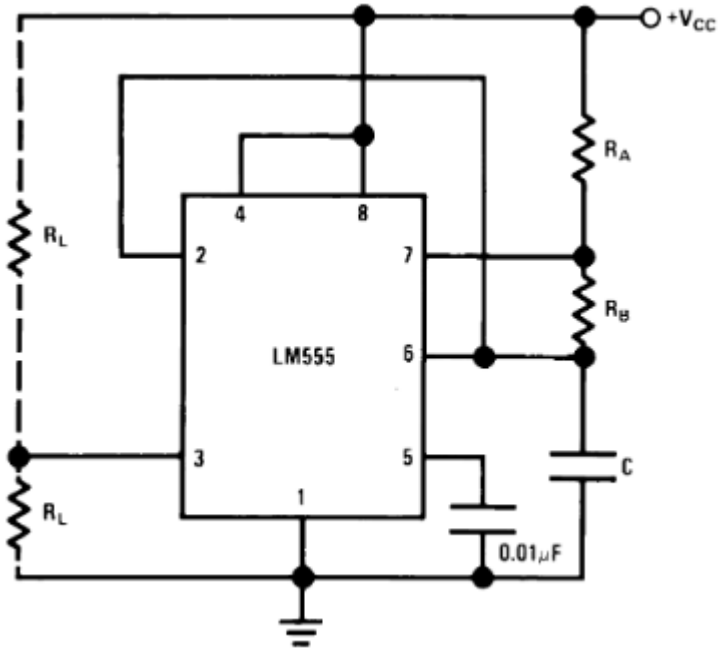


The output is initially low and the trigger input is initially high. Application of a negative going trigger pulse, less than $V_{cc}/3$, starts the process. At this time, the output goes high. When $t = 1.1R_AC$, the output goes back low and stays low until another trigger pulse is applied. The time of the pulse length is due to the voltage across C growing exponentially through R_A.

With R_L tied to ground, the pulse "turns on" the load for the duration of the pulse. For R_L tied to V_{cc}, the pulse "turns off" the load for the duration of the pulse.

Astable mode

In the astable mode of operation, the output is a pulse train. It can be a square wave, but it does not have to have a 50% duty cycle.



Capacitor C continually charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The output is high during the charge time, which is determined by $t_c = 0.693\ (R_A+R_B)C$.

The output is low during the discharge time, which is determined by $t_d = 0.693R_BC$.

Therefore, the oscillation period, T, is $T = t_c+t_d$, and

$$f = \frac{1}{T} = \frac{1.44}{C(R_A + 2R_B)}$$

Pin 3 is the output pin. It uses the same R_L convention as in the monostable mode.

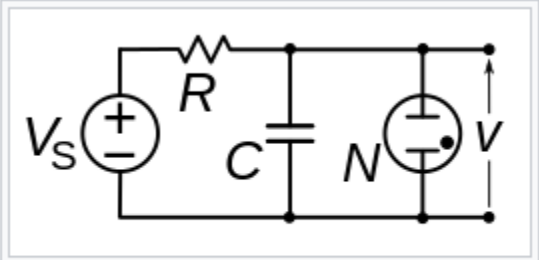
The 556 IC has two 555 timers on it.

The Pearson-Anson Effect

Discovered in 1922 by Stephen Pearson and Horatio Anson.

Some two terminal devices, including a neon lamp, maintain a high resistance between the terminals for any voltage less than a breakdown voltage, V_b. Once V_b has been reached, the resistance between the two terminals drops substantially, and remains low until the voltage across the terminals drops to some extinction voltage, V_e. With the neon lamp, dielectric breakdown occurs when V_b is reached, resulting in a low resistance plasma forming in the gas.

With this effect, a simple relaxation oscillator can be realized:



Pearson-Anson oscillator circuit

Curtesy Wikipedia

C charges through R from the DC voltage source, V_s, until V reaches V_b. Then the neon lamp, N, turns on and C quickly discharges until V reaches V_e. Then the lamp turns off and C begins to charge through R again… The output voltage, V, is a sawtooth waveform.

VCO's, DDS and PLLs

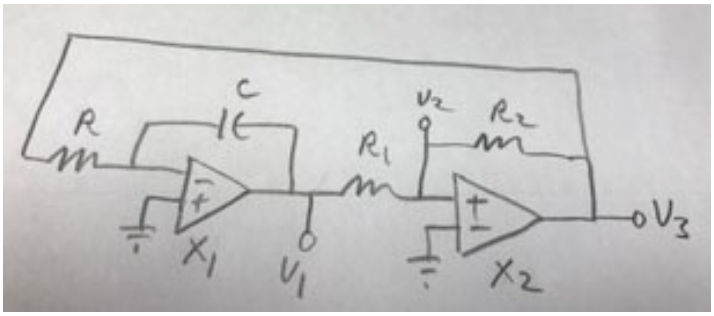
1) VCO

A VCO is a voltage controlled oscillator. How is that realized?

Most oscillators have an oscillation frequency or fundamental frequency inversely proportional to RC or the square root of LC.

One option is to use a FET as a voltage controlled resistance to affect the R in a RC time constant controlled oscillator. However, this can be problematic in an oscillator where the output signal goes positive and negative (body diode in a MOSFET, nonsymmetrical response about 0V V_{gs} in a jFET).

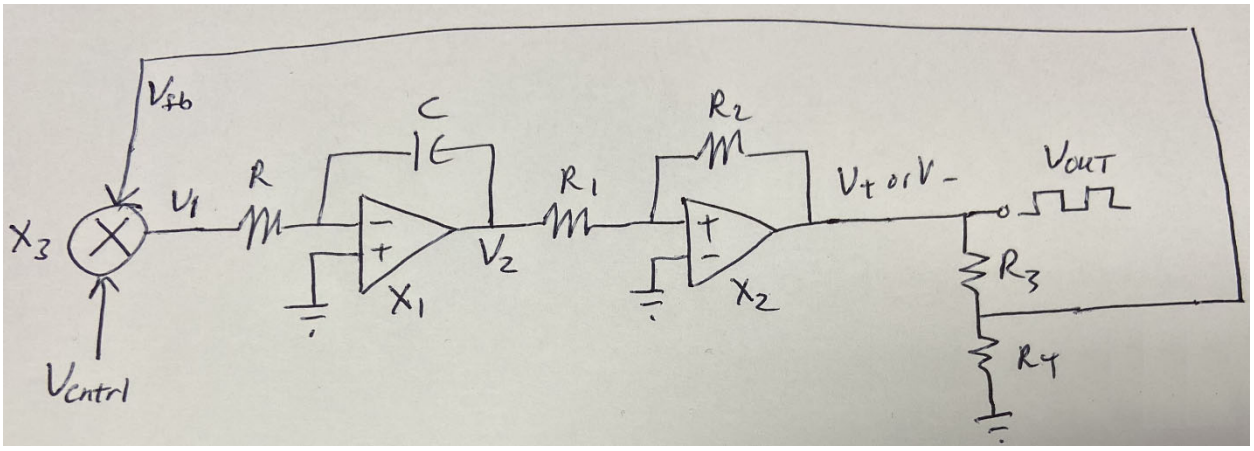
Consider again the op amp based relaxation oscillator:



V_3 is a square wave output signal. The oscillation frequency is:

$$f = \frac{1}{T} = \frac{R_2}{4R_1RC}$$

Where RC is from the integrator stage. Consider the effect of adding a four quadrant multiplier into the circuit:



V_{cntrl} is a small DC control voltage and $V_{cntrl} > 0$ V.

V_{OUT} is a square wave with voltages alternating between V+ and V-.

V_{fb} is the feedback voltage and is attenuated from V_{OUT} by the R_3:R_4 voltage divider according to:

$$V_{fb} = V_{OUT}\frac{R_4}{R_3+R_4}.$$

V_1 is the input voltage to the integrator subcircuit. X_3 is a four quadrant multiplier and its's output voltage, V_1, is the product of V_{fb} and V_{cntrl}. Assuming that V_{cntrl} changes much more slowly than the integrator's RC time constant, then

$$v_2 \approx V_{o1} - \frac{V_1}{RC}t \qquad \text{for t} \geq 0\text{s},$$

where V_{01} is the initial voltage across the capacitor at t = 0 s. From the previous analysis of the op amp relaxation oscillator:

$$0 = \left(-V_{-}\frac{R_1}{R_2} - \frac{V_1 t}{RC}\right)R_2 + V_{+}R_1,$$

which can be rewritten as:

$$t = \frac{RC}{V_1}(V_{+} - V_{-})\frac{R_1}{R_2},$$

which leads to:

$$f = \frac{1}{T} = \frac{1}{2t} = \left(\frac{V_1}{V_{+}-V_{-}}\right)\frac{R_2}{2R_1RC}.$$

Let's assume that $V_{+} = -V_{-}$, leading to:

$$f = \frac{1}{T} = \frac{1}{2t} = \left(\frac{V_1}{V_{+}}\right)\frac{R_2}{4R_1RC}.$$

With the op amp relaxation oscillator, $V_1 = V_{+}$, leading to:

$$f = \frac{R_2}{4R_1RC}.$$

But here,

$$V_1 = V_{cntrl}V_{fb} = V_{cntrl}V_{+}\left(\frac{R_4}{R_3+R_4}\right).$$

Therefore, for this square wave VCO:

$f = V_{cntrl}\left(\frac{R_4}{R_3+R_4}\right)\frac{R_2}{4R_1RC}$,

for V_{cntrl} a DC voltage and $V_{cntrl} > 0$ V

where f is the fundamental frequency of the V_{out} output square wave.

If V_{cntrl} is not a DC voltage, such as:

$V_{cntrl} = V_a + V_b \sin(\omega t)$,

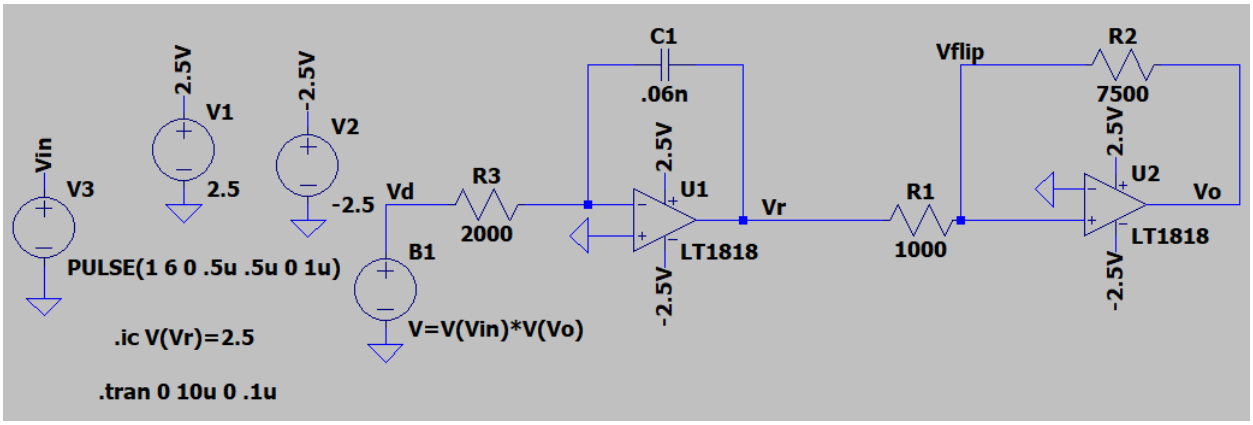
where V_a is DC and $V_a > |V_b| > 0$ V,

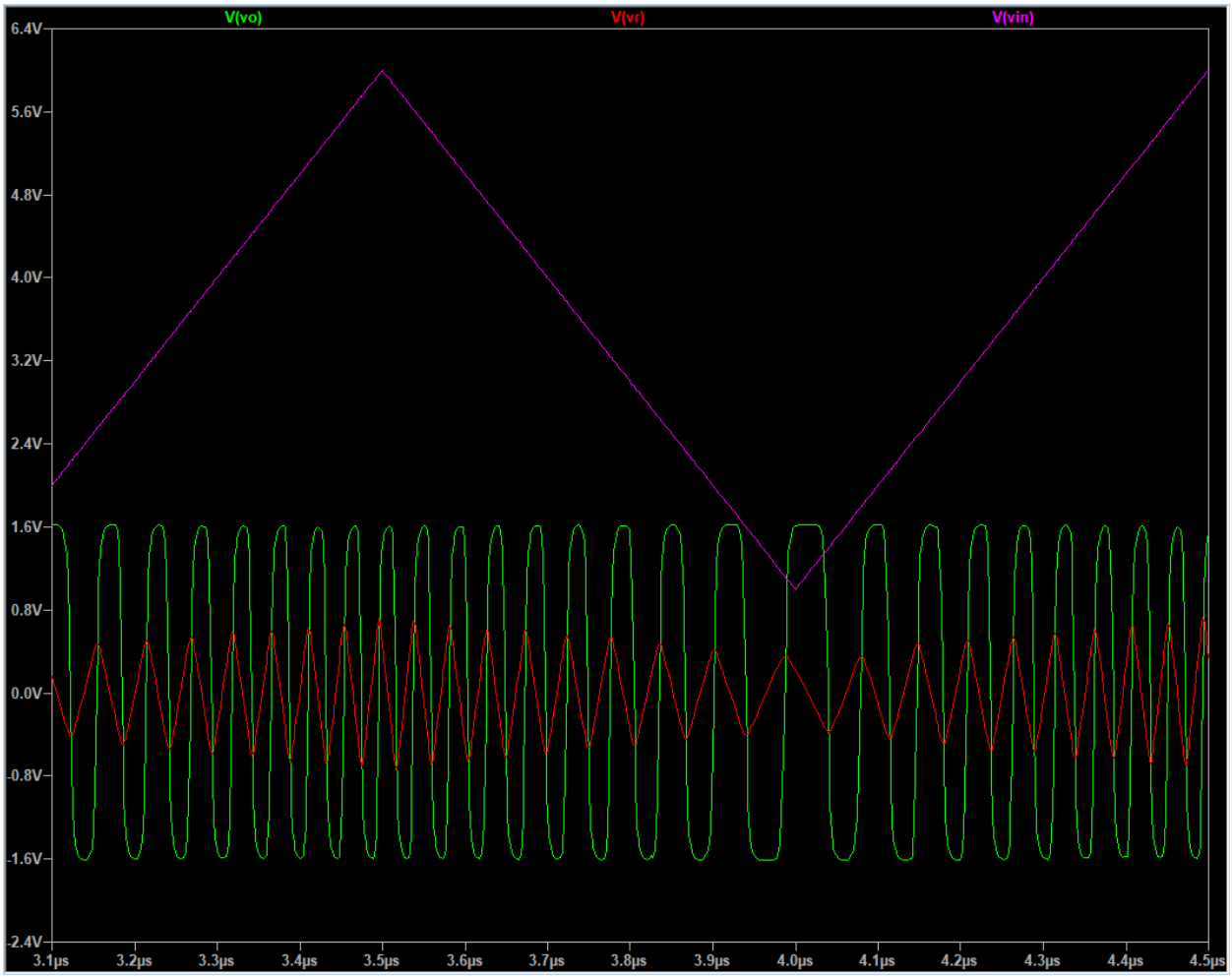
the integral of V_1 has to be recalculated and the math gets more complicated.

However, the fundamental frequency of the output square wave will change with the time varying input sinusoid and the range of f will increase in proportion to the amplitude of the input sinusoid, similar to FM.

Note, if $V_{cntrl} = 0$ V, V_{out} will be stuck at V+ or V-.

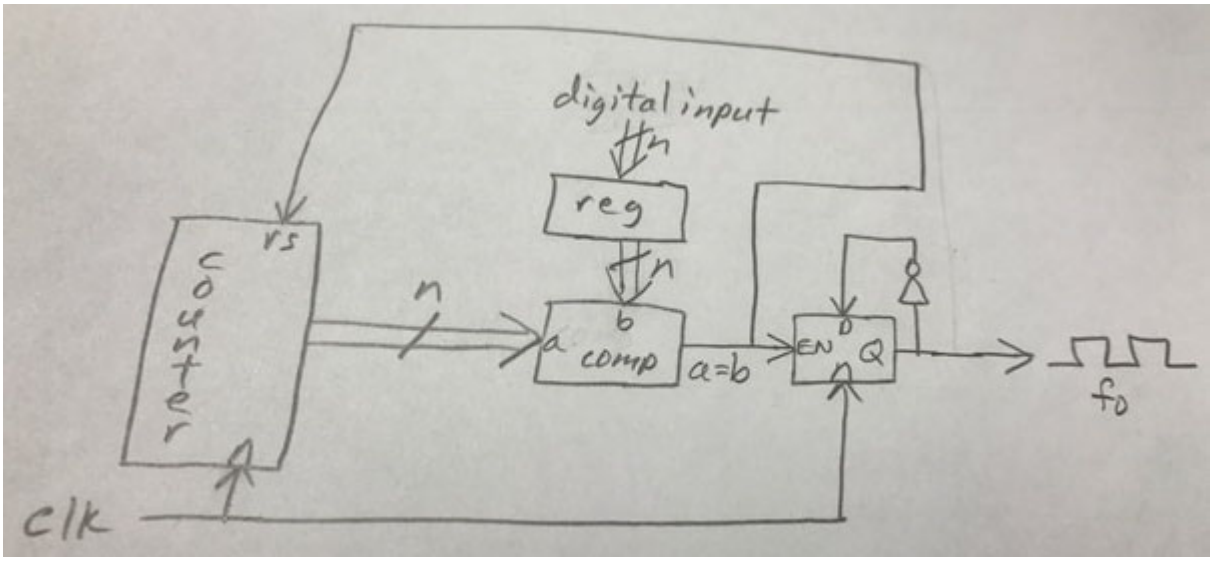
Example VCO, simulated in LTSpice





2) Digitally Controlled Oscillator

A variable frequency square wave can also be created by dividing down the frequency of a high frequency clock:



Digital input range: 1 to 2^n

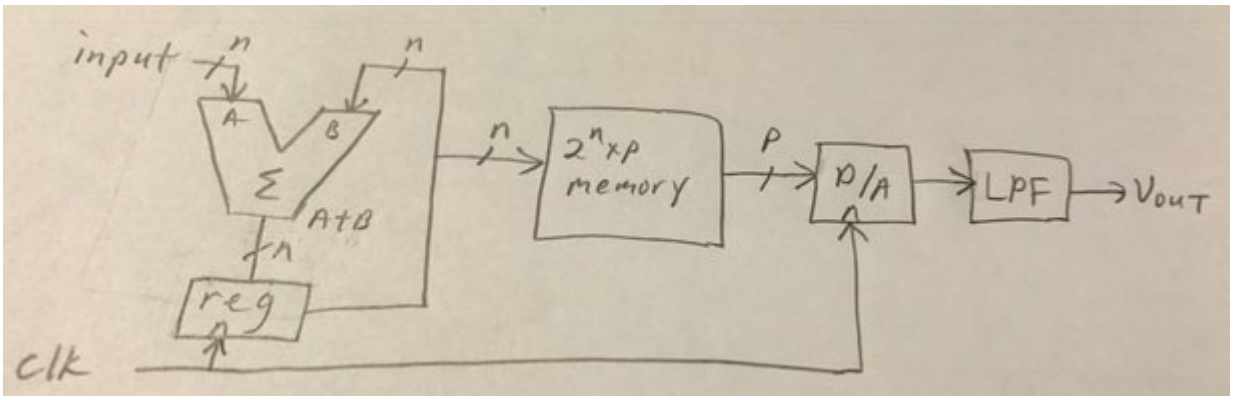
$$f_o = \frac{f_{clk}}{2(digital\ input)}$$

This digital circuit can easily be implemented in an FPGA or similar device.

An analog input signal could be run through an A/D to generate the digital input signal, thus realizing a VCO.

3) Direct Digital Synthesis (DDS)

Using a 2^nxp memory, store one cycle of a sine wave: 2^n samples [sin(2π/n)] with p-bit amplitude resolution.

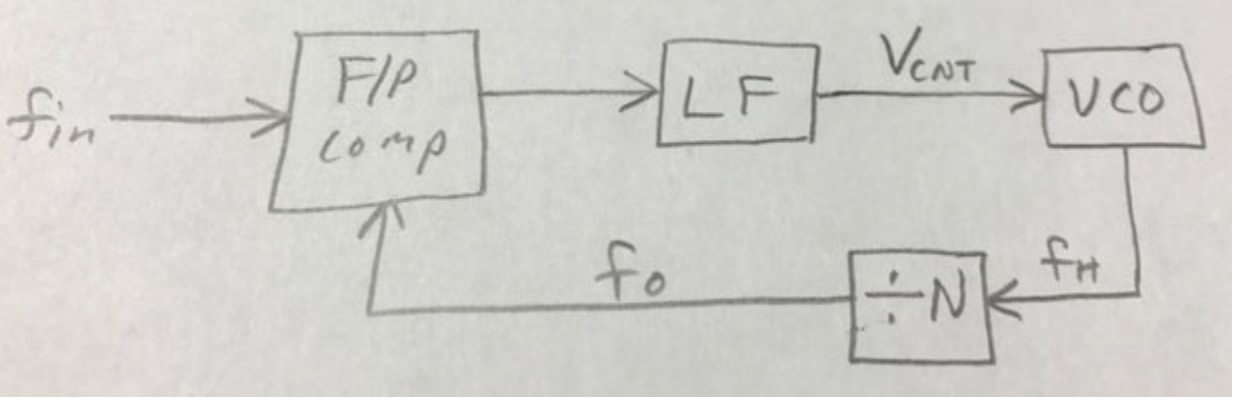


If input is 1, it takes 2^n clk cycles to go through (read out) the entire memory. The frequency of the output sinewave will then be $f_{CLK}/2^n$. As the input number increases, it takes fewer clk cycles to go through the address space of the memory, proportionally increasing the frequency of the output sinewave. The LPF is needed to reduce high frequency noise and to smooth the output sinewave. The output sinewave is directly digitally synthesized, hence the name "DDS."

Any waveform could be stored in the memory and run through the D/A and LPF to create arbitrary analog waveforms. Traditionally, high frequency versions were called a DRFM, for Digital RF Memory, and were used in radar systems.

4) Phase Locked Loops (PLL)

A PLL frequency and phase locks a voltage controlled oscillator (VCO) to an input periodic signal (sinewave or square wave).



F/P comp: frequency / phase comparator – produces a signal indicating the frequency and/or phase difference between the two input periodic signals. Implementations include four quadrant multipliers, mixers, and logic circuits.

LF: loop filter, often a lowpass filter. The output (V_{CNT}) drives the VCO. A LF may contain an integrator so that the error between f_{in} and f_o is driven to zero.

VCO: voltage controlled oscillator. The output, f_H, may be a sinewave or a square wave.

/N: "divide by N" : a digital clock divider (often a synchronous counter) is used to reduce f_H to f_o (with square wave signals). This can allow multiple frequency and phase locked clocks at different frequencies (and even phases) to be generated. This stage is not required in a PLL though.

Applications of PLLs:

(1) As a frequency synthesizer (uses the /N stage).

(2) FM demodulation. V_{CNT} is the demodulated output signal.

(3) Higher frequency clock signal generation and synchronization.

(4) Recovering a carrier or clock signal from noise, or if occasional pulses are missing.

(5) As sensor instrumentation when a measurand variable frequency oscillator is used as/with the sensor. V_{CNT} can then be proportional to the measurand.

Implementation can be all analog, analog and digital, all logic circuit based, or s/w defined with A/Ds and D/A's. They can be built at the component level or purchased as a complete system.

For a PLL, once frequency lock is achieved, it can be modeled as a linear feedback control system to lock the phase. Frequency locking a PLL is a highly nonlinear process.

FLLs (frequency locked loops) are similar and possibly a little simpler to implement, since only the frequency has to be locked between the input and output signals.

Data Sheet

ADF4377

Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Output frequency range: 800 MHz to 12.8 GHz
- Jitter = 18 fs_{RMS} (integration bandwidth: 100 Hz to 100 MHz)
- Jitter = 27 fs_{RMS} (ADC SNR method)
- Wideband noise floor: −160 dBc/Hz at 12 GHz
- PLL specifications
  - −239 dBc/Hz: normalized in-band phase noise floor
  - −147 dBc/Hz: normalized in-band 1/f noise
  - Phase detector frequency up to 500 MHz
  - Reference input frequency up to 1000 MHz
  - Typical spurious f_{PFD}: −95 dBc at f_{OUT} = 12 GHz
- Reference input to output delay specifications
  - Device-to-device standard deviation: 3 ps
  - Temperature coefficient: 0.03 ps/°C
  - Adjustment step size: < ±0.1 ps
- Multichip output phase alignment
- 3.3 V and 5 V power supplies
- 7 mm × 7 mm 48-lead LGA

APPLICATIONS

- High performance data converter and MxFE clocking
- Wireless infrastructure (MC-GSM, 5G)
- Test and measurement

GENERAL DESCRIPTION

The ADF4377 is a high performance, ultralow jitter, dual output integer-N phased locked loop (PLL) with an integrated voltage controlled oscillator (VCO) ideally suited for data converter and mixed signal front end (MxFE) clock applications. The high performance PLL has a figure of merit of −239 dBc/Hz, ultralow 1/f noise, and a high phase frequency detector (PFD) frequency that can achieve ultralow in-band noise and integrated jitter. The fundamental VCO and output divider of the ADF4377 generate frequencies from 800 MHz to 12.8 GHz. The ADF4377 integrates all necessary power supply bypass capacitors, saving board space on compact boards.

For multiple data converter and MxFE clock applications, the ADF4377 simplifies clock alignment and calibration routines required with other clock solutions by implementing the automatic reference to output synchronization feature, the matched reference to output delays across process, voltage, and temperature feature, and the less than ±0.1 ps, jitter free reference to output delay adjustment capability feature.

These features allow for predictable and precise multichip clock and system reference (SYSREF) alignment. JESD204B and JESD204C Subclass 1 solutions are supported by pairing the ADF4377 with an integrated circuit (IC) that distributes pairs of reference and SYSREF signals.

FUNCTIONAL BLOCK DIAGRAM

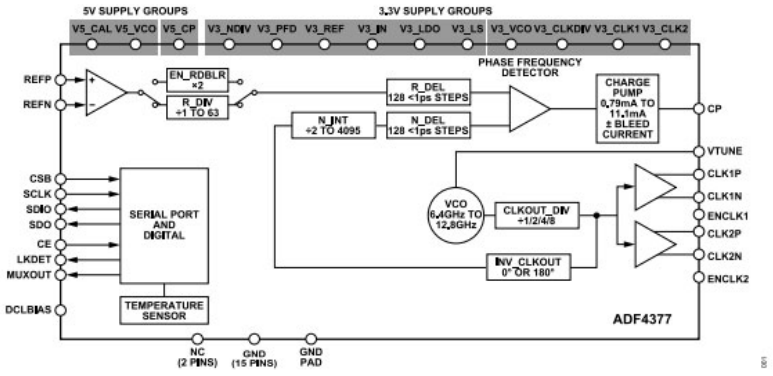


Figure 1.

SPECIFICATIONS

3.3 V Supply Group 1 pins voltage ($V_{3.3V\_1}$) = 3.3 V Supply Group 2 pins voltage ($V_{3.3V\_2}$) = 3.15 V to 3.45 V, V_{V5_VCO} = V_{V5_CP} = V_{V5_CAL} = 4.75 V to 5.25 V, all voltages are with respect to GND, T_A = −40°C to +105°C, operating temperature range, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS (REFP, REFN)						
Input Frequency	f_{REF}	10		1000	MHz	
Input Signal Level	V_{REF}	0.5		2.6	V p-p	Refer to Figure 61
Minimum Input Slew Rate			100		V/µs	
Input Duty Cycle			50		%	
Self-Bias Voltage			1.85		V	
Input Resistance			3		kΩ	Differential
Input Capacitance			1		pF	Differential
Input Current			−2		µA	
Reference Peak Detector						
Input Frequency		10		1000	MHz	
Minimum Input Signal Detected (REF_OK Bit = 1)			200		mV p-p	f_{REF} = 100 MHz, single-ended sine wave
Maximum Input Signal Not Detected (REF_OK Bit = 0)			160		mV p-p	f_{REF} = 100 MHz, single-ended sine wave
REFERENCE DIVIDER		1		63		All integers included
REFERENCE DOUBLER						
Input Frequency		10		250	MHz	EN_RDBLR = 1
PHASE/FREQUENCY DETECTOR (PFD)						
Input Frequency	f_{PFD}	3		500	MHz	
CHARGE PUMP (CP)						
Output Current Range	I_{CP}		0.79 to 11.1		mA	Set by CP_I bit fields
Output Current Source/Sink Accuracy			±2		%	All CP_I bit field settings, V_{CP} = V_{V5_CP}/2
Output Current Source/Sink Matching			±2		%	All CP_I bit field settings, V_{CP} = V_{V5_CP}/2
Output Current vs. Output Volt Sensitivity			0.2		%/V	V_{CP}[1]
Output Current vs. Temperature			280		ppm/°C	V_{CP} = V_{V5_CP}/2
Output High-Z Leakage Current			−0.01		µA	Minimum I_{CP}, V_{CP}[1]
			−0.3		µA	Maximum I_{CP}, V_{CP}[1]
VCO						
Frequency Range	f_{VCO}	6.4		12.8	GHz	
Tuning Sensitivity	K_{VCO}		0.75 to 1.25		%Hz/V	K_{VCO}[2, 3]
VCO Calibration Frequency	f_{DIV_RCLK}			125	MHz	Must set DCLK_MODE = 1, when f_{DIV_RCLK} > 80 MHz
FEEDBACK DIVIDER (N) AND CLOCK OUTPUT DIVIDER (O)						
N		2		4095		All integers included
O		1		8		1, 2, 4, 8
CLOCK OUTPUTS (CLK1P and CLK1N, CLK2P and CLK2N)						Differential termination = 100 Ω for all clock output specifications unless noted
Output Frequency	f_{OUT}	0.8		12.8	GHz	
Output Differential Voltage	V_{OD}		320		mV	V_{OH} − V_{OL} measurement across a differential pair with output driver not toggling and CLKOUT1_OP = CLKOUT2_OP = 0
			420		mV	V_{OH} − V_{OL} measurement across a differential pair with output driver not toggling and CLKOUT1_OP = CLKOUT2_OP = 1