1) Exam 1 Go-over

2) Mask layout
   - multiple die on a wafer

   Considerations

   1) space between die features and die edge
   - few hundred μm

   - for sufficient die integrity for dicing & handling

   2) Saw lanes between die
      - cut saw lane width → "kerf"
      - Dicing lanes: Si wafer ~ 75-100 μm
ceramic ~ 250 μm

   3) How close to edge of wafer?
      - depends on processing
      - DRIE ~ 1/4" from edge of wafer
      - do not etch features to die edge or wafer will
        be very fragile to handle

4) Wire bond pads
   Au wire bond
   wire ~ 25 μm dia.
   Au ball on pad ~ 75-90 μm across
   pad size 125 μm
   - process dependent
5. Mask alignment
   - Fiducials Al mask Si mask
   \[ \square + + \rightarrow \square + \]
   - Frontside/backside
   - Mask Aligner viewing area

6. Mask Technology
   - Small features < \( \approx 100 \mu m \) → Glass mask
   - Large features > \( \approx 100 \mu m \) → Glass mask (≈$200) or photoplot (≈$50)
   \[ \uparrow \sim 3 \text{ days} \quad \uparrow \sim 1 \text{ day} \]
   - Mask design: mirrored
   \[ \text{PR} \quad \text{mask} \quad \text{mask feature} \]
   \[ \text{Si wafer} \]
   - Also: light field or dark field
   \[ \downarrow \quad \uparrow \]
   \[ \text{drawn feature} \]