Nonconducting RF and DC Hot Carrier Stresses in 14/16-nm FinFETs for RF Power Amplifiers

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***Abstract*— Hot carrier reliability under nonconducting (NC) RF and dc stresses is measured and modeled on 14/16-nm FinFETs used for RF PAs. The impact of stress on I – V and RF parameters is examined. RF parameter stress response suggests that degradations are located near the drain end of the channel within the pinch-off region. For classic $V_{gs} = 0$ V OFF-state RF stress, quasi-static-approximation (QSA) significantly underestimates degradation, necessitating measurement-based lifetime modeling. At near-threshold V_{gs}, a condition of interest for our PAs, the degradation shows significant die-to-die variations dominated by variations of the subthreshold channel current that initiates the hot carriers. Modeling accounting for the subthreshold channel current variations shows that the near-threshold RF stress is approximately quasi-static. The results show that these FinFETs provide enough margins against NC RF stress for the intended PA applications.**

***Index Terms*— Hot carrier stress, nonconducting (NC) stress, power amplifiers (PAs), reliability, RF stress.**

I. Introduction

In RF power amplifiers (PAs) and switches, the transistor experiences a high drain-to-source voltage V_{ds} when the gate-to-source voltage V_{gs} is below the threshold, i.e., when the channel is not significantly conducting. Hot carrier stress under such conditions is often called nonconducting (NC) stress [1]. Models for conducting hot carrier stress underestimate the degradation under NC stress significantly [2]. In [1], RF NC stress was measured and modeled using quasi-static approximation (QSA) [3], which allows the calculation of RF stress response from dc stress measurement. In [4], we presented preliminary measurements of RF and dc NC stresses on the IO FinFETs from a 14/16-nm production technology at $V_{gs} = 0$ V, the often used NC stress bias due to its relevance in CMOS logic, SRAM [5], [6], and RF PAs.

This work presents the considerations that went into our RF measurement methodology and RF stress waveform design used in [4]. We also report on new measurements characterizing the full bias range dc and RF performance, quasi-static modeling, and the impact of die-to-die variations. To overcome the limited supply voltage and breakdown voltage in advanced CMOS technologies, stacked PA designs are widely used [7]. Stacked transistors spend a significant amount of time operating with V_{gs} close to V_{th}, the threshold voltage, and with high V_{ds}, as shown in Fig. 1 for our stacked PA design at peak output power. For handsets under a mismatched load, the maximum V_{ds} will further increase, e.g., from 2.2 to 2.6 V for a VSWR = 3:1 in a 28-nm stacked PA design [7]. The dashed line indicates V_{th}. Consequently, it is necessary to study RF NC stress around $V_{gs} = V_{th}$ in addition to the widely used $V_{gs} = 0$ V condition. However, as discussed below, the RF V_{ds} dependence for near-threshold stress is challenging to measure and model. We address this challenge by accounting for die-to-die variations of the subthreshold channel current. Our results indicate that the near-threshold RF stress is approximately quasi-static.

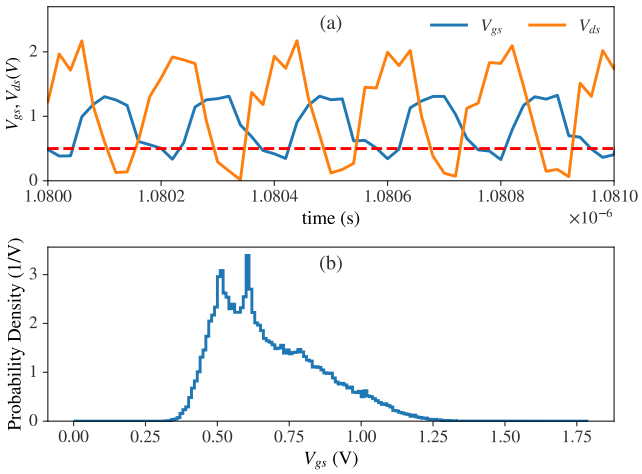

Fig. 1. (a) Simulated V_{gs} and V_{ds} waveform of a stacked transistor in a digitally-modulated RF PA at peak power. (b) Probability density of V_{gs}.

II. Technical Approach

A. Devices

$L = 135$ nm n-channel IO devices widely used in RF PA design are fabricated using a 14/16-nm FinFET technology from a major foundry and measured on-wafer at 300 K. Self-heating is negligible during NC stress. The source and

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body are tied together as in the PA and grounded by layout design for RF ground signal ground (GSG) probing. The gate and drain voltages are applied through bias tees. A 5 GHz RF NC stress is used due to its relevance for our PA. For selected experiments, 2 GHz RF stress was also used to examine frequency dependence. The nominal V_{dd} is 1.8 V. The devices used for $V_{gs} = 0$ and 0.5 V stresses have 512 and 614 fins, respectively. The stress responses were verified to be unaffected by this difference.

B. Measurement Setup

We use an HP4155 semiconductor analyzer to perform dc biasing and $I - V$ measurements, and a Keysight N5242B PNA-X to measure S-parameters and apply RF stress. We set up the RF stress using a different channel to avoid interfering with S-parameter measurements. A custom Python program controls all instruments. We account for cable and probe losses using a power meter. Standard open-short de-embedding is used to remove the impact of pads and interconnects.

C. RF Stress Waveform Design

To minimize the dc stress effect during RF stress, it is vital to reduce the dc component of V_{ds} to a level that does not significantly degrade the device under the dc bias conditions. To achieve this, we select the drain dc bias and RF power such that the minimum of V_{ds} is zero, while the maximum, $V_{ds,max}$, is set to the desired level, such as 4.2 V.

This design also helps to avoid any unintentional stress from timing latency between dc and RF instruments. For instance, when the RF power appears before the dc bias takes effect, the drain can see a negative voltage, e.g., −2 V, causing significant stress due to reverse operation. To solve the problem, we apply RF power after the dc drain bias is well established, with a sufficient delay, e.g., 1 s. Similarly, the dc drain bias is stopped after RF power is turned off by another delay. Such delays do not cause observable errors, as degradation is negligible at the dc bias by design.

S_{22} is used to estimate the impedance looking into the drain, which is then used to calculate the required RF source power. The gate RF termination is 50 Ω. As $|S_{12}|$ is small, the RF swing of V_{gs} is negligibly small, as verified by calibrated simulation.

The stress voltages are chosen so that the measurements for one stress condition can be completed within 24–30 h, including overheads of $I-V$ and S-parameters, which is at the limit of typical laboratory on-wafer RF measurement. Given the long measurement time, the PNA-X calibration is verified periodically. At each stress time, we measure:

1) $I_d - V_{ds}$, which is essential for PAs;
2) $I_d - V_{gs}$ at $V_{ds} = 0.05$ and 1.8 V; and
3) S-parameters for the same V_{gs} sweeps, from which small-signal RF parameters are extracted.

To save time, S-parameters are measured less frequently.

D. Quasi-Static Modeling

Due to the complexities of RF stress experiments, we are interested in finding out if the RF stress is quasi-static. That is, if the rate of degradation at any time can be approximated by that measured during dc stress for the same instantaneous voltages. If this is true, we can predict RF stress from much simpler dc stress measurements using QSA modeling [1], [3].

The first step is making dc stress measurements at varying dc stress input voltages V_i and constructing a model of dc stress lifetime as a function of V_i, $\tau_{dc}(V_i)$ [3]. At a given V_{gs}, the V_i includes only V_{ds} in this work.

Degradation of a transistor performance measure is modeled as a function of stress time. We choose I_{dsat}, the I_d at a well defined $V_{gs} = V_{ds} = V_{dd}$, which is widely used in the literature. While this can be repeated for all biases, we find using I_{dsat} sufficient so long as we also measure full bias range $I-V$ and S-parameters corresponding to each I_{dsat} degradation level. As shown in Fig. 1, the stacked transistor in the PA also operates in saturation, e.g., when $V_{gs} > V_{th}$ (0.5 V) and $V_{ds} > V_{gs}$.

τ_{dc} is determined as the stress time for a 10% I_{dsat} degradation, a somewhat arbitrary but widely used industry standard. We could use a different number that corresponds to a different level of overall performance degradation, e.g., the full $I_d - V_{ds}$ degradation.

Our measured degradation of I_{dsat} shows a typical power law time dependence, i.e., $\propto t^n$. If n is the same for different dc stress voltages, then it may be possible to predict the degradation under RF stress using QSA [1], [3]. If QSA modeling agrees with RF stress measurement, we can further apply QSA to determine the highest allowed RF stress. Otherwise, other approaches need to be developed.

Below, we first describe the $V_{gs} = 0$ V stress results, where the gate-induced drain leakage (GIDL) dominates the drain current [1], [4] [5], [6]. We will then present the $V_{gs} = 0.5$ V stress results where the subthreshold channel current dominates.

III. $V_{GS} = 0$ V Stress

DC stresses are applied at $V_{ds} = 4.1$, 4.2, and 4.3 V, and RF stresses are applied at $V_{ds,max} = 3.9$, 4.0, 4.1, and 4.2 V. The RF stress V_{ds} has a dc component of $V_{ds,max}/2$ so that the V_{ds} minimum is 0 V. At such high V_{ds}, the I_d at $V_{gs} = 0$ V is dominated by GIDL, as was observed in [1] and detailed below.

A. $I_d - V_{ds}$ Degradation

I_{dsat} alone is not sufficient to evaluate performance degradation, even though it is convenient and well-defined. We now examine the overall degradation, particularly the output characteristics when $\Delta I_{dsat} = 10\%$, the commonly used lifetime criterion. Fig. 2 shows the $I_d - V_{ds}$ measured for a 36 000 s $V_{ds,max} = 4.2$ V RF stress, when $\Delta I_{dsat} = 9.4\% \approx 10\%$. The results of a dc stress with the same stress time and voltage are also shown for comparison. After stress, the drain saturation voltage increases, and the I_d around linear to saturation transition decreases, which will reduce the output swing of a PA. The ON-resistance degradation at $V_{gs} = V_{dd}$ is approximately 16%, due to interface traps that decrease inversion charge density and degrade mobility. The degradation is smaller in the saturation region, suggesting that the interface traps are located

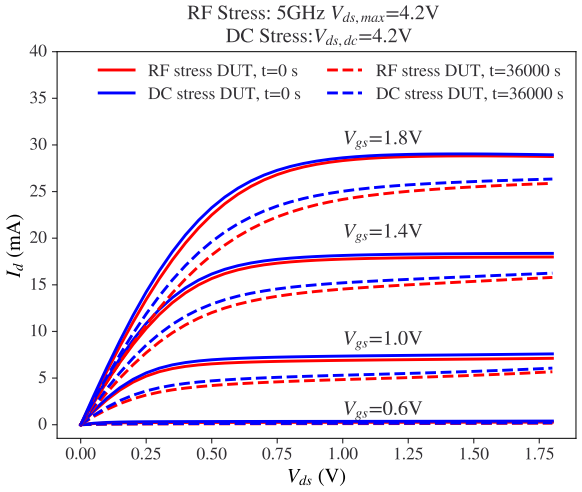

Fig. 2. Measured $I_d - V_{ds}$ degradation for 5 GHz, $V_{ds,max} = 4.2$ V RF stress, and $V_{ds} = 4.2$ V dc stress. $V_{gs} = 0$ V. $t = 0$ and 36 000 s. $\Delta I_{dsat} \approx 10\%$.

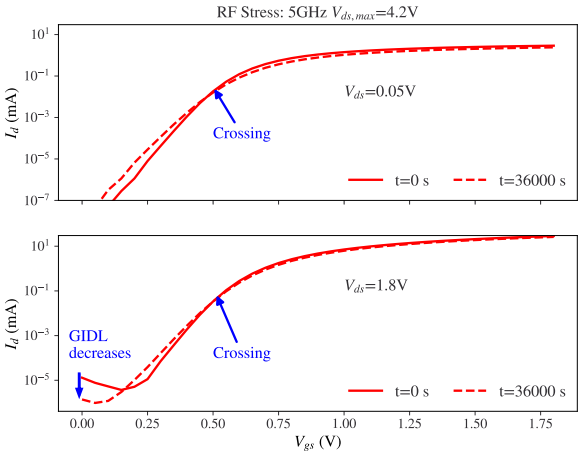

Fig. 3. Measured $I_d - V_{gs}$ degradation for 5 GHz, $V_{ds,max} = 4.2$ V RF stress. $V_{gs} = 0$ V. $t = 0$ and 36 000 s. $\Delta I_{dsat} \approx 10\%$.

near the drain, which is further evidenced by the measured RF parameters detailed below.

In the saturation region, the negative $I_d - V_{ds}$ slope at $V_{gs} = 1.8$ V due to self-heating becomes positive after stress, indicating an output conductance increase that is sufficient to offset the self-heating induced decrease. The RF Y-parameters confirm the stress-induced output conductance increase, as shown below in Section III-C.

Observe that the dc stress at the same V_{ds} as the $V_{ds,max}$ in the corresponding RF stress produces similar degradation of the $I_d - V_{ds}$ characteristics. QSA thus may not hold, as confirmed below using detailed modeling. The much simpler dc stress may still be a useful tool for assessing RF stress in these FinFETs at $V_{gs} = 0$ V in absence of RF stress capability. The dc stress V_{ds} should be set to the desired RF stress $V_{ds,max}$.

B. $I_d - V_{gs}$ Degradation

Fig. 3 shows the $I_d - V_{gs}$ measured for the 36 000 s $V_{ds,max} = 4.2$ V RF stress, when $\Delta I_{dsat} \approx 10\%$. $V_{ds} = 0.05$ and 1.8 V. The dc stress curves are qualitatively similar. At high V_{ds},

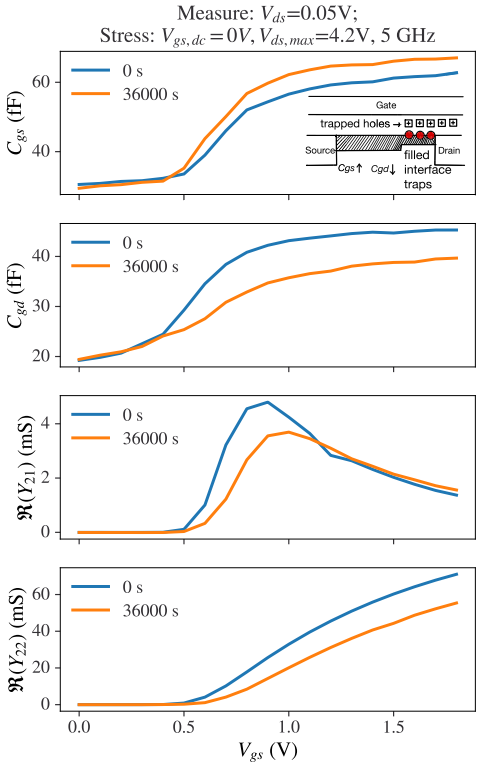

Fig. 4. Measured linear RF characteristics versus V_{gs} before and after 36 000 s RF stress at which $\Delta I_{dsat} \approx 10\%$. $V_{ds,max} = 4.2$ V.

the $V_{gs} = 0$ V current is dominated by GIDL. Crossing of the prestress and post-stress $I_d - V_{gs}$ curves is consistently observed for both RF stress and dc stress, similar to [5] and [6], due to oxide hole trapping and acceptor-like interface trap generation [6]. The holes are mainly from tunneling related to GIDL, as hole trapping is much reduced at higher stress V_{gs}. With stress, the subthreshold channel current increases, while the GIDL current decreases. The GIDL decrease is much higher than in [6], and is much higher than the subthreshold channel current increase. The subthreshold swing (SS) increases after stress, as expected.

C. RF Parameter Degradation

Figs. 4 and 5 show key linear ($V_{ds} = 0.05$ V) and saturation ($V_{ds} = 1.8$ V) RF characteristics versus V_{gs}, including C_{gs}, C_{gd}, g_m indicated by $\Re(Y_{21})$, and g_{ds} indicated by $\Re(Y_{22})$. Calculations are made using 2 GHz S-parameters before and after the 36 000 s RF stress, at which $\Delta I_{dsat} \approx 10\%$.

As the linear region shows much more changes in C_{gs}, C_{gd}, and g_m than the saturation region, we expect the damages to be located close to the drain end of the channel that is depleted in saturation. We further expect the length of the damage region to be smaller than the length of the pinch-off or velocity saturation region, as the saturation C_{gs} shows practically no change. This result is unsurprising given the relatively long channel (135 nm for high breakdown voltage). The saturation peak g_m degradation is due to mobility degradation, as evidenced by the linear region peak g_m degradation. The slight saturation C_{gd} change is likely due to damages in the gate–drain overlap region.

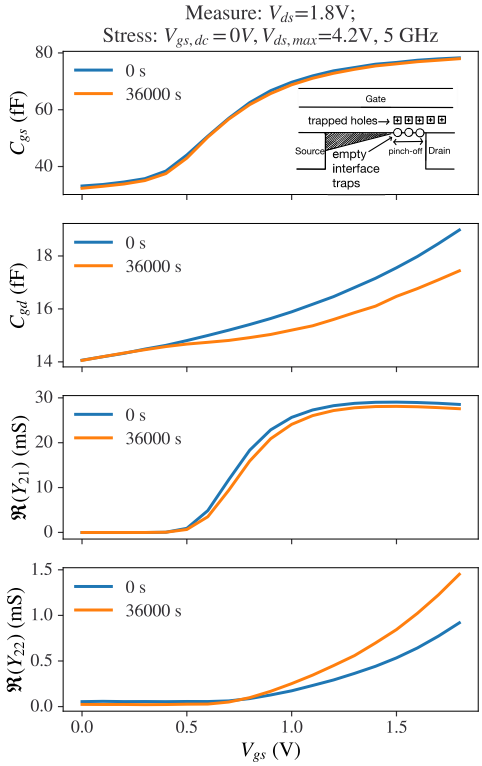

Fig. 5. Measured saturation RF characteristics versus V_{gs} before and after 36 000 s RF stress at which $\Delta I_{dsat} \approx 10\%$. $V_{ds,max} = 4.2$ V.

At $V_{ds} = 0.05$ V, once V_{gs} exceeds threshold, the transistor operates in the linear region. Compared to saturation, the interface states near the drain are much more electrically active (occupied by electrons), hence affecting the C_{gs}, C_{gd}, g_m and g_{ds} more significantly. After stress, C_{gs} increases, while C_{gd} decreases, due to reduced inversion level near the drain. The overall transistor V_{th} shows little shift, considerably smaller than what we observe for conducting stress, as can be seen from C_{gs}, g_m and g_{ds} versus V_{gs} characteristics.

At $V_{ds} = 1.8$ V, the transistor operates in the saturation region, surface potential and inversion charge are highly nonuniform along the channel. The drain-end inversion charge density is low, and experiences velocity saturation, hence affecting C_{gs}, C_{gd}, g_m and g_{ds} in a much weaker manner relative to $V_{ds} = 0.05$ V. The RF g_{ds} increases after stress, which causes the increase of $I_d - V_{ds}$ slope in Fig. 2, offsetting the prestress negative $I_d - V_{ds}$ slope due to self-heating. The g_m degradation is much less obvious than at $V_{ds} = 0.05$ V in Fig. 4, as expected. Observe that the saturation RF g_{ds} is always positive, while the dc g_{ds} from $I_d - V_{ds}$ derivative (see Fig. 2) is negative prestress. For intermediate V_{ds}, the degradation of I_{ds}, C_{gs}, C_{gd}, g_m, and g_{ds} are expected to lie between the two V_{ds} extremes.

D. Time and Voltage Dependence of DC Stress

Fig. 6 shows the ΔI_{dsat} in percentage versus stress time for various dc stress V_{ds} at $V_{gs} = 0$ V. Data can be well-fit using the usual power law, resulting in a time exponent $n \approx 0.21$. The dc stress lifetime τ_{dc} can then be determined as the time at which $\Delta I_{dsat} = C$, the end-of-life criterion. We choose $C = 10\%$ following industry practice [1], [3]. Mathematically, the dc stress degradation time dependence can be written as [2], [3]

$$D_{dc}(t) = C\left(\frac{t}{\tau_{dc}(V_{ds})}\right)^n \tag{1}$$

where $D_{dc}(t)$ is the dc stress degradation at stress time t. Here we use ΔI_{dsat} percentage as D_{dc}. The V_{ds} dependence of τ_{dc} is modeled using Takeda's equation which models the intercept of the time dependence of $D_{dc}(t)$ as a function of V_{ds} as [8]

$$\frac{C}{[\tau_{dc}(V_{ds})]^n} = \alpha_{dc} \cdot \exp\left(-\frac{\beta_{dc}}{V_{ds}}\right) \tag{2}$$

where α_{dc} and β_{dc} are empirical coefficients. We now have a $\tau_{dc}(V_{ds})$ model that can be used to calculate RF stress degradation using QSA.

E. QSA Versus RF Stress Measurement

As all the dc stresses share a time exponent n, there exists the possibility that QSA may hold. Mathematically, the degradation under time-varying stress V_{ds} can be described by [3]

$$D_{RF,QS}(t) = C\left(\int_0^t \frac{1}{\tau_{dc}(V_{ds}(t'))}dt'\right)^n. \tag{3}$$

Consider $t = N \cdot T$, with T being the period and N being a large integer. The integral only needs to be made for one cycle, and the t dependence reduces to a power law with the same time exponent n

$$D_{RF,QS}(t) = C\left(\int_0^T \frac{1}{\tau_{dc}(V_{ds}(t'))}dt' \cdot N\right)^n \tag{4}$$

$$= C\left(\int_0^T \frac{1}{\tau_{dc}(V_{ds}(t'))}dt' \frac{t}{T}\right)^n \tag{5}$$

$$= C\left(\frac{t}{\tau_{RF,QS}}\right)^n \tag{6}$$

where $\tau_{RF,QS}$ is the quasi-static RF stress lifetime [3]

$$\tau_{RF,QS} = \frac{T}{\int_0^T \frac{1}{\tau_{dc}(V_{ds}(t'))}dt'}. \tag{7}$$

From (6), if the RF stress-induced degradation is quasi-static, the time exponent n will be the same as in dc stress. The RF stress lifetime can be calculated using the dc stress lifetime model according to (7).

Using the $\tau_{dc}(V_{ds})$ model of (2), we calculate the instantaneous degradation rate, $1/\tau_{dc}(V_{ds}(t'))$, for a 5 GHz RF stress with $V_{ds,max} = 4.2$ V, for one RF cycle in Fig. 7. The left y-axis shows V_{ds}, the right y-axis shows the degradation rate, and time is normalized by the period. The average of $1/\tau_{dc}(V_{ds}(t'))$ is then calculated to obtain $\tau_{RF,QS}$ using (7).

Next, we calculate QSA RF degradation using (6) and compare the "prediction" with measured RF degradation in Fig. 8. The dc stress degradation at a V_{ds} equal to the RF stress $V_{ds,max}$ of 4.2 V is also shown for reference. The measured RF stress degradation has a different $n \approx 0.31$, much higher than the QSA prediction, which demands n to be the same as dc

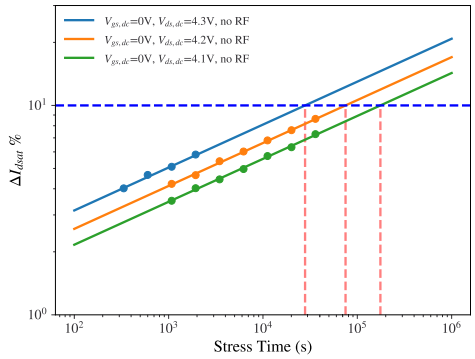

Fig. 6. Measured (symbols) and fit (lines) ΔI_{dsat} versus stress time for various dc stress V_{ds}. $V_{\text{gs}} = 0$ V. Lifetime is determined as the time required to cause 10% degradation.

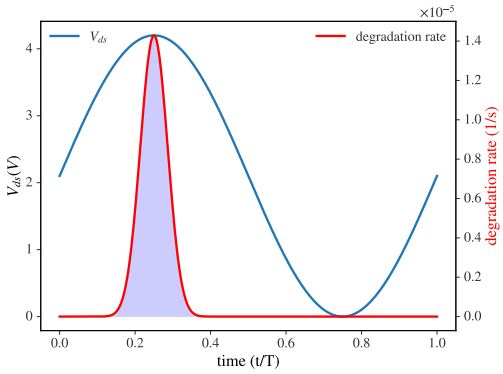

Fig. 7. $V_{\text{ds}}(t)$ and instantaneous degradation rate for one RF cycle calculated using QSA. $V_{\text{gs}} = 0$ V.

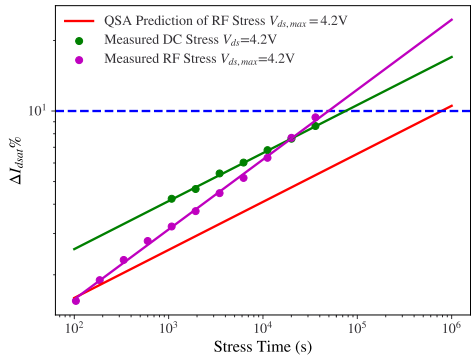

Fig. 8. Comparison of QSA (red line) and measured (symbols) RF stress degradation versus stress time. $V_{\text{gs}} = 0$ V. $V_{\text{ds,max}} = 4.2$ V, together with the measured dc stress degradation at $V_{\text{ds}} = 4.2$ V.

stress, $n \approx 0.21$. The measured RF stress lifetime is only about 1/10th of the QSA prediction.

Intuitive explanations of the higher n in RF stress and the nonquasi-static observation of the GIDL-induced stress are challenging. Processes like oxide hole trapping and Si-H bond dissociation are not necessarily quasi-static in theory, even for conducting stress [9]. At $V_{\text{gs}} = 0$ V, GIDL dominates, tunneling-induced holes gain energy and become hot while drifting in the high field. The response of tunneling, carrier energy, and hot carrier current to V_{ds} change takes time. It is plausible that 5 GHz is too fast for QSA to hold for some of these processes, particularly considering the much lower

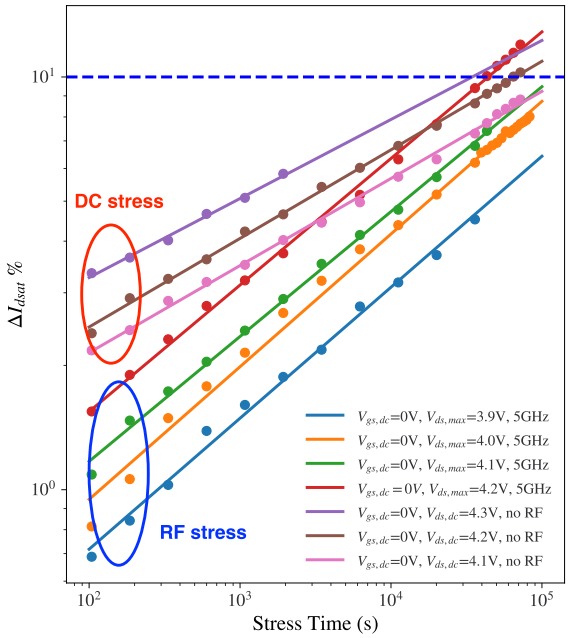

Fig. 9. ΔI_{dsat} versus stress time for dc and RF stresses at $V_{\text{gs}} = 0$ V. The dc stresses show approximately one slope, while the RF stresses show approximately another higher slope.

transistor cut-off frequency at $V_{\text{gs}} = 0$ V. If the average hot carrier energy and number in RF stress end up higher than the QSA prediction, n could be higher. Experiments at many lower frequencies are needed for further understanding. As shown below, at $V_{\text{gs}} = 0.5$ V, hot carriers originate from channel current, and the channel is relatively more conductive. Carriers gain energy faster, and QSA works approximately.

Fig. 9 compares the dc and RF stresses of varying V_{ds} at $V_{\text{gs}} = 0$ V. All the dc stresses show approximately one slope, while all the RF stresses show approximately another slope. As QSA does not hold, we cannot use (7) to determine RF stress lifetime for a given $V_{\text{ds,max}}$, or determine the allowed $V_{\text{ds,max}}$ for a ten-year lifetime.

F. RF Stress Empirical Modeling

The fact that all the RF stresses share approximately the same time exponent means that we can still model the RF stress degradation function using the simple power law. We can further model the $V_{\text{ds,max}}$ dependence of the corresponding RF stress lifetime, in the same manner as (2)

$$\frac{C}{(\tau_{\text{RF}})^n} = \alpha_{\text{RF}} \cdot \exp\left(-\frac{\beta_{\text{RF}}}{V_{\text{ds,max}}}\right) \tag{8}$$

where the subscript "RF" signifies RF stress. An inspection of (8) shows that $\ln(\tau_{\text{RF}})$ is linearly proportional to $1/V_{\text{ds,max}}$. We therefore plot τ_{RF} on a logarithmic scale versus $1/V_{\text{ds,max}}$ on a linear scale in Fig. 10. For a ten-year lifetime, the extrapolated RF $V_{\text{ds,max}}$ is 3.32 V, which is considerably higher than the NC operating condition of the transistor in our PA, if we were to design the PA for a minimum V_{gs} of 0 V. Assuming a 0.01-year lifetime requirement for mismatched loads, the allowed $V_{\text{ds,max}}$ is 3.97 V.

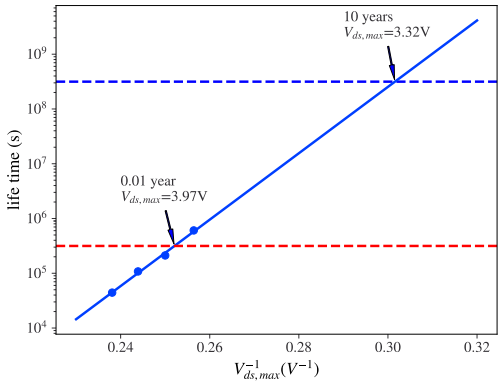

Fig. 10. RF stress lifetime defined by $\Delta I_{dsat} = 10\%$ versus $V_{ds,max}^{-1}$. $V_{gs} = 0$ V. For a ten-year lifetime, the RF maximum V_{ds} allowed is 3.32 V. For a 0.01-year lifetime, the RF maximum V_{ds} allowed is 3.97 V.

IV. Near-Threshold $V_{GS} = 0.5$ V Stress

As shown in Fig. 1, the stacked transistor in our PA operates near the threshold voltage, $V_{gs} = 0.5$ V, with a high probability. Therefore, we make dc and RF stress measurements at $V_{gs} = 0.5$ V. V_{ds} is reduced compared to $V_{gs} = 0$ V.

The $I_d - V_{ds}$ and RF parameter degradation behaviors are similar to the $V_{gs} = 0$ V results presented above for the same I_{dsat} degradation percentage. The $I_d - V_{gs}$ degradation behavior is different mainly in the subthreshold region, with a less obvious crossing of pre and post-stress curves, which indicates less oxide hole trapping due to the reduced number of holes from reduced GIDL at higher V_{gs}. However, modeling of V_{ds} dependence and related lifetime prediction proves to be much more challenging due to a much more substantial die-to-die degradation variation. By accounting for the die-to-die variation of the subthreshold channel current, we find that QSA can be used for near-threshold RF stress modeling, as detailed below.

A. Die-to-Die Variation of Degradation

Fig. 11(a) shows a set of RF stress measurements that illustrate the difficulty with identifying the $V_{ds,max}$ dependence of stress response, which was not an issue with $V_{gs} = 0$ V RF stresses.

1) Two $V_{ds,max} = 3.5$ V 5 GHz RF stresses, sc34 and sc37, showing a significant difference, implying a sizeable die-to-die variation of the stress response. The labels are identifiers of stress measurements.
2) Two $V_{ds,max} = 3.4$ V 5GHz RF stresses, sc33 and sc41, again showing considerable variation.
3) Two $V_{ds,max} = 3.3$ V RF stresses at 2 and 5 GHz, which would be identical if the stress is quasi-static and there is no die-to-die variation [1].

To confirm that die-to-die variation is at play, we compare in Fig. 12 the prestress $I_d - V_{gs}$ of the devices used in Fig. 11. $V_{ds} = V_{dd} = 1.8$ V. Observe as follows.

1) At $V_{gs} = 0.5$ V, I_{ds} varies from 16.40 to 64.39 μA. The variation is understandable as the I_{ds} in this region is due to subthreshold channel current, which depends on V_{th} exponentially. As a result, V_{th} variation greatly impacts I_{ds} in this region. V_{th} varies from 0.5046 V for sc33 to 0.5561 V for sc41, tracking I_{ds}. As V_{ds} is high, V_{th} is extracted as the V_{gs} at which I_d equals the $V_{ds} = 0.05$ V I_d at the V_{th} extracted using linear extrapolation.
2) At $V_{gs} = 0$ V, I_d shows the typical signature of GIDL. Its variation is much less. Thus we did not experience a sizeable die-to-die degradation variation.
3) At V_{gs} much higher than the threshold, the variation of I_d is slight and consistent with the amount of variation in the $I_d - V_{ds}$ characteristics.

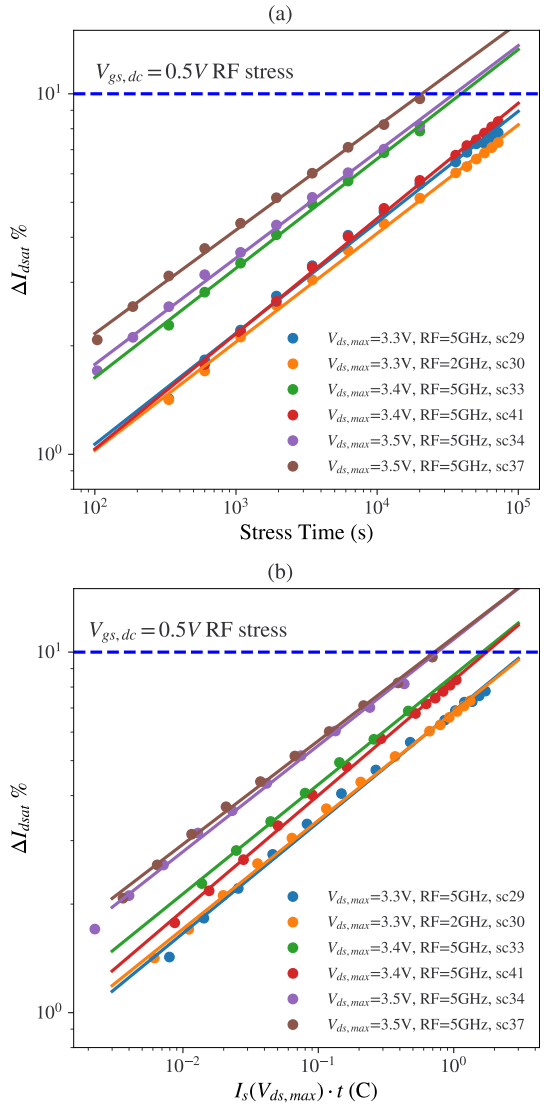

Fig. 11. (a) Measured (symbols) and fit (lines) ΔI_{dsat} versus stress time for RF stresses at $V_{gs} = 0.5$ V, illustrating the difficulty of identifying $V_{ds,max}$ dependence. (b) ΔI_{dsat} versus $I_s(V_{ds,max}) \cdot t$.

This significant variation of subthreshold I_d is a primary contributor to the observed die-to-die variation of stress responses, as the hot carriers are initiated by the electrons coming from the source. A higher channel current naturally leads to more hot carriers. The time exponent n in Fig. 11(a) varies from 0.29 to 0.32, centering around 0.3. As described below, the n value is similar to the n for dc stress, making QSA possible.

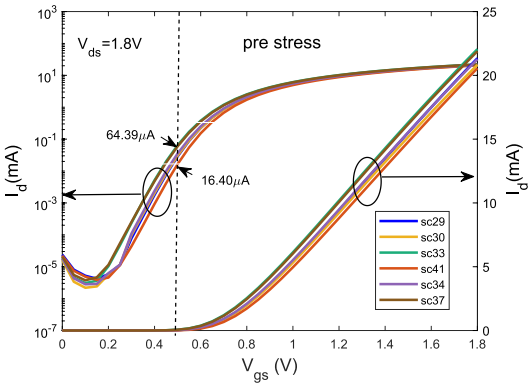

Fig. 12. Comparison of prestress $I_d - V_{gs}$ of transistors used for $V_{gs} = 0.5$ V RF stresses. $V_{ds} = 1.8$ V.

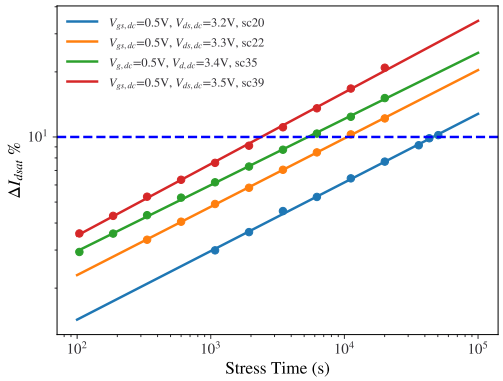

Fig. 13. Measured (symbols) and fit (lines) ΔI_{dsat} versus stress time for dc stresses at $V_{gs} = 0.5$ V.

B. DC Stress Degradation Modeling

We adapt the degradation model of [1] for FinFETs

$$D_{dc}(t) = \left(K \frac{I_s}{N_{fin}} V_{ds}^m t\right)^n \tag{9}$$

where I_s is the source current, N_{fin} is the total number of fins, K, m, and n are model parameters. It is necessary to model the V_{ds} dependence of I_s, as the RF V_{ds} varies by several volts in one cycle. On RF structures, as the source is grounded and not accessible, we still measure I_d at lower V_{ds} before avalanche becomes appreciable and extrapolate to higher V_{ds}.

In theory K, m, and n also have die-to-die variations [9]. The time exponent n extracted from fitting $D_{dc}(t)$ versus t varies from 0.28 to 0.31, as shown in Fig. 13, which is slight but observable. However, our measurements show that the I_s variation is *dominant*. Once we account for I_s variation, and determine K, m, and n from dc stresses, we can apply QSA to reasonably "predict" the RF stress lifetime. The dc stress n is similar to the RF stress n, suggesting we explore QSA. We now recast (9) into the form of (1), and obtain the dc stress degradation rate, as defined by

$$\frac{1}{\tau_{dc}} = C^{-\frac{1}{n}} \cdot K \cdot \frac{I_s}{N_{fin}} \cdot V_{ds}^m. \tag{10}$$

For dc stress *only*, we rewrite (10) as

$$\frac{N_{fin}}{I_s \cdot \tau_{dc}} = C^{-\frac{1}{n}} \cdot K \cdot V_{ds}^m. \tag{11}$$

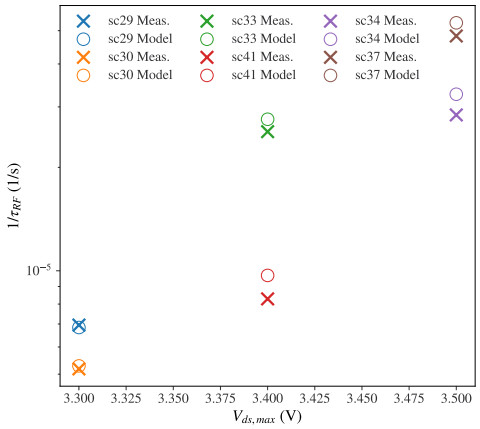

Fig. 14. Comparison of $1/\tau_{RF}$ versus $V_{ds,max}$ from quasi-static modeling and RF stress measurements. Each measurement is made on a fresh new die.

K and m can then be determined through a straight-line fitting of the left-hand side of (11) as a function of V_{ds} on logarithmic scales.

C. RF Stress Degradation Quasi-Static Modeling

Substituting (10) into (7), we can obtain the quasi-static RF stress lifetime, and then $D_{RF,QS}(t)$ using (6). A simple yet effective method to examine the impact of die-to-die I_s variation on RF stress is used during model development. In applying (10) to (7), we can approximate $I_s(t')$ by its value at the RF peak when the degradation rate $(1/(\tau_{dc}(V_{ds}(t'))))$ is the highest and contributes most to the integral in (7). Then, $(1/(\tau_{dc}(V_{ds}(t')))) \propto I_s(V_{ds,max})$, and $(1/\tau_{RF,QS}) \propto I_s(V_{ds,max})$.

We can then plot the RF stress degradation as a function of $I_s(V_{ds,max}) \cdot t$ according to (6), as shown in Fig. 11(b), before calculating the integral required for (7). For dc stress, V_{ds} is time-invariant, and $I_s \cdot t$ can be interpreted as a "stress charge" that measures the number of channel charges initiating the hot carriers. dc stress model parameter extraction using (11) then automatically accounts for I_s variation. For RF stress, such interpretation is less valid but not essential, as this "stress charge" is not used for calculating $\tau_{RF,QS}$. Instead, the entire time dependence of I_s through V_{ds} will be used. With a simple change of the x-axis from time to a charge quantity, we can account for the I_s variation, which is highly useful during measurement. The degradation data for the same $V_{ds,max}$ from different dies are much closer, suggesting that I_s variation is the main reason for the observed degradation variation.

We now proceed with the complete QSA formulation, i.e., (7), to calculate RF stress lifetime and compare the results with RF stress measurements. The quasi-static instantaneous degradation rate is calculated using (10) with complete time dependence of I_s through its V_{ds} dependence primarily due to DIBL. The die-to-die variation of I_s is considered using the prestress measurement data. Fig. 14 compares the $1/\tau_{RF}$ versus RF stress $V_{ds,max}$ from quasi-static modeling and RF stress measurements. Modeling results are shown in ○, and measurements are shown in ×. A reasonable agreement between QSA modeling and RF stress measurement is achieved. To predict the allowed $V_{ds,max}$ for a ten-year lifetime under matched load,

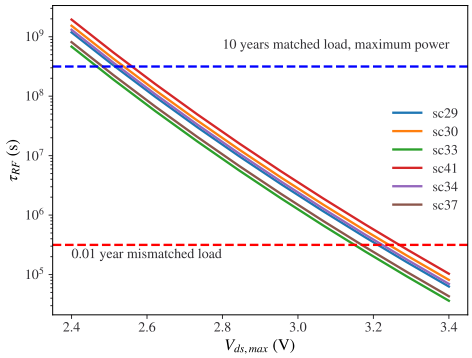

Fig. 15. τ_{RF} versus $V_{ds,max}$ using QSA for the transistors used in Fig. 11, accounting for die-to-die variation. The blue and red dashed lines indicate a ten-year and a 0.01-year lifetime. $V_{gs,dc} = 0.5$ V.

we calculate the quasi-static τ_{RF} as a function of $V_{ds,max}$, using the I_s of the devices in Fig. 11. The results are shown in Fig. 15. The $V_{ds,max}$ varies from 2.46 to 2.56 V, which is sufficient for our PAs that see less than 2 V. While the variation in $V_{ds,max}$ is small, it is important to note that modeling the $V_{ds,max}$ dependence of τ_{RF} was impossible without considering the die-to-die variation of I_s. Also shown is the 0.01-year lifetime line for the estimation of $V_{ds,max}$ under mismatched load, which is around 3.2 V.

V. Conclusion

The impact of NC RF and dc stresses on the dc and RF parameters of IO FinFETs used for RF PAs in a 14/16-nm production technology is investigated experimentally. At $V_{gs} = 0$ V, the drain current is dominated by GIDL. The dc and RF stress degradation show different time exponents (n), and QSA significantly overestimates RF stress lifetime. All the RF stress degradation share a common n, and exhibit a $V_{ds,max}$ dependence that can be modeled using Takeda's equation. The die-to-die variations of GIDL and the resulting degradation are slight. A significant die-to-die degradation variation is observed for near-threshold stress, which we attribute to subthreshold current variations. By modeling the die-to-die variation of the source current, we show that the RF stress degradation is reasonably quasi-static. The result supports channel current as the primary source of hot carriers, as is in conducting stress [10], despite the much lower V_{gs}. A simple method for a quick inspection of the impact of die-to-die variation is demonstrated. In both cases, the modeled $V_{ds,max}$ is found to be sufficient for our intended PAs. RF measurements of C_{gs}, C_{gd}, g_m, and g_{ds} suggest that the damages are located near the drain end of the channel within the pinch-off region in saturation.

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