A 12-Bit 260-MS/s Pipelined-SAR ADC With Ring-TDC-Based Fine Quantizer for Automatic Cross-Domain Scale Alignment

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***Abstract*— This article presents a power efficient and process, voltage, and temperature (PVT) robust pipelined successive approximation register (SAR) analog-to-digital converter (ADC) that quantizes signals in both voltage and time domains. In this work, a low-power SAR ADC is adopted as the coarse quantizer, while a ring-configured time-to-digital converter (TDC) is utilized in the fine quantizer to improve the linearity and power efficiency. In addition, the ring TDC also participates in the voltage-to-time conversion to guarantee that one-lap delay in the ring TDC is aligned with the least quantization step in the voltage domain. As a result, an auto-scale alignment between voltage and time domains is promised regardless of PVT variations. The ADC prototype IC was fabricated in a 22-nm CMOS technology. When measured at 260 MS/s, the ADC achieves 60.5-dB signal-to-noise and distortion ratio (SNDR) and 77-dB spurious-free dynamic range (SFDR) with a Nyquist input, while consuming 0.97 mW from a 0.8-V power supply. The calculated Walden and Schreier figures-of-merit (FoMs) are 4.27 fJ/conversion step and 171.8 dB, respectively.**

***Index Terms*— Analog-to-digital converter (ADC), hybrid ADC, pipelined successive approximation register (SAR) ADC, process, voltage, and temperature (PVT) robust cross-domain ADC, ring time-to-digital converter (TDC), TDC-assisted SAR ADC.**

I. Introduction

THE successive approximation register (SAR) analog-to-digital converter (ADC) has attracted increasing attention over the past decade for its energy efficiency, which is demanded by advanced wireless communication systems. The conversion speed of the SAR ADC is also improved with the technology scaling. It becomes feasible to implement a single-channel SAR ADC with a sample rate of a few hundred MS/s and a resolution of 8–10 bits [1], [2]. However, it is challenging for SAR ADCs to achieve a high resolution (10–12 bits) since the precision is mainly constrained by the noise level of the voltage comparator. Due to the nonlinear tradeoff between the power consumption and the comparator noise, significant power is needed to suppress the noise in a high-resolution SAR ADC [3], which degrades the overall power efficiency. The pipelined-SAR ADC or two-stage SAR ADC has been massively studied in recent years to resolve this problem. In a pipelined-SAR ADC, the noise of the subsequent stage is relaxed by the voltage amplification stage and the conversion speed is also improved by the pipelining operation. The one-time low-noise amplification seems a better solution than consuming significant power in each comparison cycle. However, it is challenging for the interstage amplifier to meet the gain and linearity requirements in advanced CMOS technologies due to the reduced power supply and lower intrinsic gain. The gain fluctuation due to process, voltage, and temperature (PVT) variations presents another problem when the amplification stage is implemented in an open-loop format [4], [5], [6]. Furthermore, the full-scale of the input signals is greatly reduced in deep submicrometer technologies, requiring even lower noise or higher gain from the amplification stage. With the reduced full-scale voltage, the size of the capacitor array used in a capacitive DAC (CDAC) has to be enlarged to guarantee that the thermal noise of the sampler is much smaller than the quantization noise. As a result, switching the capacitor array demands larger transistor size and power.

In summary, with technology scaling, reduced voltage dynamic range adversely affects the size and power of the CDAC and comparator. It becomes a challenge to achieve high resolution under reduced supply voltage.

As the signal quantization becomes difficult in voltage domain, implementing the fine quantizer in the time domain seems an attractive solution. The time-to-digital converter (TDC) is based on delay cells. Therefore, its power consumption and operational speed can be benefited from technology scaling. Moreover, the logic circuits have better noise tolerance intrinsically such that the power consumption of the delay cells and arbiters used in TDC is not a concern. The quantization resolution of a TDC is not affected by the reduced power supply and can be flexibly designed by tuning the latency of delay cells, making the TDC a good candidate for low-supply applications. Previously published TDC-assisted SAR ADCs have shown promising power efficiency when achieving high resolution [7], [8]. However, the drawback of utilizing TDC as the fine quantizer lies in its conversion speed, nonlinearity due to mismatch, and cross-domain scale-alignment against PVT variations during voltage-to-time conversion. Unlike the SAR ADC implementation, the amount of hardware needed in a flash

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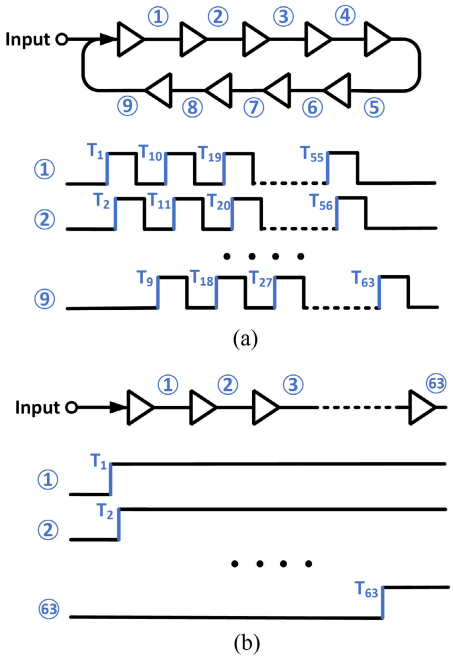

Fig. 1. Diagrams of: (a) ring TDC and (b) single-line flash TDC for 6-bit quantization.

TDC is doubled with each additional bit. This means prolonged conversion time and worsened mismatch among different delay cells. Although high gain is generally not required in the voltage-to-time converter (VTC) design, it must ensure that the least quantization step in voltage domain is aligned with the full scale in the time domain. This is hard to achieve since the quantization step of the TDC, as well as the transfer curve of the VTC, is easily sensitive to PVT variations. Inner tracking technique between VTC and TDC has been adopted to solve this problem [9], yet the operational speed is limited to maintain the tracking accuracy. High-speed TDCs, such as a 2-D Vernier TDC, have been employed to accelerate the conversion speed in time domain, yet the TDC nonlinearity and the across-domain scale alignment remain unsolved [10], [11], [12].

To overcome the aforementioned problems, this work presents a ring-TDC-based fine quantizer as the second stage of the proposed hybrid pipelined-SAR ADC. As illustrated in Fig. 1(a), the ring TDC employs only a few delay cells configured in a ring to achieve 6-bit resolution [13]. Compared to a single-line flash TDC shown in Fig. 1(b), reuse of the delay cells greatly enhances TDC's linearity with less mismatch, and less area and power. Most importantly, the presented architecture automatically matches one-lap delay of the ring TDC with the least quantization step in voltage domain, promising a PVT robust performance. Consuming only 0.97 mW from a 0.8-V supply, the prototype ADC achieves a signal-to-noise and distortion ratio (SNDR) of 60.5 dB and a spurious-free dynamic range (SFDR) of 77 dB with Nyquist input at 260-MS/s sampling rate. The prototype ADC was fabricated in a 22-nm CMOS technology and occupies a core area of 320 $\times$ 150 μm.

This article is organized as follows. Section II presents the overall architecture of the proposed hybrid pipelined-SAR ADC. Section III describes the operational principle of the ring-TDC-based fine quantizer. Section IV illustrates implementations and circuits of the critical building blocks of the ADC. Section V reports the measurement results. Finally, conclusions are drawn in Section VI.

II. Proposed ADC Architecture

A. Energy-Efficiency Consideration

In many prior-art designs, pipelined-SAR ADCs have been explored and improved for medium-to-high sample rate and high-resolution applications. To overcome the reduced voltage headroom and degraded gain encountered in small feature-size CMOS, new residual amplifiers such as ring amplifiers and open-loop amplifiers are exploited [14], [15]. Nevertheless, considerable power is still needed to provide the desired gain and linearity. A passive pipelined-SAR ADC is another approach that aims to completely remove the amplifier from the pipeline architecture [16], [17]. However, the unity-gain interstage sacrifices the noise performance of the subsequent stages.

Therefore, the combination of a passive interstage and a TDC-subsequent stage is desired. Prior arts have shown that the main block in the VTC, i.e., the cross detector, can meet the noise requirement with less power consumption than a regenerative comparator since it generally works within lower bandwidth and thus is less sensitive to high-frequency noise and is free from metastability [9], [18].

B. Architecture Overview

The block diagram and operational timing diagram of the proposed ADC are illustrated in Fig. 2(a) and (b), respectively. The 7-bit coarse SAR ADC is followed by voltage duplicated sub-quantizers in time domain, which include two identical 6-bit ring-TDC-based time quantizers with 1-bit over range to tolerate the offset between coarse and fine stages. The pipeline architecture is bridged by a ping-pong switching passive interstage for low-power and fast residue transfer [19]. In the coarse SAR ADC, split switching is adopted to maintain the common mode level of the comparator, achieving fast comparator settling time [20]. During sampling phase, one of the two sub-quantizers is connected to the coarse SAR ADC through the pipeline switches, while another sub-quantizer is performing fine conversion. During the coarse conversion, one of the two sub-quantizers remains connected to the coarse SAR combination of the passive pipeline architecture and the time ADC until the least significant bit (LSB) conversion in voltage domain is completed. Therefore, the voltage residue is already stored on the sub-CDAC when the coarse conversion is completed. The pipeline switches are then turned off and the fine conversion begins. Subsequently, another sub-quantizer is connected to the coarse SAR ADC prior to the next sampling phase.

In the second stage, the voltage-to-time conversion is accomplished by continuous switching of the sub-CDAC that causes its stored voltage to decay until it triggers the

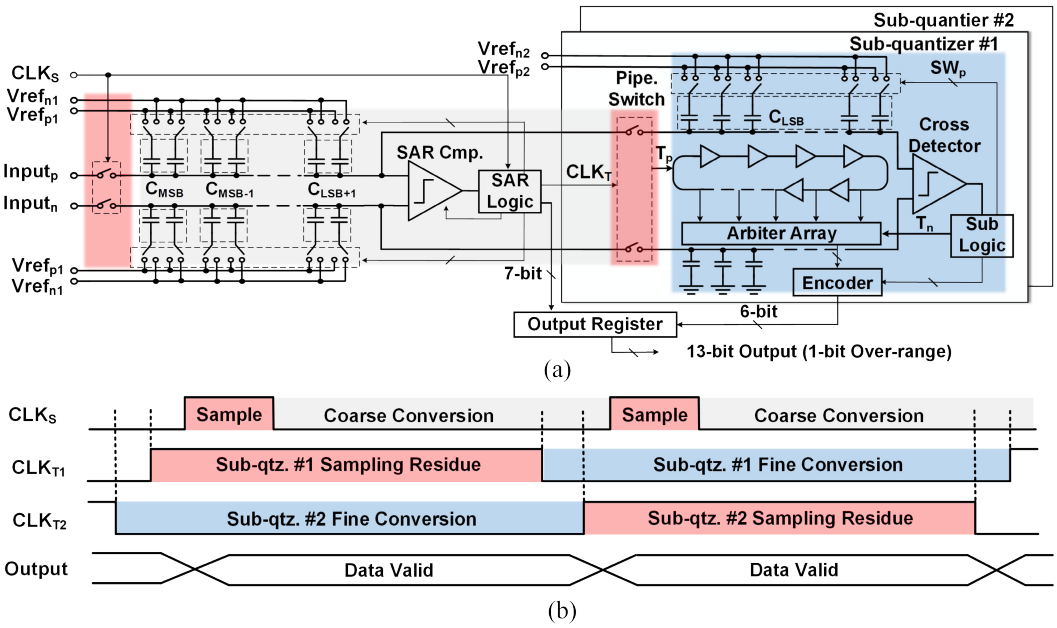

Fig. 2. (a) Block diagram and (b) timing diagram of the proposed 12-bit pipelined-SAR ADC.

cross detector. As in a digital-slope ADC [18], the time-domain conversion starts simultaneously with the voltage-to-time conversion, and thus, the VTC latency is saved. Furthermore, by employing a ring TDC in this design, a 3-bit time-domain interpolation is achieved with a minimal cost of hardware. Most importantly, PVT robustness between voltage and time domains is guaranteed. The operation of the fine quantizer is detailed in Section III. When the time-domain conversion is completed, the comparison results obtained from the arbiter array are translated to 6-bit binary codes through the encoder. Then, the 13-bit digital codes including 1-bit over range code are resampled and stored in the output registers. All the control clocks depicted in Fig. 2 are generated on-chip with asynchronous logics clocked by the external sample clock.

Thanks to the ring-TDC configuration, more bits can be partitioned in time domain without largely increased area and power. Therefore, the main concern of bit partition becomes the timing balance between the coarse and fine converters. Both voltage- and time-domain converters are designed to meet their given timing budget, thus resulting in 7 bits in SAR ADC and 6 bits in time domain. The timing budget for both stages in a balanced pipelining operation is depicted in Fig. 3.

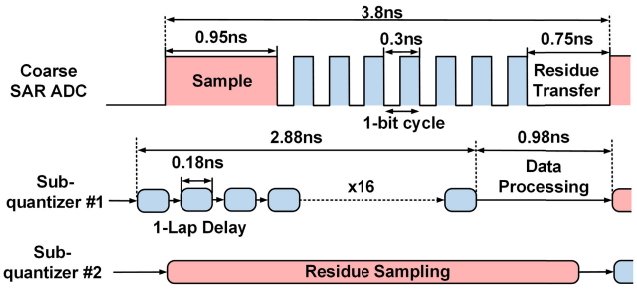

Fig. 3. Time allocations for the two-stage pipeline operations.

III. Proposed Ring-TDC-Based Fine Quantizer

The TDC-assisted ADC relaxes the noise performance in the fine quantization stage, but it still induces challenges when more bits are partitioned into time domain to improve the power and speed of the coarse stage. First, the TDC's precision relies on its linearity, which degrades with the increased hardware, thus limiting the achievable resolution of the TDC [21]. Two-step TDC is adopted to increase resolution in [9]. However, it requires a time residue transfer block which causes extra error and power consumption. In addition, it is challenging to align the time resolution of the two stages (i.e., the flash and Vernier TDC) under PVT variations. Second, fine resolution is desired when conversion speed becomes critical, and thus, fast propagation delay per stage is required, which increases power consumption since both delay stages and TDC comparators are operating at higher frequency. Moreover, the PVT robust operation discussed in Section I needs to be addressed to make the TDC-assisted ADC prototype feasible.

A. Time-Domain Quantizer Architecture

As depicted in Fig. 2(a), the proposed time-domain fine quantizer consists of a ring-configured TDC, a sub-CDAC, a cross detector, and logic circuits along with an encoder. The sub-CDAC is comprised of multiple identical unit capacitors for the digital ramp generation. As illustrated in Fig. 4, the voltage residue is initially stored on sub-CDAC and then transferred to time-domain pulses by capacitor switching and cross detection. The switching of each unit capacitor is timed by the ring-configured delay chain, namely, a switching step in the voltage domain always corresponds to one-lap delay in the time domain. Therefore, the voltage-to-time conversion gain is

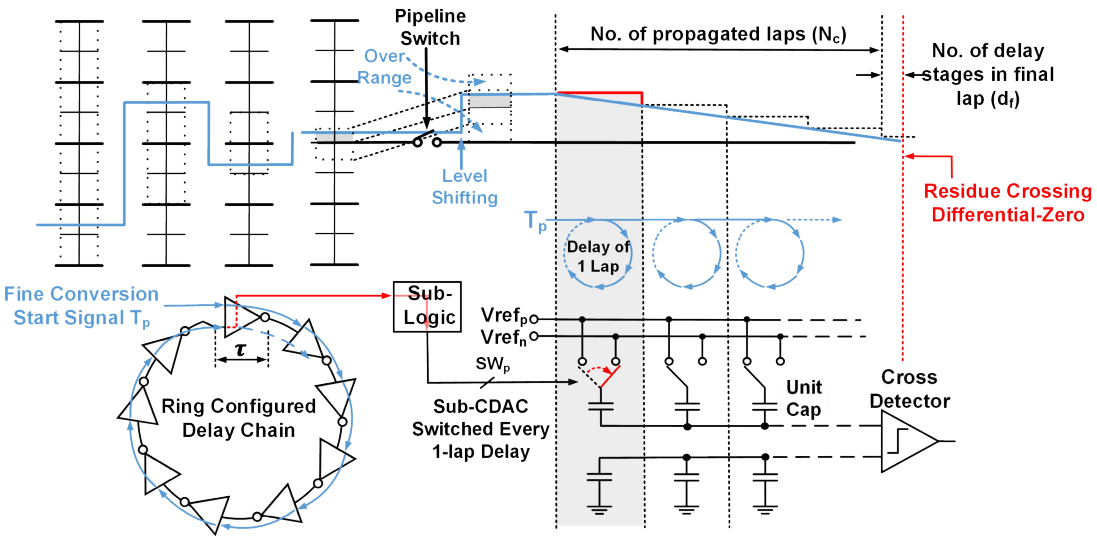

Fig. 4. Operational principle of the proposed ring-TDC-based fine quantization.

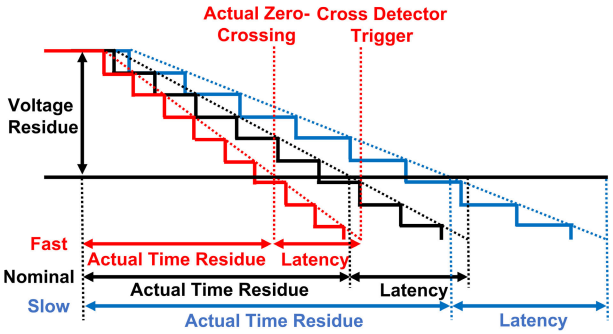

Fig. 5. PVT robust voltage-to-time conversion achieved by switching the CDAC using the lap delay signal generated in the ring TDC.

fixed regardless of any change in TDC resolution caused by PVT variations, which is illustrated in Fig. 5.

It is important to mention that the resultant VTC transfer slope is mainly determined by the scale relationship between voltage and time domains rather than the cross-detector bandwidth since the ADC architecture results in a fixed relationship that one-lap delay of the ring always corresponds to one step voltage drop on the sub-CDAC regardless of the PVT variations. The bandwidth of the cross detector will not alter this relationship. Indeed, the actual measured time includes the time spent until zero-crossing and the latency of the cross detector. The former represents the wanted data, and the latter is a data-independent dc offset. The former has a transfer gain fixed by the proposed auto-scale alignment, and the latter is PVT sensitive yet can be removed by a calibration. Therefore, the voltage-to-time conversion gain is fixed regardless of the delay variations in the TDC or the cross detector due to PVT variations, which is illustrated in Fig. 5. The proposed ADC architecture guarantees that one-lap delay in the ring TDC is always aligned with the least quantization step in the voltage domain, thus achieving auto-scale alignment against PVT variations.

This point will be further elaborated later.

The ring-TDC configuration also improves the time-domain resolution with the additional 3-bit time-domain interpolations, meaning that the LSB in the time domain is eight times finer than the capacitor switching step. The TDC LSB, i.e., the delay of one delay stage, is designed to be 20 ps while the sub-CDAC switching occurs every 180 ps, which equals to one-lap delay. This also helps to reduce the ratio of $C_{\mathrm{MSB}}/C_{\mathrm{LSB}}$ and improves the capacitor matching.

The proposed self-alignment technique between voltage and time domains is the key for this work to achieve the desired PVT robustness. It is a well-known challenge problem in the time-assisted ADC that requires the transfer curve of the VTC to track the TDC resolution over PVT variations. In this work, the CDAC switching is timed by the lap delay of the ring TDC. With a low-pass profile of the cross detector, a linear voltage-to-time (VTC) transfer function is achieved, thus allowing further time interpolation in the last lap. Compared to a discharging-based VTC, the proposed self-aligned VTC gains two advantages. The first benefit is the self-alignment embedded in the proposed architecture that automatically locks the relationship between the full-scale residual voltage and the full scale of the time quantizer. The second benefit lies upon the fact that the VTC operates at the same time as the fine quantization through the ring TDC, thus eliminating the additional time needed for the VTC as the prior-art time-assisted ADCs require. Thus, the overall conversion time is reduced.

Although the VTC speed can be further improved by either reducing the delay time, i.e., the resolution, of the ring TDC or reducing the number of delay stages per lap, both options come with penalties. The first option will cause higher power, and the second option will limit the number of bits available for interpolation in the last lap. Utilizing a two-step TDC or a Vernier TDC can refine the resolution of the time quantizer at costs of additional hardware and power. Without losing generality, we choose discharging-based VTCs and flash TDCs that have been adopted in time-assisted ADC designs for

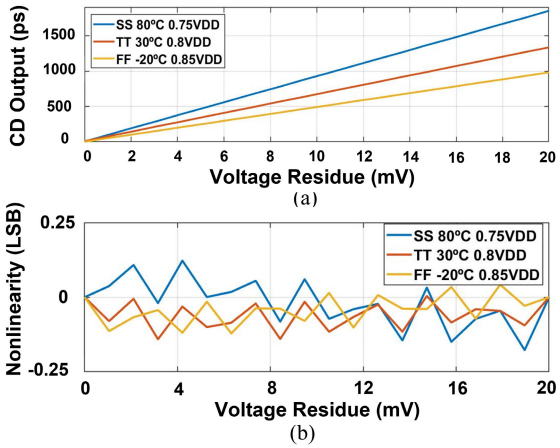

Fig. 6. Simulation of: (a) transfer function of the low-bandwidth cross detector and (b) nonlinearity of cross detector over various processes, temperatures, and power supplies.

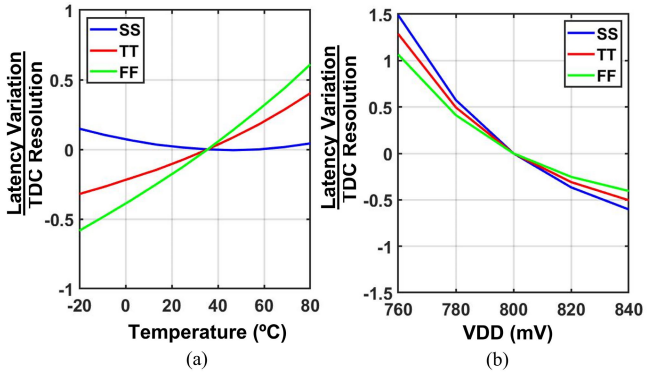

Fig. 7. Simulated cross-detector latency variation with respect to the TDC resolution over various: (a) temperatures and (b) power supplies.

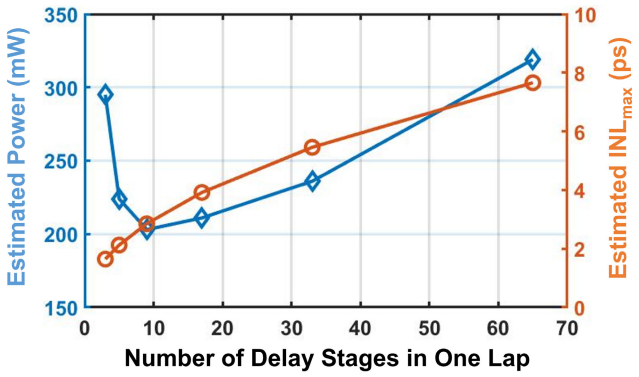

Fig. 8. Estimated TDC power and maximum INL with various number of delay stages configured in one lap.

comparison. Taking the 6-bit TDC as an example, the required discharging VTC latency would be 64 times of the TDC resolution plus the preset time of the VTC. The preset time is determined by the voltage difference between the residue common mode and the discharging threshold, which needs to be sufficiently large to maintain the VTC linearity [9]. For comparison, the reasonable estimation of the discharging-based VTC latency would be 1.5–1.7 ns, which is about half of the total conversion cycle. Therefore, the proposed structure enhances the conversion speed roughly by a factor of 2 compared to the topology using a stand-alone discharging-based VTC.

It is worth mentioning that the proposed VTC linearity relies on the low-pass filtering profile of the cross detector since the voltage signal obtained by sub-CDAC switching remains staircase decay. Smoothing the staircase is critical to the time interpolation in the last lap. The 3-dB cutoff frequency of the cross detector is designed to be around 1/50 times of the switching frequency to achieve the desired VTC linearity. The cross detector with low-bandwidth profile introduces latency to the cross-detection process. Even though the latency varies with PVT conditions, it is input-independent and adds only a fixed delay to all the outputs under a given corner. Therefore, it is considered as a dc offset and can be easily calibrated in digital data processing. The nonlinearity of cross detector is estimated as the difference between its simulated transfer curve and the ideal transfer curve divided by the TDC resolution, i.e., the LSB in time domain. Fig. 6 shows that the VTC transfer linearity varies less than $+/-0.25$ LSB under various process, temperature, and power supply. The simulation of the latency variations with respect to the TDC resolution is summarized in Fig. 7. The latency varies less than half of the TDC resolution over 80° of temperature change or 5% of VDD change. Thus, it is reasonable to treat the cross-detector latency as a constant dc offset under certain corner conditions. The latency causes 300–500-ps additional delay in the TDC conversion, which is around 15% of the required TDC conversion time and around 8% of the entire ADC conversion period. Considering the additional benefit of 3-bits conversion obtained by interpolation, the VTC latency penalty is acceptable.

The ring TDC operates similar to the conventional single-line flash TDCs except that the delay cells are reused during the conversion. The number of delay stages employed in one lap is designed to be 9 to balance the tradeoff among linearity, power, and conversion time. Fig. 8 shows the estimated power consumption and TDC nonlinearity with different numbers of delay cells configured in one lap. While the TDC conversion time remains the same, its linearity is degraded with increased delay stages and the power efficiency becomes worse with less delay stages.

As discussed above, the ring-TDC configuration with a small number of delay cells allows more compact layout and thus less mismatches and better linearity. In addition, the standard deviation of the maximum TDC integral nonlinearity (INL), which can be calculated as [22]

$$\sigma_{\max \mathrm{INL}} = 0.5\sqrt{n} * \sigma \tag{1}$$

which is reduced about three times when the number of stages, n, is reduced from 64 to 9. This can also be understood since the worst INL in each lap is the same as the worst INL in the entire conversion range of ring TDC, as depicted in Fig. 9(a). The improvement becomes critical when delay mismatch worsens in deep submicrometer technology. Fig. 9(b) shows that the simulated 3-sigma deviation of the delay mismatch σ is 1.9 ps, thus resulting in a maximum INL of 2.85 ps that

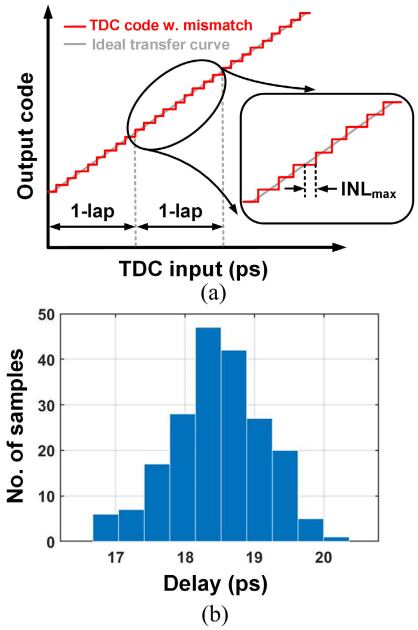

Fig. 9. (a) TDC transfer curve illustrates improved INL in ring TDC. (b) Simulated delay variations in TDC.

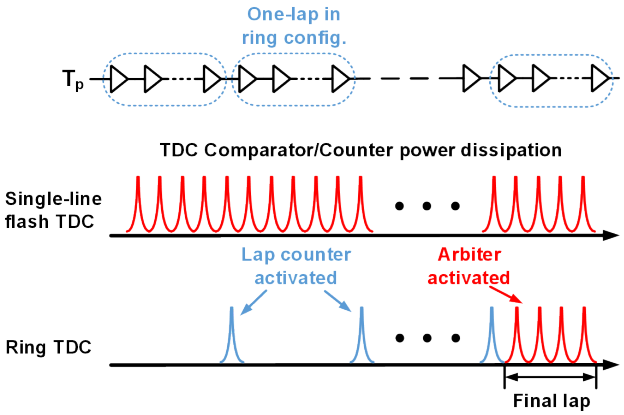

Fig. 10. Comparisons between power consumption of time comparators of a single-line flash TDC and a ring TDC.

is around one-eighth of the TDC quantization step. Therefore, the delay mismatch effect is minimized in the proposed ring TDC.

Unlike a single-line TDC, where the TDC comparator works at frequency $(1/\tau)$ set by TDC's resolution τ, the ring counter works at a lowered frequency $(1/9\tau)$ since it only needs to count the number of laps before zero-crossing is detected, as shown in Fig. 10. The comparators are turned on to detect the location of the propagating pulse for time interpolation in the last lap, which happens only when the cross-detector output is triggered. When the time resolution is shrunk to 20 ps, the low-frequency counter greatly helps the TDC power reduction, thus leading to an overall improved power efficiency of the pipelined ADC. Compared to a 6-bit flash TDC, the proposed ring-TDC quantizer uses only one-seventh of the area and consumes only about half of the power, in addition to its benefit of cross-domain auto-scale alignment for PVT robust performance.

B. Operational Procedure

Fig. 4 shows the residue signal conversion procedure from voltage domain to time domain. In the voltage domain, a 4-bit SAR conversion is illustrated for simplicity. After coarse conversion of the first-stage SAR ADC, the voltage residue is automatically stored in the sub-CDAC in the fine quantizer through the passive ping-pong switching inter-stage. Prior to the fine quantization, the voltage residue is level-shifted and the differential residual signal can be considered as a single-ended signal which is always larger than its differential zero-point. The level shifting is performed by switching the negative side of sub-CDAC from reference to ground. In addition, the over range is also included during the level shifting, which equals to the full scale of the TDC detection range. The over range implementation saves additional switching cycles compared to adding redundancy in non-binary CDAC. Furthermore, since the TDC detection time depends upon the value of the residue, the extra conversion time for over range is only needed when an error occurs in the first stage. In contrast, a redundancy bit in an SAR ADC takes a fixed conversion cycle time. When the inter-stage signal T_p in the ring causes a stair–ramp decay of the voltage residue until it crosses the differential zero point, where a signal T_n is generated by the cross detector. Thus, the time interval between T_p and T_n represents the residue signal transferred to time domain, thus performing a VTC function. Note that the voltage-to-time transfer slope is dependent on the capacitor switching step as well as its switching time, which is fixed as one-lap delay of the ring. Thus, the architecture guarantees that the LSB in voltage domain is automatically aligned with the full scale in the time domain regardless of PVT variations. Finally, the time-domain residue is measured as the number of propagated laps N_c plus the number of delays in the final lap d_f. Therefore, the time resolution τ is determined by the delay of a single delay stage, thus leading to time interpolation beyond the lap delay that corresponds to one step of the residual voltage drop.

The detailed TDC quantization process is illustrated in Fig. 11. Fig. 11(a) shows that T_p has propagated four laps before T_n is triggered such that N_c recorded in lap counter equals 4. It is worth mentioning that the staircase decay of the voltage residual is low-pass filtered by the cross detector with low bandwidth so that the voltage-to-time transfer curve is similar to that of a discharging-based VTC, thus promising a linear transfer [16]. Fig. 11(b) shows that in the final lap, where T_n has been triggered, T_1 and T_n automatically become inputs to a 3-bit flash TDC. The sequences of T_1–T_9 and A_1–A_9 are only drawn for better illustration in Fig. 11. The actual sequences are dependent on the implementations and are detailed in Section III. The arbiter results, d_f, is measured as 001 in the example, which translates to 3 LSB delays in the TDC. The time-domain residue is then calculated as

$$T_{\text{quantized}} = N_c * 9\tau + d_f * \tau. \tag{2}$$

C. Ring-TDC Implementation

There are several approaches for the implantation of the ring-configured delay chain to operate properly. The first and

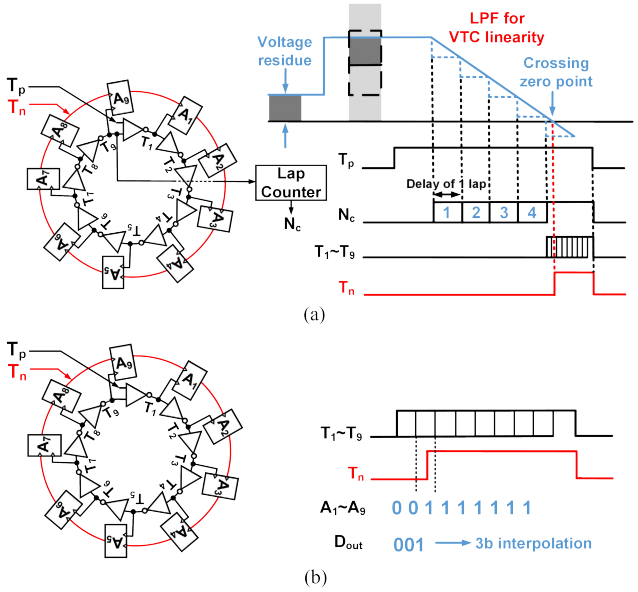

Fig. 11. Detailed ring-TDC quantization in: (a) lap counting and (b) interpolation of the final lap.

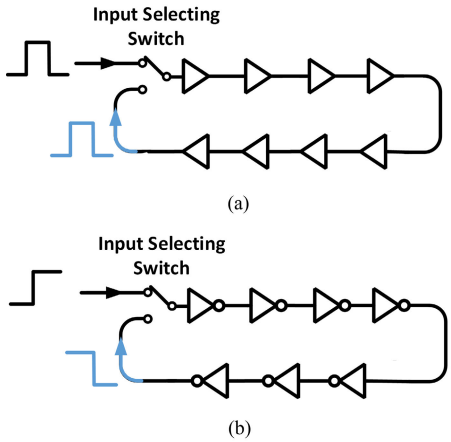

Fig. 12. Ring configurations of: (a) buffer-based delay stages and (b) odd numbers of inverter-based delay stages.

most straightforward approach is to form an end-to-end delay chain with a path-selecting switch at the input node, as shown in Fig. 12(a). Unlike the single-line delay chain, the ring requires a reset signal prior to the beginning of each lap so that the signal can keep propagating. Therefore, a pulse input signal which has both rising and falling edges is required instead of a single edge signal. The falling edge of the pulse signal is used to reset the delay cell [12].

The delay cells employed in this architecture are buffer-like stages which have in-phase input and output signals, and the delay chain can consist of any number of delay cells. Fig. 12(b) shows another approach where odd numbers of delay cells are used to form the ring TDC [13]. Unlike the first approach, the delay cells used in this structure are inverter-based delay stages that have input and output signals with opposite phase. The phase of the input signal is inverted at the beginning of each lap, so delay cells are automatically reset in each lap. This approach only requires a single edge signal as the initial

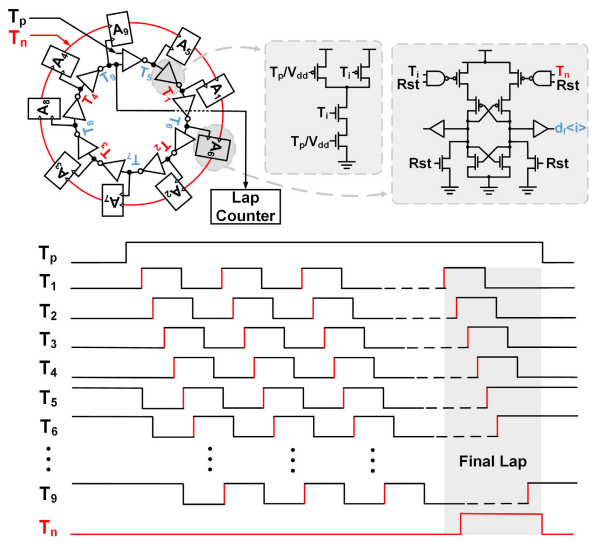

Fig. 13. Implementation of the ring TDC and rearranged sequence for T_1–T_9.

start signal avoiding using a pulse signal with its pulsewidth varying during propagation.

While the first approach seems more flexible with the capability of allowing an arbitrary number of delay cells, it encounters tough design challenges. The mismatch between the rise and fall transition times causes the duty cycle gradually to vary in each propagation lap. Eventually, the duty cycle vanishes, and the propagation ceased. According to Monte Carlo simulation, the standard variation of the mismatch between rising and falling edges ranges from 1 to 3 ps for a 20-ps delay cell, depending on the actual layout implementation, which means that the pulse signal propagation vanishes in two–three laps at most. Therefore, the second approach with odd number of delay cells are adopted in the proposed ring TDC.

The path-selecting switch introduces additional transition time, and thus, it is not used in building the delay cell. The NAND gate is adopted as the delay unit since it has two inputs and provides outputs with opposite phases. The implementation of the ring-configured delay chain is depicted in Fig. 13. The TDC resolution, 20 ps according to the post-simulation, is determined by the achievable delay time of the utilized CMOS technology with reasonable power and drive strength. The simulated TDC jitter is less than 300 fs which is much less than the TDC resolution. Utilizing a Vernier TDC or a two-step TDC can improve the TDC resolution with the penalty of higher power and larger jitter-to-resolution ratio. While both rising and falling edges are propagating through the ring, only rising edges are used to compare with T_n when the residue signal crosses the differential zero. Falling edges are treated as reset signals, and their timings are not critical. Therefore, the mismatch between rising and falling edges does not affect the precision of the TDC. Due to the phase inversion after each delay cell, the output sequence of the delay cells (T_1–T_9) is rearranged to obtain the desired order of rising edges, as shown in Fig. 13.

Since both rising and falling edges exist during TDC comparisons, digital outputs retrieved from TDC comparators

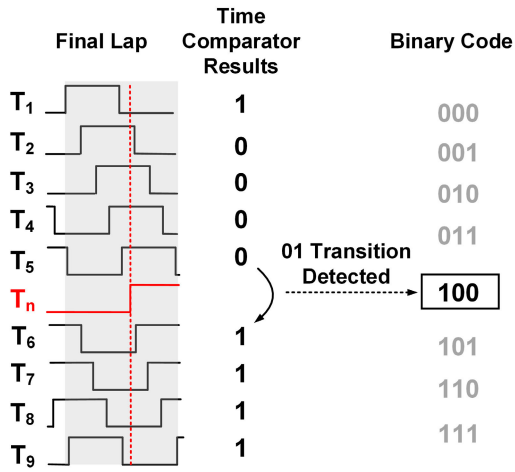

Fig. 14. Decoding example of the proposed ring-TDC output.

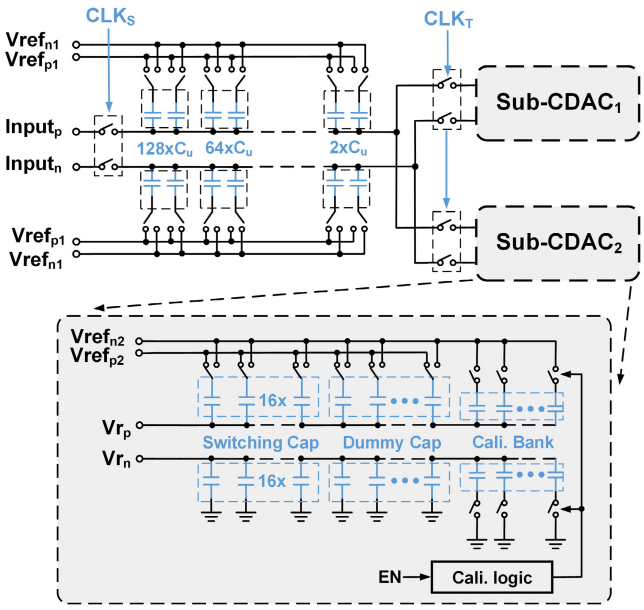

Fig. 15. Implementation of the CDAC for passive pipeline operation.

are different than outputs from a single-line flash or Vernier TDC. An example of decoding the TDC output to binary codes is illustrated in Fig. 14. Although multiple sequences of 0 and 1 may exist in the retrieved digital codes, the transition from 0 to 1 only appears once when T_n becomes ahead of the propagating signal in the ring. In the depicted example, the TDC comparator results are transferred to 3-bit binary code 100 since the 0–1 transition was detected at the output node of the 5th delay cell.

IV. Implementations of Critical Blocks

A. Capacitive DAC Implementation

The implementation of the CDAC is illustrated in Fig. 15. The top-plate sampling is employed to enhance the conversion speed. Due to top-plate parasitic, the reference switched at the back end of CDAC would be attenuated on the top plate, thus resulting in shrinking searching range. Therefore, the reference is slightly increased to 900 mV to compensate for this error. The main CDAC of the coarse SAR ADC consists

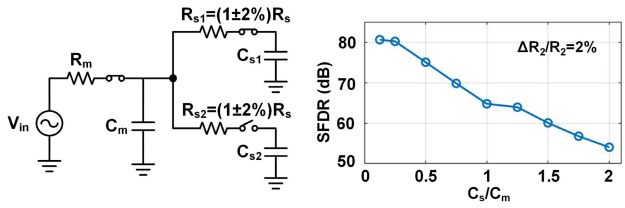

Fig. 16. Sampling model and simulated sampling bandwidth mismatch of the dual sub-CDACs network.

of 256 unit capacitors (C_u), while each of the sub-CDACs from the fine quantizer consists of 64 C_u. The ratio between the sizes of main CDAC and sub-CDAC depends on several considerations. First, since the capacitor array in the sub-CDAC becomes a passive load to the first stage during the coarse conversion, a larger size of sub-CDAC leads to greater reference attenuation. Second, the size of sub-CDAC should be sufficiently large to suppress the sampling noise in the second stage. Third, the mismatch between sub-CDACs introduces sampling error due to the ping-pong switching manner. The ping-pong switching structure can be simplified to a sampling circuit model depicted in Fig. 16. The sampling bandwidth of this equivalent circuit is calculated as

$$\omega_s = \frac{1}{R_s C_s + R_m(C_m + C_s)}. \tag{3}$$

The mismatch between the ON-resistance of the two inter-stage switches generally dominates. Therefore, the sampling bandwidth mismatch is calculated as [17]

$$\frac{\Delta\omega_s}{\omega_s} = \frac{-1}{\frac{R_m}{R_s}\left(\frac{C_m}{C_s}+1\right)+1} * \frac{\Delta R_s}{R_s}. \tag{4}$$

To improve the sampling linearity, a large ratio between the main CDAC and sub-CDAC is desired. Last, but not the least, when switching from one sub-quantizer to another, the detection range of the ADC is multiplied by a gain error factor of

$$\alpha = \frac{G_1}{G_2} = \frac{C_m + C_{s2}}{C_m + C_{s1}} \tag{5}$$

where G_1 and G_2 are capacitance ratios between the main CDAC and two sub-CDACs and are calculated as

$$G_1 = \frac{C_m}{C_m + C_{s1}} \tag{6}$$

$$G_2 = \frac{C_m}{C_m + C_{s2}}. \tag{7}$$

It is shown from (5) that to obtain α close to 1, a large ratio of C_m–C_s and a small mismatch between C_{s1} and C_{s2} are desired. To address these tradeoffs, the CDAC ratio is designed to be 4–1 in this design, thus resulting in 240 fF capacitance in sub-CDAC. With about 2% ON-resistance variation, the simulated SFDR achieves 80 dB with the designed capacitance ratio, as shown in Fig. 16. In addition to 16 unit capacitors that are used to perform the stair–ramp switching, 48 dummy unit capacitors are employed to enlarge the CDAC size. Furthermore, calibration capacitive banks comprising fractional capacitors are employed to compensate the capacitor process mismatch and routing parasitic. To obtain

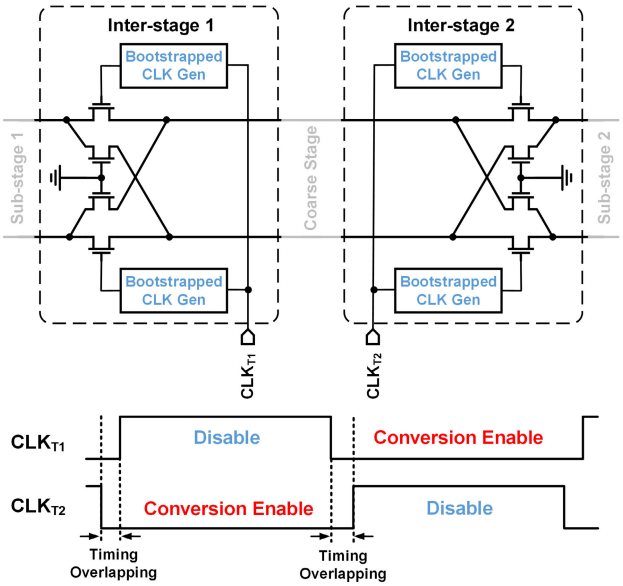

Fig. 17. Circuits and timing diagrams of the adopted passive inter-stage.

the correct switching step in the sub-CDAC, a second reference voltage that is one-fifth of the main reference voltage is required. Both references of the first and second stages are generated from an on-board low-noise low-dropout regulator (LDO) chip with fine tuning network to compensate the reference mismatch caused by routing parasitics.

B. Passive Inter-Stage

Fig. 17 depicts the circuit of the passive inter-stage bridging coarse and fine stages. The enable and disable clocks for two sub-quantizers CLK_{T1} and CLK_{T2} are generated with an asynchronous logic unit from the ADC sample clock CLK_S. It is shown in (4) that the sampling bandwidth limit is improved by an enlarged ON-resistance of pipeline switches. However, sufficiently small ON-resistance R_S is required for residue transfer. In this design, the ON-resistance of inter-stage switches is slightly smaller than that of sampling switches to meet the 12-bit precision for residue transfer. Large switches introduce significant kick-back effect between pipeline stages. As illustrated in Fig. 17, the overlapping of enabled cycles of CLK_{T1} and CLK_{T2} allows additional time for TDC conversion and saves around 600-ps conversion time in each conversion cycle according to the simulation.

C. Cross Detector

As discussed in Section II, the noise from the cross detector becomes the major noise contributor in the fine quantizer and thus requires a careful design. The circuit of the cross detector is illustrated in Fig. 18. A two-stage architecture is adopted to enhance the gain under reduced power supply. The cross detector is reset during the idle phase of each fine quantizer. The reset switches pre-charge the output nodes of the cross detector to VDD or GND accordingly. Due to the ping-pong operation, the reset time for each cross detector is sufficiently long to avoid any memory effect. The bandwidth of the cross detector is designed to be 80 MHz, which is around

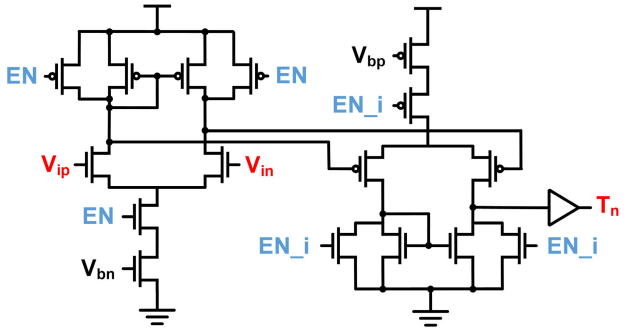

Fig. 18. Circuit of the cross detector employed in the fine quantizer.

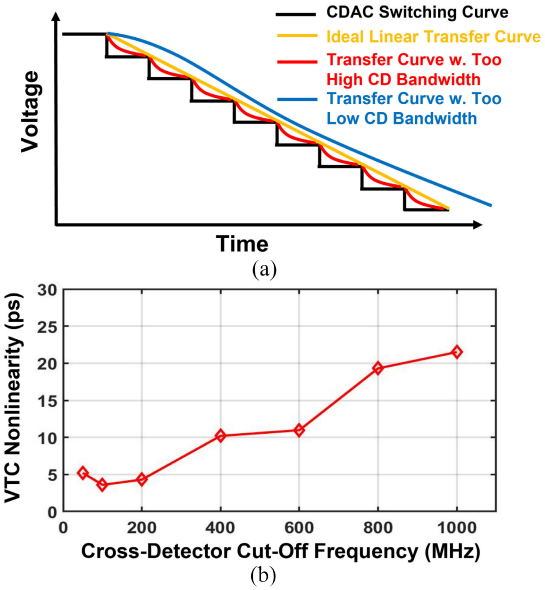

Fig. 19. (a) Illustration of voltage-to-time transfer curve with different cross-detector bandwidths. (b) Simulation of VTC nonlinearity with a different cutoff frequency of the cross detector.

1/50 of the sub-CDAC's switching frequency (5.5 GHz). The low-bandwidth profile allows the cross detector to work as a low-pass filter (LPF) to filter out the switching glitches in the original staircase waveform, thus resulting in a linear voltage-to-time conversion [16]. The linearity of voltage-to-time conversion relies on the bandwidth optimization of the cross detector. As depicted in Fig. 19(a), the nonlinearity of the cross detector, defined as the difference between the actual voltage-to-time transfer function and the ideal linear transfer curve, will be degraded when the bandwidth of the cross detector is either too high or too low. Therefore, the bandwidth is optimized based on simulated linearity. According to the simulation results shown in Fig. 19(b), bandwidth lower than 200 MHz is required to achieve acceptable nonlinearity within 1/4 LSB. The resultant nonlinearity from the 80-MHz bandwidth is around 2.8 ps (15% LSB), which is sufficient to tolerate the nonlinearities from the TDC and the sub-CDACs. Bandwidth lower than 50 MHz does not further improve the nonlinearity and rather prolong the latency since the response time of the cross detector is increased. Therefore, the bandwidth is selected to be 80 MHz to balance the linearity and conversion time requirements.

TABLE I
NOISE BUDGET OF THE PROPOSED ADC

	Simulation Results	% of Total Noise
Quantization Noise	7.76 nV^2	22.1%
Sample Noise (Coarse + Fine)	20.11 nV^2	57.4%
Cross Detector Noise	6.97 nV^2	19.9%
TDC Noise	0.19 nV^2	0.6%
Total Noise	35.03 nV^2	100%
Resultant SNR	66.9 dB	

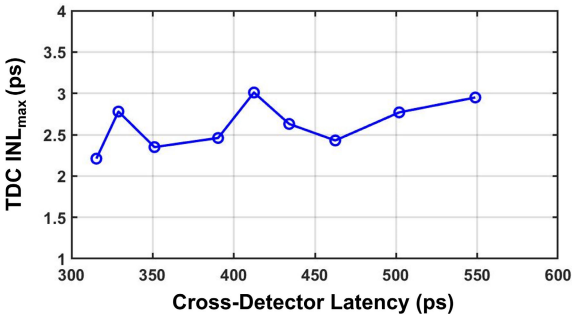

Fig. 20. Simulation of maximum TDC INL with varied cross-detector latency over process and mismatch.

The simulation results indicate that the cross detector achieves 6.9 nV^2 of noise power when consuming 0.23 mW from a 0.8-V power supply. The noise power breakdown of the proposed ADC is summarized in Table I.

The sub-CDAC switching time by the ring lap delay sets up the coarse transfer function of the VTC, whose gain (slope of the staircase waveform) is PVT insensitive. The LPF profile of the cross-detector transfer function smoothens the VTC transfer curve, thus allowing further interpolation between the coarse quantization steps in time domain. Although the bandwidth of the cross detector is PVT sensitive, it will not affect the interpolation greatly since it only provides filtering effect between adjacent coarse quantization steps. The latency of the cross-detector does not affect the fine quantization, because the variation of the latency is a relatively slow process and is thus input independent. However, the variation of the latency is a relatively slow process and thus is input-independent. The only remaining nonlinearity of the fine quantizer is the mismatch among the delays in the ring TDC. However, the proposed ring TDC greatly reduces the number of delay stages compared to a flash TDC and aligns the total lap delay with the voltage scale. In addition, the proposed VTC is embedded in the fine quantization process and thus does not consume extra time. Therefore, the proposed ADC architecture with a ring TDC achieves good linearity, and excellent power and time efficiencies for the voltage-to-time transfer.

To carefully examine the effect of cross-detector latency variation on the resulted output digital code, the worst INL of the ring TDC is simulated and presented in Fig. 20. The latency is mainly determined by both the response time of the two-stage amplifier and the delay time of the subsequent inverter stages, which amplify the polarity change event to a rail-to-rail pulse signal. Although the cross-detector latency is not aligned to the lap delay of the ring TDC, the extra latency does not affect the final accuracy of digital outputs. To better illustrate this, consider two time-domain outputs that equal to 2.1 and 3.4 laps in a ring-configured delay chain, respectively. When added with the extra VTC latency of 1.4 laps, the final time-domain outputs are 3.5 and 4.8 laps. The difference between these two codes remains the same. The example shows that the latency does not have to be aligned to the lap delay of the ring TDC. The final TDC outputs only need to measure the total time of the original zero-crossing signal and the latency. To verify the statement, TDC INL is simulated with Monte Carlo simulation to obtain the maximum INL in output data with various cross-detector latencies. It is shown in Fig. 20 that the resultant TDC worst INL barely changes with the variation of VTC latency.

The drawback of utilizing a low-bandwidth cross detector is that the detection latency is prolonged, which introduces the dc offset in digital outputs. The slow startup of the cross detector also becomes a concern if it starts to limit the conversion time in the second stage. To overcome these problems, a maximum of 16 unit capacitors rather than 8 are available for switching in the sub-CDAC to cover the latency of the cross detector. The capacitor switching is turned off after T_n is generated to save power. Not all the additional eight capacitors will be used for switching. They are implemented so that the latency is covered even in the slowest corner.

The overlapping timing in fine quantizers mentioned above helps to save the conversion time such that the overall timing in the second stage is still balanced with that in the first stage. The resulting dc offset is estimated by post-simulation and digitally subtracted from the final outputs.

D. Nonidealities and Calibration

The performance of the proposed ADC can be degraded by the mismatch of the dual fine quantizers. The mismatch between sub-CDACs leads to pipeline gain error when switching from one fine quantizer to another. To minimize the gain error, a foreground calibration is performed in both sub-CDACs by adding fractional unit capacitors to the capacitive array. The calibration bank of the fractional unit capacitors allows fine calibration precision below the LSB in voltage domain. During the calibration mode, a differential-zero signal is sampled by the coarse stage. Then, two types of residues are created by adjusting the capacitor switching in the first stage. One residue is the full scale for the fine quantizer, and another residue is half of the full scale. By quantizing these two types of residues using two fine quantizers separately, the gain errors can be estimated and calibrated. The one-time reference tuning is performed with a similar method. By sampling full-scale and half-scale residue to the fine quantizer, the proper reference ratio is obtained when the difference between outputs of these two types of residues equals 16, which is half of the second-stage detection range.

Since two cross detectors are used alternately, the mismatch between cross detectors is not input-dependent and can be digitally corrected. The calibration method is similar to the

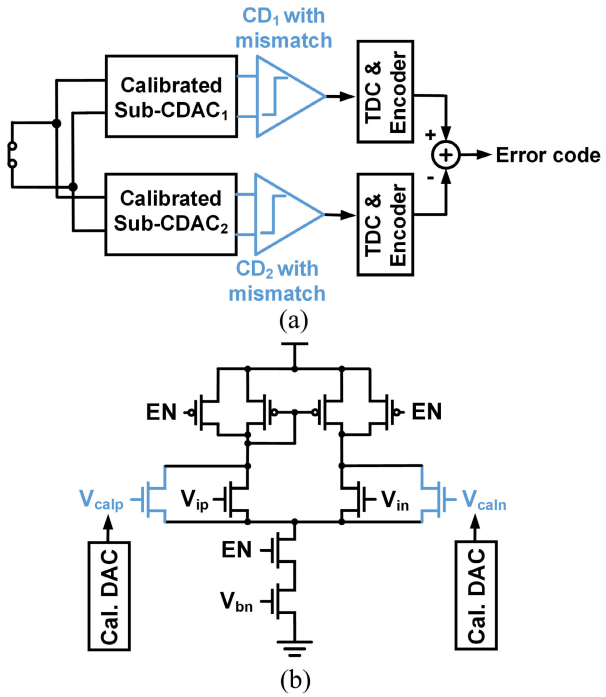

Fig. 21. Calibration schemes of: (a) mismatch between the dual cross detectors and (b) input offset of the cross detector.

calibration of the sub-CDACs, except that only a fixed differential-zero sampling is required, which is depicted in Fig. 21(a). In addition, the offsets of both cross detectors are calibrated prior to the mismatch calibration to minimize the needed correction range, as shown in Fig. 21(b). The aforementioned foreground calibration is performed only one time during the measurement under varied temperatures and power supplies since most of the errors are considered static and data-independent, except the errors caused by the mismatches among the delay stages and between the dual fine quantizers.

The ring-configured TDC utilizes nine delay stages instead of 8 to eliminate the mismatch effects of rising and falling edges that could cause pulse vanishing during its propagation. Therefore, the weightings for lap counter results and digital bits from the coarse stage are changed to multiples of 9 instead of 8. As a result, one additional bit is needed to cover the entire range of the code since it is larger than 2^{12}. The outputs can be easily converted to binary format, either with hardware or digital processing. For hardware implementation, the cost of these encoders is low compared to the ADC core since the needed digital circuits are simple and work only once during one conversion cycle.

The sampling noise of the second stage is the main drawback of using a unity-gain inter-stage. Fortunately, with current technology, the CDAC size is more determined by the unit-capacitor matching requirement of a 12-bit ADC than the required kT/C noise. In this design, the unit capacitor is designed to be 3.8 fF to meet the matching requirement, and the resulted sampling noise is tolerable as summarized in Table I. Thanks to the passive inter-stage, dynamic mismatches of these critical blocks drift slowly over time. Hence, the foreground calibration is sufficient for the measurement of the proposed ADC.

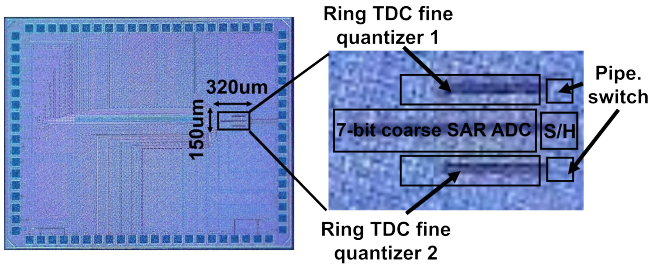

Fig. 22. Die microphotograph of the proposed hybrid ADC.

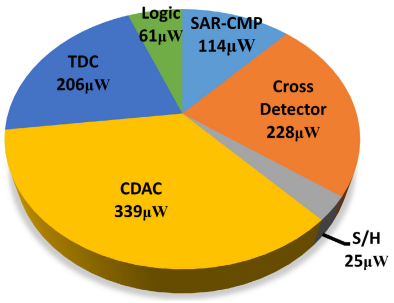

Fig. 23. ADC chip power consumption breakdown.

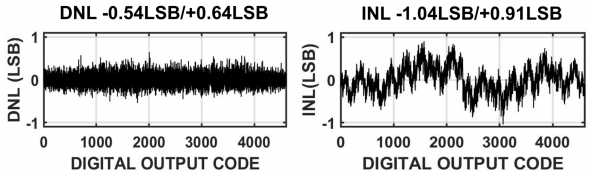

Fig. 24. Measured static performance of DNL and INL.

V. Measurement Results

The concept of the proposed hybrid ADC architecture with time-domain fine quantization was presented in [23]. To prove the concept, a prototype of the proposed 12-bit hybrid ADC with ring TDC as its fine quantizer was fabricated in a 22-nm fully depleted silicon on insulator (FDSOI) technology [24]. The die photograph in Fig. 22 shows that the active area of the ADC core is 0.048 mm^2.

The input sampling capacitance is the total CDAC capacitance including the main CDAC and one of the sub-CDACs, i.e., 1.2 pF. An on-board low-noise regulator is used to generate the reference voltage, and sufficiently large on-chip bypass capacitance is used to stabilize the reference. Digital outputs are resampled by a 1/9 down-sample clock rate to relax the output buffer design. Prior to the measurement, offsets of the main SAR ADC comparator and the cross detector in the fine quantizer are foreground calibrated with automatic searching logics, which are the same as the SAR algorithm. Then, mismatch of the dual sub-quantizers is calibrated as detailed in Section IV. Since the interstage is passive and time-domain full-scale is auto-aligned with the coarse sub-range, no background calibration is needed for this design. Measurement results of the prototype ADC are summarized in the following.

When operating at a sampling rate of 260 MS/s, the prototype ADC core consumes only 0.97 mW from a 0.8-V power supply with a 0.9-V reference voltage. The power

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART ADCS

	This Work	ISSCC 2017 [4]	VLSI 2019 [5]	ISSCC 2016 [18]	VLSI2014 [19]
Architecture	**Pipelined SAR-Ring TDC**	Pipelined SAR	Pipelined SAR	Digital Slope-SAR	Pipelined SAR
Process [nm]	**22**	65	40	28	65
Resolution [bit]	**12**	12	12	12	12
Supply [V]	**0.8**	1.3	0.9	0.9	1
Fs [MS/s]	**260**	330	200	100	210
Power [mW]	**0.97**	6.23	3.9	0.35	5.3
$SNDR_{LF}$ [dB]	**63.5**	67.7	61.1	65.67	63.48
$SNDR_{HF}$ [dB]	**60.5**	63.5	62.1	64.43	60.1
$FoM_{Walden\ HF}$ [fJ/c.s.]	**4.27**	15.4	19	2.63	30.3
$FoM_{Schreier\ HF}$ [dB]	**171.8**	167.7	166.2	176	163
Area [mm^2]	**0.048**	0.08	0.026	0.047	0.48

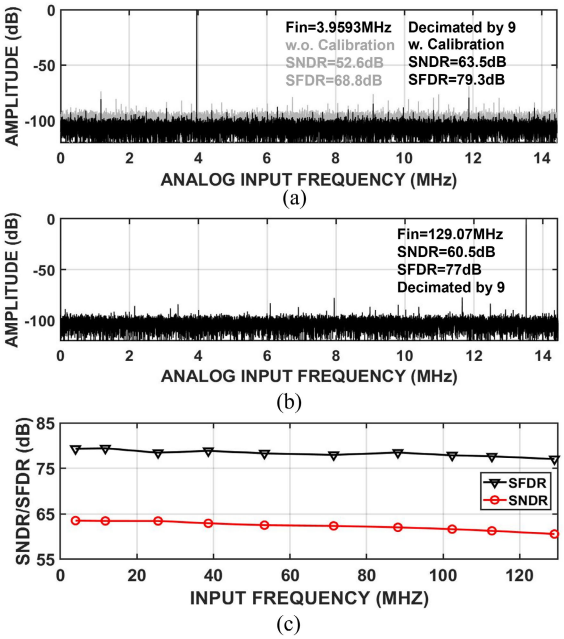

Fig. 25. Measured ADC output spectra: (a) comparison of with and without calibration at low input frequency and (b) at close to Nyquist input frequency. (c) Measured SNDR/SFDR versus the input frequency.

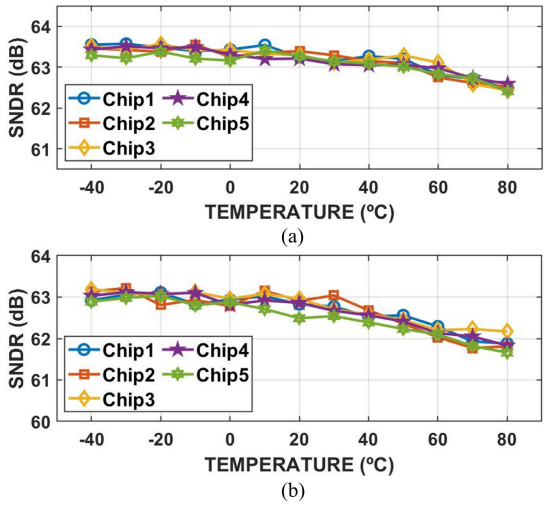

Fig. 26. Measured cross-chip SNDR under temperature variations with: (a) 0.85 V power supply and (b) 0.75 V power supply.

consumption breakdown is depicted in Fig. 23. Analog blocks including SAR comparator, cross detector, and sampling circuits consume about 366.5 μW. Capacitive DACs including the main CDAC and sub-CDACs consume about 339.1 μW. The ring TDC in the fine quantizers consumes 206.6 μW. Control logic circuits in both coarse and fine quantizers consume an additional power of 60.4 μW.

The static performance of the prototype ADC was measured with an input frequency close to 1 MHz. As shown in Fig. 24, the measured differential nonlinearity (DNL) and INL are $-0.54/+0.64$ and $-1.04/+0.91$ LSB, respectively. When measuring the dynamic performance, the input frequency of the prototype ADC was swept from low frequency to Nyquist input frequency with a sampling rate of 260 MS/s and an input swing of 1.25 Vpp. The prototype ADC achieves peak SNDR of 63.5 dB and SFDR of 79.3 dB at the input frequency of 3.9 MHz. At Nyquist input frequency, the measured SNDR and SFDR are 60.5 and 77 dB, respectively. The measured spectra before and after foreground calibration are illustrated in Fig. 25(a) to show 10.9-dB SNDR improvement with sub-quantizer mismatch and offset calibration. Measured spectra at Nyquist input frequency are shown in Fig. 25(b), while Fig. 25(c) shows the plot of SNDR/SFDR versus the ADC input frequency.

To illustrate the PVT robustness of the proposed ADC, SNDR of the ADC was measured over supply and temperature variations. As shown in Fig. 26, the measured cross-chip

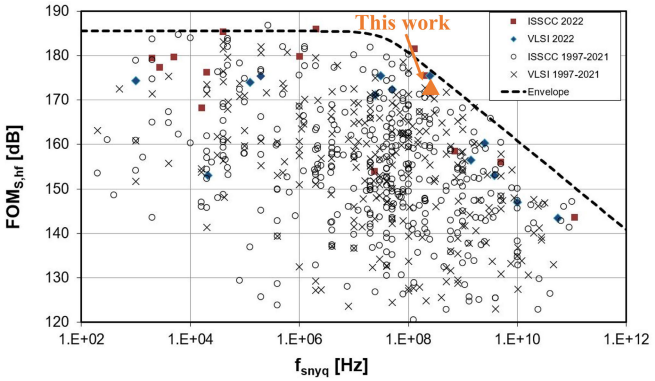

Fig. 27. Comparison of Schreier FoM with prior-art ADCs published at ISSCC and VLSI from 1997 to 2022.

SNDR degrades less than 1.9 dB over 0.75–0.85-V power supply variations and −40 °C to 80 °C temperature variations, thus demonstrating the robust performance over PVT variations without background calibration.

At Nyquist input frequency, the resultant Walden and Schreier figures-of-merit (FoMs) of the proposed ADC are 4.27 fJ/conversion step and 171.8 dB, respectively. Table II summarizes the ADC performance with comparisons to the recent published works with similar sample rates. According to Dr. Boris Murmann's ADC performance survey, the Schreier FoM of the proposed ADC is plotted in Fig. 27 as comparisons with previously published works at ISSCC and VLSI from 1997 to 2022, thus showing improved power efficiency performances at the sampling rate in the range of 200–300 MS/s.

VI. Conclusion

This article presents a 12-bit hybrid pipelined-SAR ADC with ring-TDC-based time-domain fine quantizer to achieve a good power efficiency and PVT robust performance at 260-MS/s sample rate. The demanding noise requirement of the 12-bit ADC is relaxed by utilizing a low-power ring TDC and a low-bandwidth cross detector in the fine quantizer. The adopted passive pipeline stage saves power and eliminates transition latency during the residue transfer. The ring-TDC fine quantizer not only saves power by using lap counter that operates at a lowered frequency, but also improves linearity by reusing the delay stages in a ring-configured delay chain. Furthermore, PVT robustness between voltage and time domains is promised since the lap delay of the ring TDC is automatically aligned with the switching step in the voltage domain.

The prototype ADC that was fabricated in a 22-nm CMOS process achieves a peak SNDR of 63.5 dB when operating at 260-MS/s sampling rate. Due to the proposed power efficient architecture with time-domain fine quantizer, the ADC core consumes only 0.97 mW. In addition, the prototype ADC exhibits less than 1.9-dB SNDR degradation over 0.75–0.85-V power supply variations and −40 °C to 80 °C temperature variations. Consuming a low power of less than 1 mW, the 12-bit 260-MS/s ADC prototype achieves PVT robust performance with a measured Walden FoM of 4.27 fJ/conversion step and a measured Schreier FoM of 171.8 dB, respectively.

Acknowledgment

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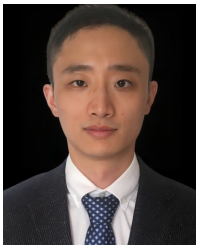

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