10.4 A 0.97mW 260MS/s 12b Pipelined-SAR ADC with Ring-TDC-Based Fine Quantizer for PVT Robust Automatic Cross-Domain Scale Alignment

Haoyi Zhao, Fa Foster Dai

Auburn University, Auburn, AL

The pipelined SAR ADC is a promising architecture to achieve high sample rate with high resolution. Residue amplifiers are normally required between pipelined stages to provide sufficient gain for relaxing the noise requirement in subsequent stages. However, these amplifiers generally induce issues such as large power consumption, stringent linearity requirements, and PVT-sensitive gain errors [1,4]. Moreover, reduced voltage dynamic range in deep submicron nodes presents challenges for the design of high-performance amplifiers and fine quantizers in voltage domain. Therefore, implementing the fine quantizer in time domain becomes attractive due to its better noise tolerance and lower power consumption. Nevertheless, the linearity and conversion speed of the time-to-digital converter (TDC) used as the fine quantizer degrades quickly with the increase of its resolution due to the exponentially increased hardware. Moreover, its full-scale and resolution are determined by the delay cells and are thus sensitive to PVT variations. In prior-art, the time-domain assisted SAR ADC [2] adopts a current-discharging-based inner-tracking technique in a voltage-to-time converter (VTC) and TDC to compensate PVT variations, yet the conversion speed is limited by slow conversions of the VTC and the TDC. The digital slope assisted SAR ADC [3] guarantees that the time full-scale is aligned with the LSB in the voltage-domain. However, the architecture doesn't fully exploit the benefits of time-domain conversion since the ADC resolution is still dependent on the unit-capacitor switching, leading to an enlarged MSB-to-LSB ratio in the CDAC.

To overcome the aforementioned challenges, this paper presents a ring-TDC-based fine quantizer as the second stage of the pipelined SAR ADC. The ring TDC employs only 9 delay cells configured in a ring to achieve 6b resolution. Reuse of the delay cells greatly enhances the TDC linearity with less area and power. The 9-stage ring TDC intrinsically includes 3b time-domain interpolations to further refine time resolution, while simultaneously achieving a large time conversion range. Most importantly, the presented architecture automatically matches one-lap delay of the ring TDC with the LSB in voltage-domain, resulting in auto-scale alignment between voltage and time domains over PVT variations.

The TDC-assisted pipelined SAR ADC depicted in Fig. 10.4.1 comprises a 7b coarse SAR ADC and a ping-pong switching passive pipeline interstage followed by duplicated sub-quantizers, which include two identical 6b ring-TDC-based time-quantizers with 1b over-range to tolerate the offset between coarse and fine stages. The operation of the time domain fine quantizer is illustrated in Fig. 10.4.2, where only a 4b SAR is shown for simplicity. After coarse conversion of the first-stage SAR ADC, the residue is transferred to a sub-CDAC in the fine quantizer through the passive ping-pong switching inter-stage [5]. When the inter-stage switch is turned off, a start signal T_p is fed to the ring TDC. Then, T_p starts to propagate in the delay ring repeatedly. Each time T_p reaches the start point of the ring, the counter records the number of laps it propagates, and a switching signal SW_p is generated by the sub-logic to switch one unit capacitor of the sub-CDAC from V_{refp} to V_{refn}, causing the voltage stored on the sub-CDAC to drop one step. Further propagation of signal T_p in the ring causes a stair-ramp decay of the voltage residue until it crosses the differential zero point, where a signal T_n is generated by the cross detector. Thus, the time-interval between T_p and T_n represents the residue signal transferred to time-domain, performing a VTC function. Note that the voltage-to-time transfer slope is dependent on the capacitor switching step as well as its switching time, which is the one-lap delay in the ring. The full-scale residual voltage stored on the sub-CDAC, which includes 8 unit switching capacitors, needs 8 steps to reach the differential zero. Thus, the architecture guarantees that the LSB in voltage domain is automatically aligned with the full-scale in time-domain regardless of PVT variations. Finally, the time-domain residue is measured as the number of propagated laps N_c plus the number of delays in the final lap d_f. The time resolution τ is therefore determined by the delay of a single delay stage, leading to time-interpolation beyond the lap delay that corresponds to voltage drop step. Moreover, the detectable range of the ring TDC can be infinite as long as the lap counter is sufficiently large, which enables fine resolution and large conversion range simultaneously, allowing more bits partitioned in time domain for improved performance.

The coarse SAR ADC in Fig. 10.4.1 employs the monotonic switching technique to enhance conversion speed and reduce the MSB-to-LSB ratio in the coarse CDAC. The CDAC performs split-switching to maintain constant comparator common mode. As for the pipeline interstage, one of the two sub-quantizers is connected to the first stage alternately to keep tracking the voltage residue, using the ping-pong switching technique [5]. The level shifting after the residue transfer guarantees a positive voltage residue above the differential zero for time-domain processing. The ring-TDC-based fine quantizer depicted in Fig. 10.4.3 includes a ring TDC, a TDC-controlled capacitor array (sub-CDAC), a crossing detector, and a sub-logic circuit. The ring-configured delay line requires an odd number of delay stages for proper signal propagation. To implement 3b time interpolation, 9 delay stages are employed in this design. The unit delay in the ring TDC, as illustrated in Fig. 10.4.3, is built with a NAND gate that allows the signal to propagate through once its input is set to "1". To achieve good VTC transfer linearity, a two-stage cross detector is adopted for high-gain with a bandwidth of 80MHz, which is much lower than the sub-CDAC switching frequency [3]. Arbiters are enabled only when T_n is generated to save power. Differential-pair-based arbiters are used instead of DFFs to avoid unwanted offsets. The digital outputs from the lap counter and arbiters are sent to the encoder that converts the raw data to 6b binary codes with 1b over-range.

The ring TDC operates similarly to the conventional single-line flash TDCs except that the delay cells are reused during the conversion. The ring TDC consists of only 9 delay cells for 6b time-domain conversion, while a single-line flash TDC would require 64 delay cells for the same conversion range. The small number of delay cells allows more compact layout and thus better TDC linearity. In addition, the standard deviation of the TDC INL, which can be calculated as $\sigma_{maxINL} = 0.5 * sqrt(n) * \sigma$ [3], is reduced by about 3 times when the number of stages, n, is reduced from 64 to 9. This becomes critical when delay mismatch worsens in deep submicron technology. Unlike a single-line TDC, where the DFF/arbiter works at a frequency set by TDC resolution ($1/\tau$), the ring counter works at a lowered frequency ($1/9\tau$) since it only needs to count the number of laps before T_n is generated. The arbiters are turned on to detect the location of the propagating pulse for time-interpolation in the last lap, which happens only when the cross-detector output is triggered. The delay of cross-detector output contributes only a DC offset, which can be calibrated together with other DC offsets. When the time resolution is shrunk to 20ps, the low-frequency counter greatly helps TDC power reduction, leading to an improved overall power efficiency of the pipelined ADC. Compared with a 6b flash TDC, the presented ring TDC quantizer uses only 1/7 of the area and about 1/2 of the power, in addition to its benefit of cross-domain auto-scale alignment for PVT robust performance.

The prototype of the 12b hybrid ADC is fabricated in a 22nm FDSOI technology. The ADC core occupies only $0.048mm^2$ as shown in Fig. 10.4.7. In this design, the input sampling capacitance is the total CDAC capacitance of 1.2pF. On-chip foreground calibration is performed before the measurement to correct offsets of the 1st-stage comparator and the 2nd-stage cross detector as well as the signal range offset between coarse and fine convertors. Since the interstage is passive and time-domain full-scale is auto-aligned with the coarse sub-range, no background calibration is needed for this design. The ADC consumes only 0.97mW from a 0.8V supply when operating at 260MS/s. Figure 10.4.4 shows the measured SNDR and SFDR versus input frequency and SNDR over supply and temperature variations. The SNDR degrades less than 1.5dB over 0.75~0.85V supply and 0~80°C ambient temperature variations, demonstrating PVT robust performance without background calibration. The measured spectra and DNL/INL are illustrated in Fig. 10.4.5. Measured DNL and INL are -0.54/+0.64LSB and -1.04/0.91LSB, respectively. With an input swing of 1.25Vpp at 3.9MHz, the measured SNDR of 63.5dB and SFDR of 79.3dB are achieved under 260MS/s sample rate. The measured performance is summarized in Fig. 10.4.6 with comparisons to state-of-art ADCs.

Acknowledgement:
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[2] M. Zhang, et al., "3.5 A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques," *ISSCC*, pp. 66-68, Feb. 2019.
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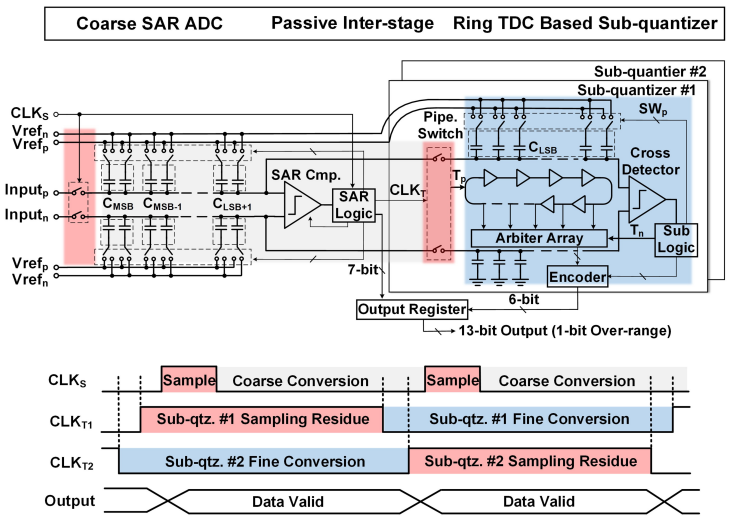

Figure 10.4.1: Block and timing diagrams of the prototype 12b pipelined SAR ADC with ring TDC based fine quantizer.

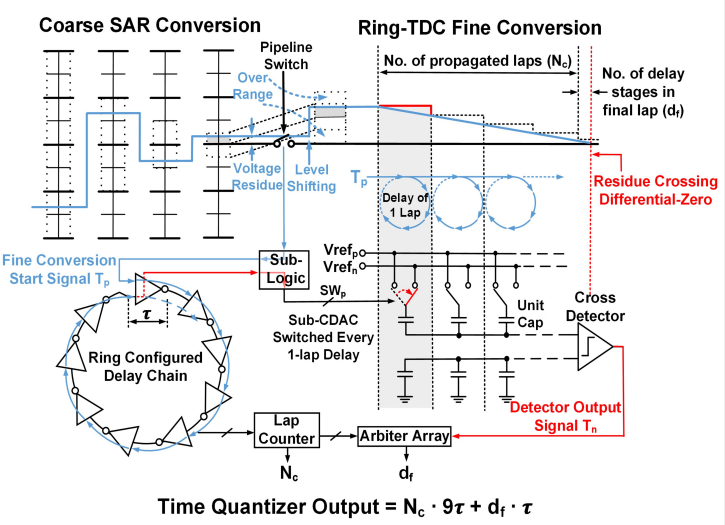

Figure 10.4.2: Illustration of ring TDC based fine quantizer and CDAC based VTC operations.

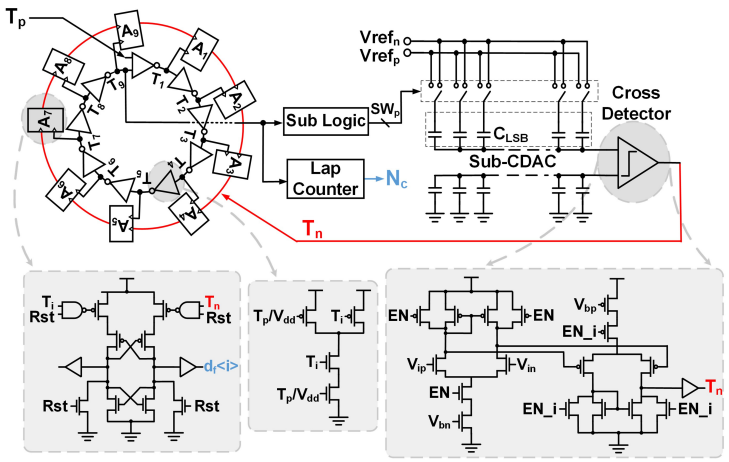

Figure 10.4.3: Block and circuit diagrams of the ring-TDC-based fine quantizer with cross detector, delay cells, and arbiters.

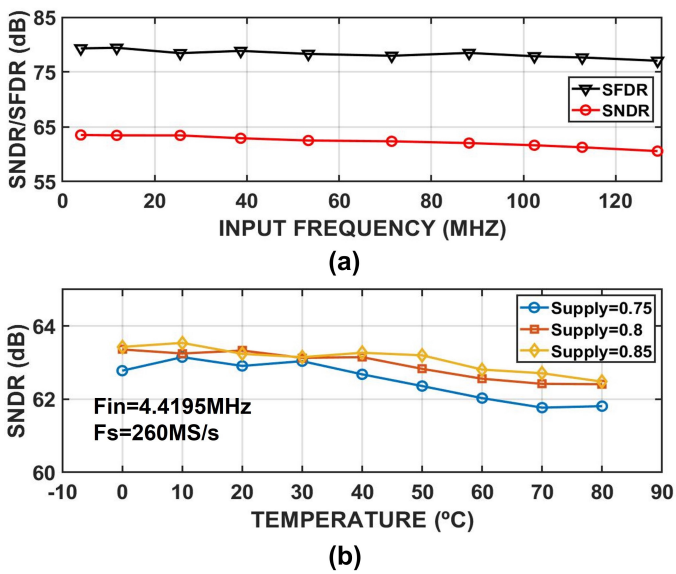

Figure 10.4.4: (a) Measured SNDR/SFDR versus input frequency; (b) measured SNDR over supply range (0.75-0.85V) and temperature variation (0-80 degrees).

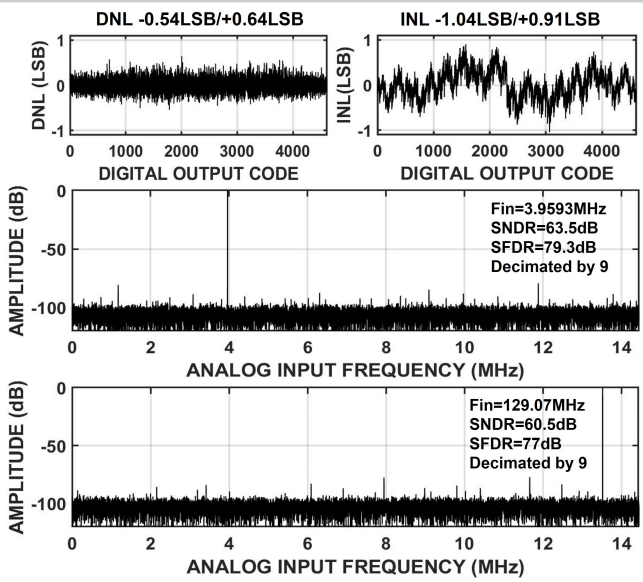

Figure 10.4.5: Measured DNL/INL and spectra with outputs decimated by 9 (32768 bins).

	This Work	[1] ISSCC2017	[3] ISSCC2016	[4] VLSI2019	[5] VLSI2014
Architecture	**Pipelined SAR-Ring TDC**	Pipelined SAR	Digital Slope-SAR	Pipelined SAR	Pipelined SAR
Process [nm]	**22**	65	28	40	65
Resolution [bit]	**12**	12	12	12	12
Supply [V]	**0.8**	1.3	0.9	0.9	1
Fs [MS/s]	**260**	330	100	200	210
Power [mW]	**0.97**	6.23	0.35	3.9	5.3
$SNDR_{LF}$ [dB]	**63.5**	67.7	65.67	61.1	63.48
$SNDR_{HF}$ [dB]	**60.5**	63.5	64.43	62.1	60.1
$FoM_{Walden\ HF}$ [fJ/c.s.]	**4.27**	15.4	2.63	19	30.3
$FoM_{Schreier\ HF}$ [dB]	**171.8**	167.7	176	166.2	163
Area [mm²]	**0.048**	0.08	0.047	0.026	0.48

Figure 10.4.6: Measured performance summary and comparison with state-of-art ADCs.

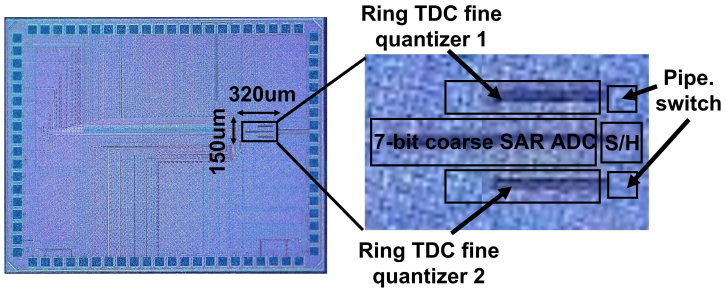

Figure 10.4.7: Die photo of the fabricated ADC prototype chip in 22nm CMOS.

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