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A dual-residue pipelined SAR ADC using only zero-crossing signals

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Abstract
This paper presents a dual-residue pipelined successive approximation register (SAR) A/D converter (ADC) that relaxes the accuracy requirement for residue amplifications and thus enables use of only zero-crossing (ZX) signals for the benefits of power efficiency and technology scalability. The dual-residue architecture is illustrated with design of an 11b two-step pipelined ADC consisting of 8b coarse and 5b fine (with 2b over-range) SAR sub-ADCs, which resolve 2b and 1b per SAR conversion cycle, respectively. Two ZX signals (or dual-residues) in opposite polarities automatically available in each 2b SAR cycle are sampled and held at the end of the coarse conversion for use as the full-scale reference for the fine SAR that quantizes a fixed input of zero. Simulations show that the ADC in 45 nm CMOS using typical open-loop circuits for inter-stage residue operation can achieve ENOB > 10 at 400 MS/s and Schreier FoM = 171.4 dB without residue gain calibration.

Keywords Pipelined ADC · Pipelined SAR ADC · SAR ADC · Dual Residue ADC · Dual Residues

1 Introduction

As pipelining being widely used in SAR ADCs to overcome the speed and resolution bottlenecks [1–12], issues associated residue generation and amplification for high-resolution (≥ 10b) pipelined ADCs come back to plague SAR ADC designs; and as a result, power efficient and technology friendly residue amplifiers (RA) continue to be a focus of research. In the past, zero-crossing detection (ZCD) based RAs [5, 13] were explored to eliminate the need for accurate and power-hungry settling of closed loop op-amps. Recently, open-loop dynamic amplifiers (DA) [3] and inverter-based ring-amps have become popular for minimizing RA power consumption and improving technology scalability [6, 14], where residue gain calibration and reference sharing [5] across pipeline stages are used to align the residue full scale (FS) with the succeeding fine quantization FS.

This work employs a dual-residue architecture where the alignment is automatic. The first attempt in this direction was made with an interpolation based dual-residue architecture [15] as is illustrated in Fig. 1, where the fine quantizations are carried out with interpolations between two adjacent coarse residues (e.g., $V1_a$ and $V1_b$) of opposite polarities. Since the difference of the dual residues determines the fine interpolation range, the residue FS and fine quantization FS are inherently aligned irrespective of the residue gain as long as it is the same for the two residues. Gain mismatch between the dual residues causes signal-dependent variation in the residue difference and should be limited within one LSB of the fine quantization. Even though this matching requirement can be readily met with integrated-circuit RA replicas for identical residue inputs, it imposes a challenge to the RA linearity as the two RA inputs could differ by as much as the ADC input FS. It is for this reason that the dual-residue architecture has not gained the expected popularity, though it was revisited recently for design of a calibration-free pipelined ADC [16].

Fortunately, the linearity issue can be mitigated using coarse SAR sub-ADCs that can generate arbitrarily small

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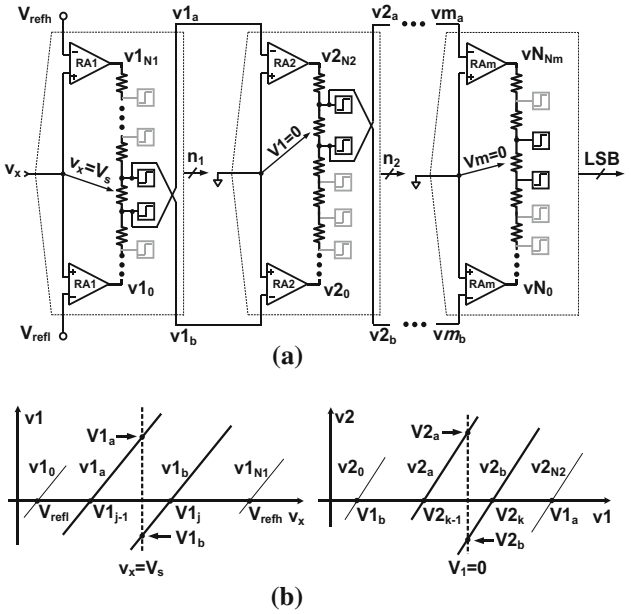

Fig. 1 An interpolation based dual-residue ADC **a** schematic [15] and **b** the residue signals in the first two stages of the sub-ADCs

residues with increasing SAR cycles. Based on this important observation, dual-residue SAR ADC architectures have been proposed [17, 18]. This paper details the design and operation principles using an 11b two-step pipelined dual-residue ADC as example that removes both the accuracy and linearity bottlenecks for residue amplification. Following a high-level extension of the dual-residue ADC concept in Sect. 2, the architecture and operation of the 11b ADC in a 45 nm CMOS process are presented in Sect. 3. The circuit designs are described in Sect. 4, with the required dual residue offset calibration included in Sect. 5. The simulation results are reported and compared with the existing dual-residue and SAR-assisted pipelined ADC counterparts in Sect. 6, followed by conclusions in Sect. 7.

2 Dual-residue extension

Residues are ideally linear zero-crossing (ZX) signals $v_i(-v_x–V_i)$ [19] that cross zero ($v_i = 0$) when the input v_x equals the quantization threshold V_i with the ZX slope equal to the residue gain A, i.e., $v_i = A*(v_x–V_i)$. For an n-bit dual-residue ADC with N + 1 quantization thresholds V_i (i = 0, 1, …, $N = 2^n$) the interpolation starts (as shown in Fig. 1) with generation of the two extreme ZX signals $v1_0 = A*(v_x–V_{refl})$ and $v1_{N1} = A*(v_x–V_{refh})$ by two replica RAs in the n1-bit first stage ($N1 = 2^{n1}$), where the ADC reference voltages $V_{refl} = V_0$ and $V_{refh} = V_N$ set the ADC input full-scale $FS = V_{refh}–V_{refl}$. By resistive interpolation between $v1_0$ and $v1_{N1}$, the ZX signals $v1_j$ (j = 1, 2, …, N1–1) for the coarse quantization are generated at the (N1– 1) taps across the first stage resistor string. The polarities of the ZX signals $v1_j$ are detected in parallel with regenerative latches for a given input sample $v_x = V_s$ to identify the string section that contains the zero of the first-stage string voltage v1. The two identified ZX signals, $v1_b = v1_j$ and $v1_a = v1_{(j-1)}$ that encompass the zero are amplified by the second stage RAs to drive the second stage string for fine quantization. The interpolated fine ZX signals $v2_k$ (k = 1, 2, …, N2–1, where $N2 = 2^{n2}$) and the fine dual residues $v2_a$ and $v2_b$ are generated in the second stage for the third-stage interpolation and quantization, and so on.

The first-stage RA (RA1) output must meet the highest (n-bit full resolution) linearity requirement over the full-scale input range. The second-stage linearity requirement can be relaxed by increasing the coarse resolution (n1), but to a limited extent constrained by the exponential growth in complexity, power, and input capacitance of the *parallel* interpolation based coarse sub-ADC. The RA linearity requirement and coarse sub-ADC complexity tradeoff can be avoided in principle using *serial* interpolation for efficient coarse quantization. This is possible based on an important observation that the flash-type sub-ADC stages in Fig. 1 can be black-boxed and substituted with any other types such as SAR ADCs as shown in Fig. 2, where the fine residues are generated by *serial* interpolations between the references for each stage. The first stage sub-ADC takes input signal v_x with the references connected to external sources. Starting the 2nd stage, the sub-ADC inputs are set to zero while the reference pins are connected to the dual residue outputs of the preceding stage.

In Fig. 2, the required dual residues are readily available from the three parallel ZX signals generated for the 2b/cycle conversion [20]. The costly RAs in the first stage of Fig. 1a are now replaced with two fixed voltage reference buffers without linearity requirement. The RA overheads of the following stages are drastically reduced by increasing the number of coarse SAR cycles so that the dual residues are arbitrarily small and linear without worsening the coarse sub-ADC complexity. As for the last stage without the need to generate the dual residues, a 1b/cycle SAR is better choice, because only one comparator offset needs to be calibrated. The INL degradation

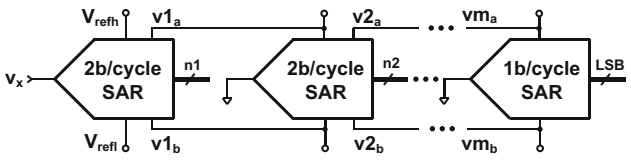

Fig. 2 Dual residue ADC architecture extended to use SAR sub-ADCs

by coarse comparator offsets can be avoided by over-ranging the succeeding fine stage.

With the RA accuracy and linearity bottlenecks both removed, the pipelined dual-residue SAR ADC preserves the ZX-only operation and power efficiency of SAR ADCs. In addition, sub-ADCs operating in different signal domains can be exploited with little concern about the accuracy of signal conversions, say, from the voltage to the time domain [9, 21] and vice versa. The resulted sub-ADC modularity thus opens a new dimension for design of pipelined ADCs.

3 Architecture and operation

Figure 3 shows the 11b ADC architecture consisting of an 8b SAR with bottom-plate sampling for 2b/cycle coarse quantization, a 5b SAR with 2b over-ranging for 1b/cycle fine quantization, and two parallel inter-stage T/H amplifiers for pipeline operation. The coarse and fine conversions are balanced in latency with 5 cycles each, including an extra cycle for dual-residue generation in the coarse conversion.

3.1 8b Coarse SAR

The input differential voltage $v_x = v_{ip}–v_{in}$ is sampled as V_s on the two capacitor DACs, $CDAC_a$ and $CDAC_b$, at the end of the track phase A ($\Phi_1 = 1$) by the bottom-plate switches S_{1e}, which are opened slightly earlier than the input top-plate switches S_{1t}. In the coarse conversion phase B ($\Phi_1 = 0$), the CDAC capacitor top plates are switched to either reference voltage V_{refl} or V_{refh}, generating the CDAC output ZX signal samples $V1_a = –(V_s–V_{ja})$ and $V1_b = –(V_s–V_{jb})$, where V_{ja} and V_{jb} are the quantization thresholds determined by the CDAC top-plate connections to the reference voltages in the j-th conversion cycle. The third ZX sample $V1_{ab} = –(V_s–V1_j)$ required for the 2b/cycle quantization is interpolated from $v1_a$ and $V1_b$ as shown in Fig. 3, where $V1_j = (V1_{ja} + V1_{jb})/2$. The three coarse comparators $cmp1_a$, $cmp1_b$, and cmp1 detect the polarities of the corresponding ZX samples at the end of each 2b conversion cycle and determine the CDAC top-plate reference connections for the next cycle ZX sample generation.

3.2 Dual residue generation and 5b fine SAR

After four cycles (j = 1 to 4) of conversions as shown in Fig., the coarse SAR enters cycle j = 5 in phase C ($\Phi_1 = 0$, $\Phi_2 = 1$) to generate ZX samples $V1_a$ and $V1_b$ as the dual residues for fine quantization. In the meantime, the fine quantizer enters its tracking phase D ($\Phi_2 = 1$) with the fine $CDAC_f$ top plates connected to a differential ground $V2_{CM}$ and the fine reference voltages $v2_0$ and $v2_{N2}$ tracking the dual residue generation through the inter-stage amplifiers

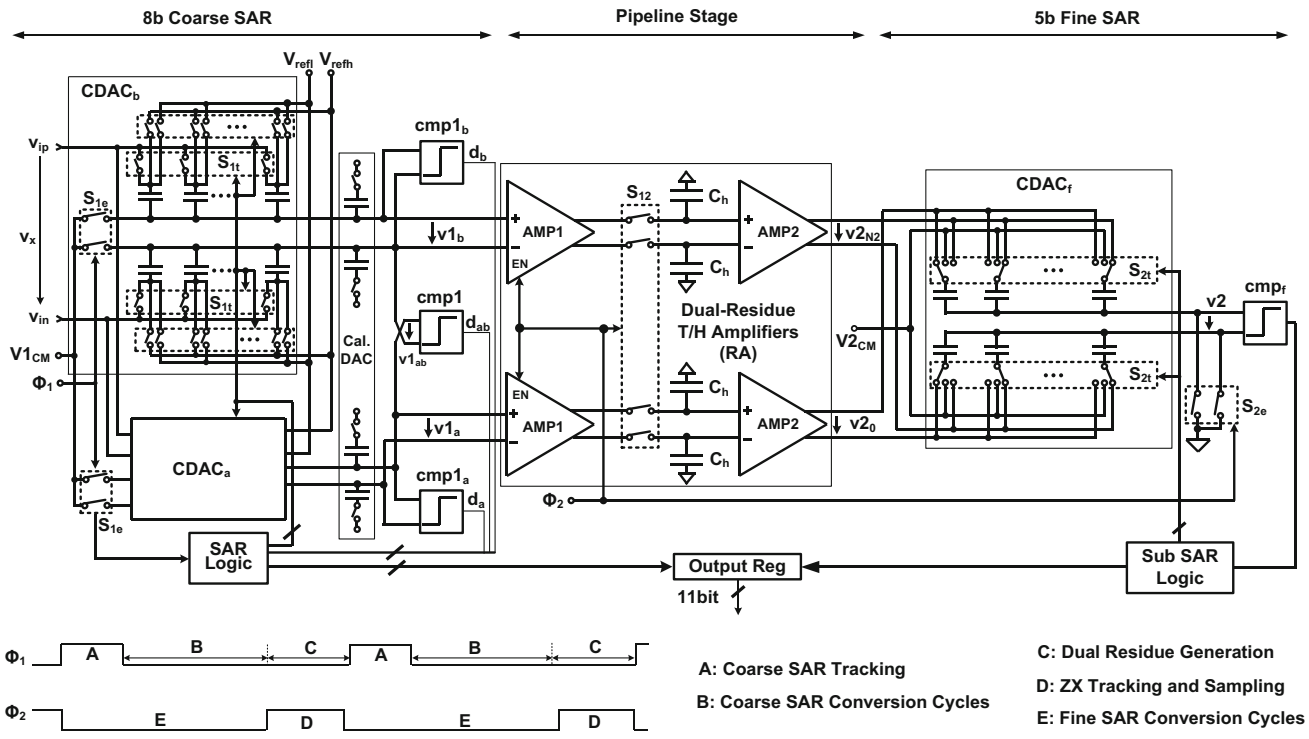

Fig. 3 Block diagram of the 11b prototype of the proposed pipelined dual-residue SAR ADC

AMP1 and AMP2. $V2_{CM}$ is set to match the AMP2 output CM to avoid CM jump at CMP_f input eliminating the need for low-impedance CM voltage source.

The 1b/cycle fine conversion phase E ($\Phi_2 = 0$) starts as Φ_2 falls, with the fine references $v2_0$ and $v2_{N2}$ sampled by S_{12} and held by C_h. Simultaneously, the $CDAC_f$ split-cap top plates are switched to $v2_0$ and $v2_{N2}$ by half and half, respectively, generating the first-cycle fine ZX signal $V2 = v2_1(v1 = 0) = -(0–V2_1)$ at the $CDAC_f$ bottom plate output, where $V2_1 = (v2_0 + v2_{N2}) / 2$ is the first fine quantization threshold. The fine comparator CMP_f detects the ZX polarity resolving the fine MSB and switches one of the fine MSB split caps from 0 to 1 or 1 to 0 for fine MSB = 0 or 1, respectively, generating the ZX signal for the second cycle conversion. This continues till the 5 fine bits are all resolved and the next tracking phase of the fine SAR starts.

3.3 2b Over-ranging

The 2b over-ranging extends the fine quantization FS from 8 to 32 LSBs, where one LSB = $2(V_{refh}–Vrefl) / 2^{11} \sim 0.6$ mV for the 11b prototype. This is realized by offsetting the ZX points that define the fine FS by –12 LSB and + 12 LSB, respectively, in the residue generation cycle j = 5 (Fig. 4). The offsets are injected with a small auxiliary CDAC in each of $CDAC_a$ and $CDAC_b$. As a result, total tolerance for the coarse comparator offsets and the coarse CDAC incomplete settling increases by 24 LSBs or + /–6 mV. The offset mismatch between the two residue paths is corrected with auxiliary CDACs to be described in Sect. 5.

4 Circuit implementation

In order to highlight the architecture benefits, simple open-loop switched-capacitor amplifier circuits that scale well with technology are adopted without aggressive circuit-level power minimization. The design considerations and circuit operations are described as follows.

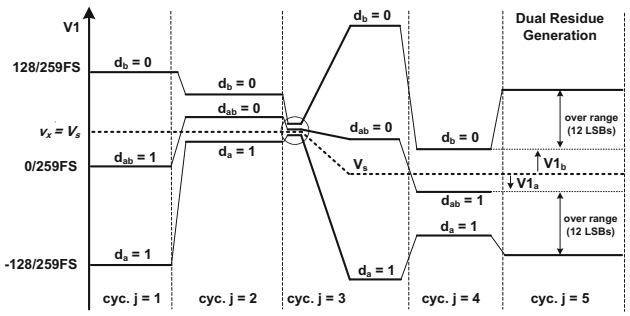

Fig. 4 Coarse quantization thresholds generated in each conversion cycle for a given input sample $v_x = V_s$

4.1 2b/Cycle CDAC capacitor splitting

The cycle-to-cycle threshold updates shown in Fig. 4 involve charge transfer among the CDAC capacitors, which consume dynamic power and cause settling issues. To minimize the charge transfer, the 1b/cycle split-cap scheme [22] is extended for use in this 2b/cycle SAR.

Figure 5 shows how the coarse CDAC capacitor array is divided in groups of different weights corresponding to the conversion cycles and how the top-plate connections of each group are switched from a preset initial state to a state determined by the comparator outputs ($d_b d_{ab} d_a$) for the cycle. The capacitor top-plate connection states are labeled with 0 or 1 to indicate connection to low or high reference voltages V_{refl} or V_{refh}, respectively. The $CDAC_a$ and $CDAC_b$ initial connections are complementary to each other.

The groups corresponding to cycle j = 1 ∼ 4 each consist of three identical capacitors with one of the capacitors in the first three groups split in weight by 1:3 for different initial connections, as is highlighted in the solid boxes. The connection state of the three identical capacitors (including the split capacitor) in each group is switched to equal the three comparator outputs (d_b d_{ab} d_a) or (d_a d_{ab} d_b) for $CDAC_a$ or $CDAC_b$, respectively, at the end of the corresponding cycle. The $CDAC_b$ positive side split capacitors are switched to equal d_b and the $CDAC_a$ counterparts are switched to equal d_a. This ensures the split capacitor switching that causes less charge transfer takes precedence over the switching of other capacitors in the group. The capacitor weights and connections define the quantization thresholds and the corresponding ZX points.

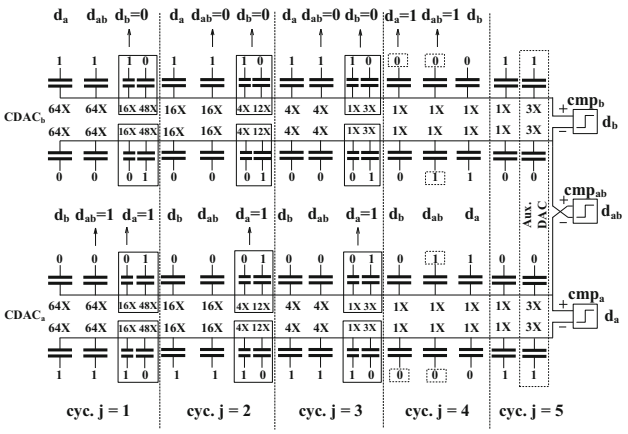

Fig. 5 The coarse CDAC capacitor top-plate initial connections to the references (0 for V_{refl} and 1 for V_{refh}) and the connection transitions for each conversion cycle given the same input sample $v_x = V_s$ as for Fig. 4

Each 0 → 1 (or 1 → 0) transition of a 1X weight differential capacitor pair corresponds to an increment (or decrement) of one coarse LSB.

Since the "0" connection state of each split capacitor in $CDAC_b$ is compensated with the same total weight of "1" connection states in the subsequent groups on the right-hand side, each group effectively has all the three connections preset to "1", and all the subsequent groups amount to one "0" connection. Therefore, each group in $CDAC_b$ generates a threshold at ¾ of the subrange for the corresponding cycle. Similarly, the same $CDAC_a$ group generates a threshold at ¼ of subrange due to the initial complementary connections. The midpoint threshold at ½ subrange is generated by interpolation of the $CDAC_a$ and $CDAC_b$ outputs. Upon sampling of the differential input, $CDAC_a$ and $CDAC_b$ top-plate connections are switched from the input to the preset initial state shown in Fig. 5, generating ZX signals at the CDAC outputs for the first cycle. The initial connections for each group in both $CDAC_a$ and $CDAC_b$ are overwritten at the end of the corresponding cycle as aforementioned. The total amount of charge transfer is greatly reduced not only because the switching of split capacitors causes less charge transfer but also because switching happens only once at most for each capacitor.

To meet the 11b kT/C noise requirement for ADC FS = 1.2 V_{ppd}, the total capacitance of $CDAC_a$ and $CDAC_b$ is chosen to be 500 fF (single-ended) each. Implemented with MOM capacitors, the CDAC is large enough to ensure 11b matching precision.

4.2 Auxiliary CDAC

A 3X capacitor is added at the LSB end of the capacitor array (Fig. 5) to act as the aforementioned auxiliary CDAC for 2b over-ranging. The 3X capacitor connection state is fixed to "1" in $CDAC_b$ and "0" in $CDAC_a$ such that 3X8 = 24 LSB extra spacing or over-range is automatically generated between the $CDAC_a$ and $CDAC_b$ output residues upon completion of the 4-cycle coarse conversion (Fig. 4). To compensate for the 3X capacitor impact on the coarse conversion, some capacitors for cycle 4 are flipped, as shown in the dashed boxes in Fig. 5, such that the total capacitance preset to 1 and 0 remains differentially unchanged for both CDACs.

4.3 Residue amplifiers and comparators

The residue amplifier schematic is shown in Fig. 6. It consists of AMP1 and AMP2 that amplify the coarse residue by 5X and 3.5X, respectively, and the open-loop switched capacitor circuit (S_{12} and C_h) that samples and holds the amplified residue signals for fine quantization. As

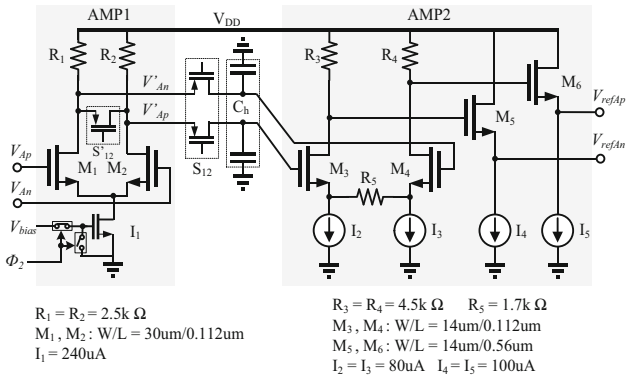

Fig. 6 Schematic of interstage residue T/H amplifier

a result of the residue amplification, the inter-stage hold capacitor C_h and the fine SAR $CDAC_f$ have very small capacitance of 30 fF and 40 fF, respectively. In the hold mode, switch S'_{12} is closed to short the AMP1 output for better isolation of C_h from the coarse SAR switching activities. In addition, a source follower output stage drives $CDAC_f$ for fast settling and for CM lowering that allows $CDAC_f$ top plates to be switched with simple NMOS FETs.

Given peak-peak differential (ppd) residue = 4*FS / 2^8 < 20 mV, the track switches S_{12} and S_{2t} (Fig. 3) seeing voltage swing less than 100 mVppd and 350 mVppd, respectively, meet the 5b linearity requirement with margin. Switch S_{2t} tolerates more voltage swing than S_{12} because $CDAC_f$ driven by the residue amplifier source followers settles much faster in the conversion phase E than C_h in the track phase D. AMP2 is source degenerated for extra margin in residue linearity. The size and currents are scaled as shown in Fig. 6 to meet the 11b input referred noise requirement. A foreground calibration loop to be.described in Sect. 5 cancels the amplifier input referred offset for 11b accuracy.

The coarse and fine comparators use the same strongArm dynamic latch with the transistors sized as shown in Fig. 7 to meet 1mVrms noise target. Startup offset calibration using capacitors attached to the intermediate differential nodes [23] reduces the comparator offset from 25 mV (3σ) to 2.5 mV. The offsets and noise do not cause ADC output error because they are all within the fine quantization over-range of ± 6 mV, where the extra margin covers incomplete settling of the coarse CDACs. The fine comparator noise and calibrated offset are negligible given the > 10X residue gain.

5 Dual residue offset calibration

The common part of the offsets in the dual residues maps to a DC offset in the ADC output, but the differential part directly adds to the fine quantization range, causing

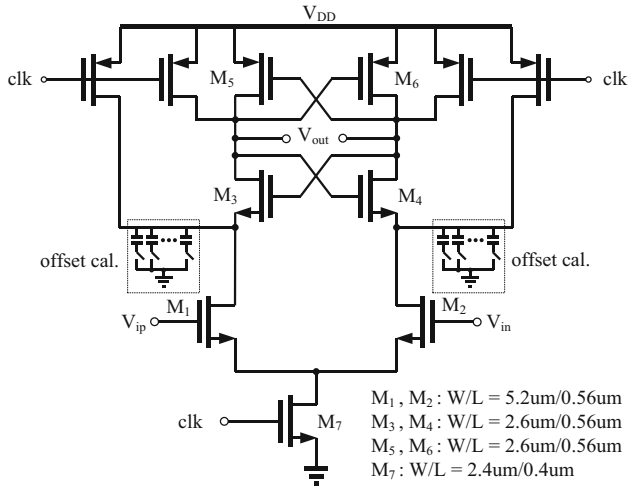

Fig. 7 Schematic of the strongArm latch comparator used in both coarse and fine SAR ADCs. Foreground offset calibration is carried out at startup

misalignment with the residue FS range and therefore additional quantization error. For INL less than one LSB, the differential offset should be less than one LSB = FS/2^{11} $\sim$ 0.6 mV. As shown in Fig. 8, a 5b calibration DAC is added to inject offset correction charge to the $CDAC_b$ and $CDAC_a$ outputs during the fine quantizer tracking phase ($\Phi_2 = 1$). It provides $\pm$ 9 mV correction range at the required sub-1 mV step to cover the simulated DC offset of σ = 2.5 mV in residue paths a and b.

The two paths are calibrated upon startup in two separate steps to remove the respective DC offsets as follows. The calibration mode is entered with $CAL_{en} = 1$, which shorts the ADC differential input to a common-mode voltage $V1_{CM}$. At the first Φ_1 falling edge after $CAL_{en} = 1$, the coarse quantizer samples the zero differential input onto the $CDAC_b$ capacitors for the calibration of path b. In the meantime, the coarse comparators are disabled and the calibration capacitor top plates are all connected to the low reference voltage V_{refl} with the 10 calibration registers holding the 5b correction code and its complement all reset to 0. At the Φ_2 falling edge, the inter-stage T/H samples and holds the $CDAC_b$ output, the $CDAC_f$ bottom-plate switches S_{2e} sample the zero differential input, and then the top-plate switches S_{2t} switch connection from the common mode voltage $V2_{CM}$ to the RA output $v2_{N2}$. After a preset short delay, the sampled offset voltage appearing at the $CDAC_f$ output is latched by the fine comparator cmp_f. At the next Φ_2 falling edge (i.e., $ck_{cal} < 4 >$ rising edge), the calibration DAC MSB register $D'cal < 4 >$ and the complement are updated with the comparator output D_{cal}. At the following Φ_2 rising edge, the calibration DAC subtracts or adds one MSB from or to the sampled offset for $D'cal < 4 >$ = "1" or "0". In two Φ_2 cycles, $D'cal < 3$

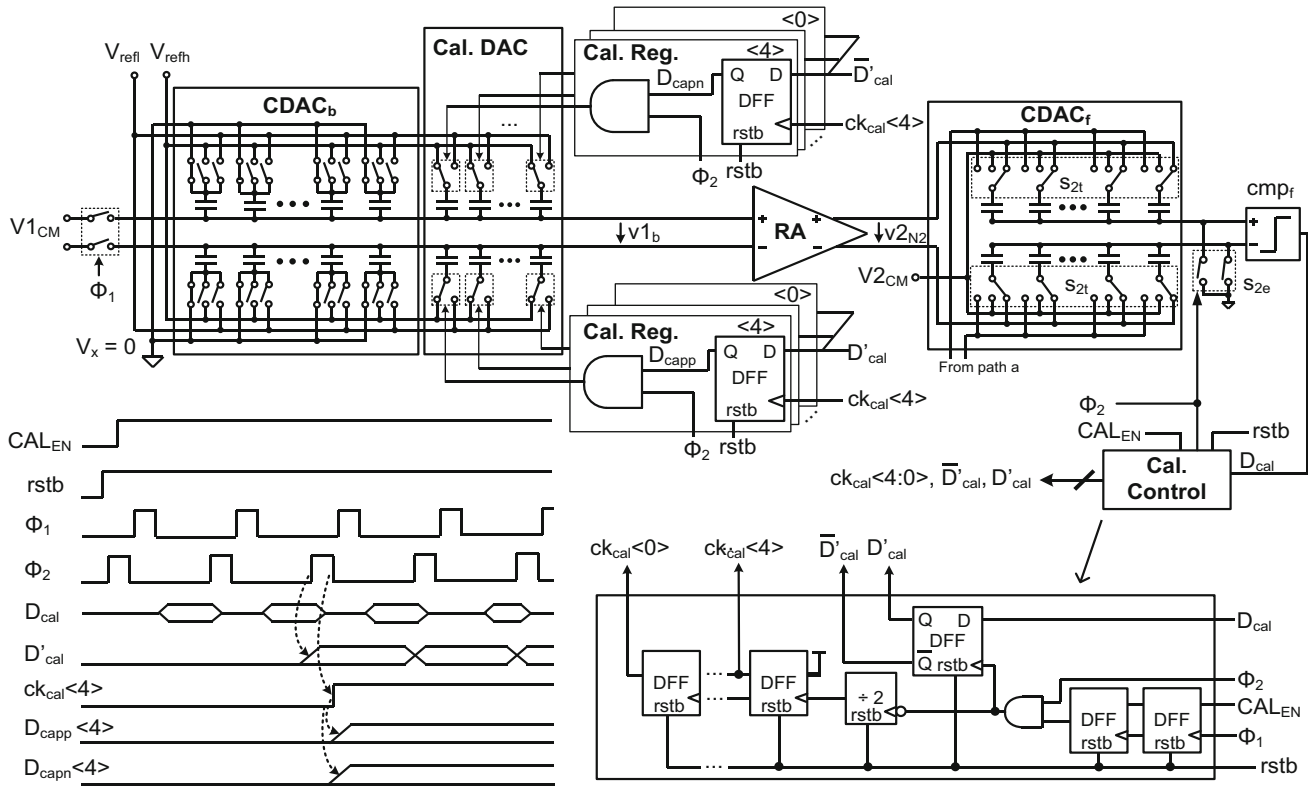

Fig. 8 Residue offset calibration illustrated for signal path b

$>$ is updated upon the rising edge of $ck_{cal} < 3 >$, and eventually, the 5b offset correction code for path b is resolved through this binary successive approximation process. This is then repeated to correct the offset in path a.

6 Simulation results

Designed in a 45 nm SOI CMOS process with an active layout area of 0.07 mm^2 (Fig. 9), the 11b ADC runs up to 400 MS/s and achieves a typical SFDR of 75.8 dB and ENOB of 10.24 based on Monte Carlo and typical corner simulations that include effects of thermal noise, random FET and resistor mismatch and back-annotated parasitics. The total power consumption, dominated by the RA and coarse SAR as shown in Fig. 10, is 3.16 mW, which corresponds to a Schreier FoM of 171.4 dB. The comparator offset calibrations improve the near Nyquist SNDR from 51.2 dB to 56.1 dB (Fig. 11 (a), (b)). The dual residue offset calibrations enhance it further to 63.4 dB (Fig. 11(c)), with the SFDR reaching 75.8 dB and 88 dB for Nyquist and low frequency inputs (Fig. 11(d)), respectively. Figure 12 shows the DNL and INL of the prototype ADC in one run of Monte-Carlo simulation after offset calibration. Figure 13 shows the SFDR and SNDR stay flat despite more than ± 25% variation in the RA gain over 100 °C temperature range. This confirms the robustness of the dual residue architecture against RA gain variations. The SFDR and SNDR over input frequency and sampling frequency are shown in Fig. 14.

Table 1 compares the ADC with some publications that represent the recent trends of pipeline ADCs. For FoM comparison, [16] and [3] are most relevant to this ADC due to similar technology in 40 nm, similar SNDR around 60 dB, and not much different speeds in hundreds of MS/s. It is unfair to compare the simulated results directly with the measured counterparts, but given one-bit ENOB reduction to account for silicon performance degradation, the resulted FoM = 171.4 – 6 = 165.4 dB for the prototype is still much better than the 155 dB Schreier FoM calculated for the latest dual-residue counterpart [16]. The lane speed is also faster (400 MS/s vs. 200 MS/s) than this

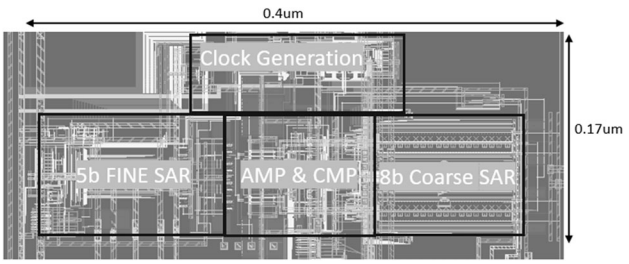

Fig. 9 ADC prototype layout

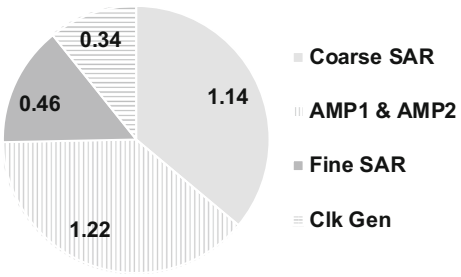

Fig. 10 Power Consumption breakdown (mW)

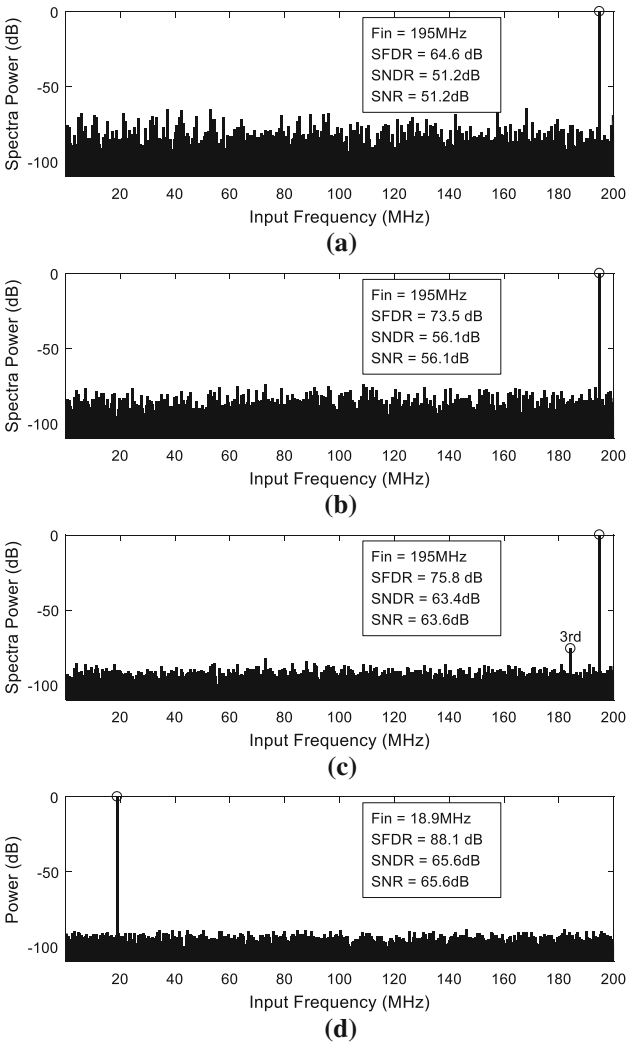

Fig. 11 Typical-corner output spectra from Monte-Carlo simulations of the prototype ADC running at 400 MS/s with **a** Nyquist input before offset calibrations, **b** after comparator calibrations, **c** after residue offset calibrations, and **d** low frequency input after all calibrations. Device random mismatch and thermal noise are included in the simulations

counterpart that uses multistage flash sub-ADCs. The better overall performance can be ascribed to the use of power efficient SAR sub-ADCs and simple open-loop RAs. Compared with [3] that uses power-efficient dynamic RA,

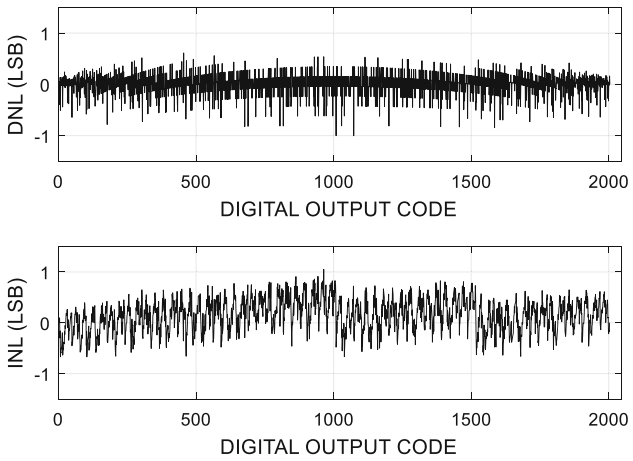

Fig. 12 Typical-corner DNL and INL from Monte-Carlo simulations of the prototype ADC after offset calibration

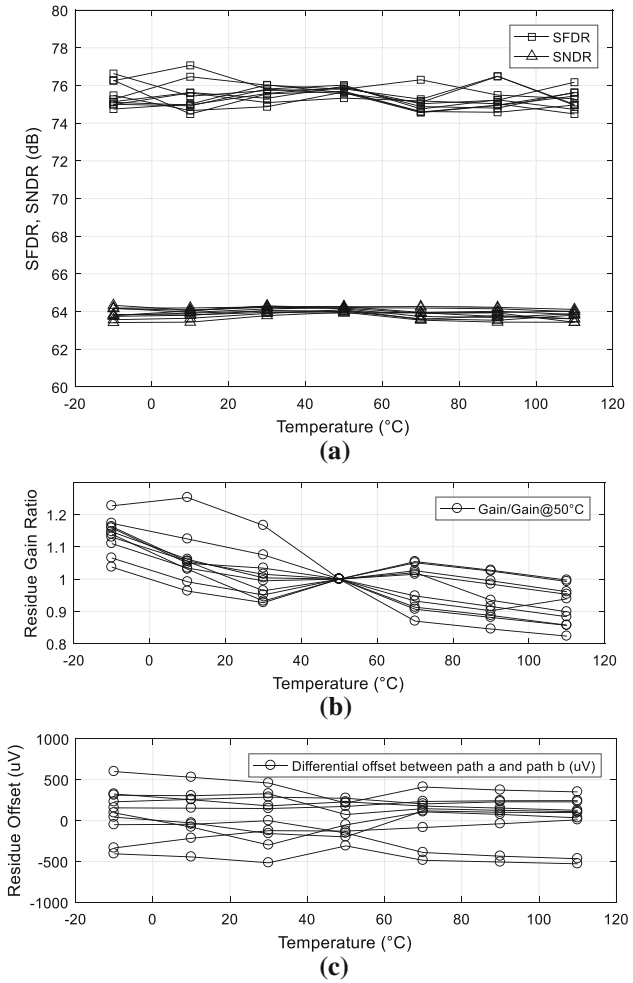

Fig. 13 Temperature dependence of **a** the typical-corner SFDR and SNDR, **b** residue gain, and **c** residue offset from Monte-Carlo simulations. The foreground residue offset calibrations are simulated at 50 °C

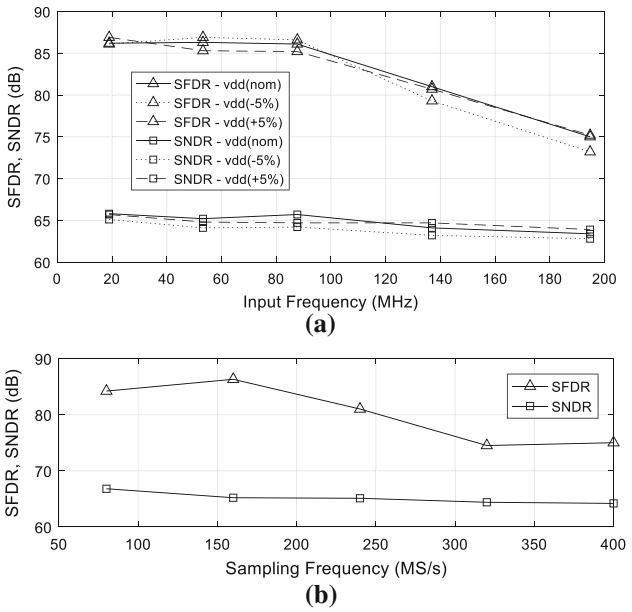

Fig. 14 SFDR and SNDR of ADC prototype vs. **a** input frequency with supply variation, sampling rate at 400MS/s, **b** sampling frequency

this prototype does not exhibit definite advantage in the FoM. However, it avoids the postprocessing used in [3] for residue gain correction, which would have significantly worsened the FoM if implemented on chip as background calibration to track out the impact of PVT variations. In contrast, the prototype can further enhance the FoM using dynamic RAs without any concern of background calibration.Compared with [5] where the RAs are based on low-power virtual ground ZCD, this prototype do without the need for use of a delicate current reference to overcome the reference disturbance triggered by asynchronous detections of virtual ground zero crossings in different pipeline stages and the need for the associated temperature compensation and reference trimming. When ringamps [6, 14] can deliver sufficient residue gain at the required accuracy and power efficiency, it is unlikely to get a FoM any better than [6] by going to dual residues. However, when speed is important, the proposed dual residue architecture could be a better choice because the RAs do not have to be tied to slow closed-loop operation as the ringamps do. The remaining two counterparts [10] and [12] in Table 1 both use open-loop RAs to get relatively higher conversion rates but necessitates residue gain adjustment against PVT variations.

Table 1 Pipelined ADC Performance Comparison

	This work*	Vecchi JSSC 2011 [16]	Verbruggen JSSC 2012 [3]	Kuppambatti JSSC 2014 [5]	Lim JSSC 2015 [6]	Kull ISSCC 2017 [10]		Wu JSSC 2019 [12]
Residue(s)	Dual	Dual	Single	Single	Single	Single		Single
Sub-ADC	SAR	Flash	SAR	SAR	SAR	SAR		SAR
Process (nm)	40	40	40	65	65	14		65
Resolution (bit)	11	12	11	12.1	13	10		12
Speed (MS/s)	400	800 (4-way)	250 (2-way)	50	50	1550	950	300
Full Scale (V_{ppd})	1.2	1.2	–	–	2.4	0.65	0.5	1.6
Supply (V)	1	1, 2.5	1.1	1.3	1.2, 0.8	0.95	0.7	1.2
SNDR (dB)	63.4	59	56	66	70.9	50.1	50.3	63.55
SFDR (dB)	75.8	70.1	67.13	77	84.6	–	–	–
Power (mW)	3.16	105**	1.7	4.8	1	6.92	2.26	12.5
FoM (dB)	171.4	155	164.7	163	174.9	160.6	163.5	164.3
Area (mm^2)	0.07	0.88	0.07	1.1	0.054	0.0016		0.5
Residue Amplifier	CML Open loop	Opamp Closed loop	DA Open loop	ZX based Closed loop	RingAmp Closed loop	CML Open loop		Opamp open loop
Residue Gain Adjustment	No	No	Post Processing	Ref. Trimming	No	Ref. calibration		Gain calibration

*simulation results, **including reference buffer

7 Conclusions

This paper extends the dual-residue architecture to use any sub-ADCs that can generate dual residues as reference for the succeeding sub-ADCs and to use any sub-ADCs that can take the dual residues as reference to terminate the pipeline. This extension allows use of efficient SAR sub-ADCs to remove the sub-ADC complexity and the RA linearity bottlenecks of the traditional parallel interpolation-based dual-residue ADCs. When small enough, the dual residues degenerate into the zero-crossing signals inherently available in multibit sub-ADCs, leading to much lower RA overhead. Small dual residues can be realized using a relatively high resolution 2b/cycle SAR sub-ADC for coarse quantization with little tradeoff in sub-ADC complexity and power efficiency. This results in a pipelined dual-residue SAR ADC architecture that preserves the SAR advantages of power efficiency and technology scalability using only ZX signals. The advantages are illustrated by design and comparison of an 11b pipelined two-step SAR to the state-of-the-art pipelined dual and single residue ADCs.

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Data availability The data that support the findings of this study are available from the corresponding author upon reasonable request.

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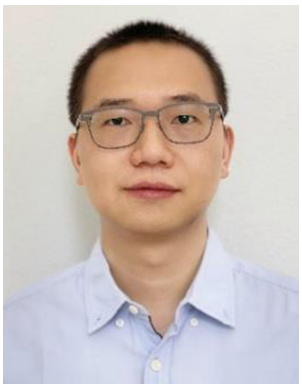

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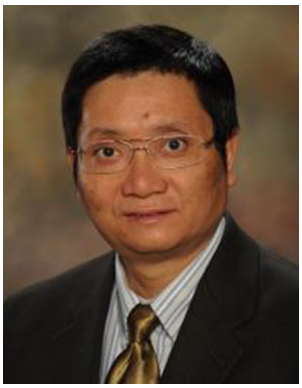

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