A Fractional-*N* Reference Sampling PLL With Linear Sampler and CDAC Based Fractional Spur Cancellation

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***Abstract*— In this article, a fractional-*N* reference sampling phase-locked loop (PLL) (RSPLL) is presented. A capacitor-based digital-to-analog converter (CDAC) is implemented at the output of the reference sampling phase detector (RSPD) to cancel the divider quantization error in fractional mode. The RSPD is linearized by maintaining a constant discharge current from the sampling capacitor. Although the discharging current source may induce some noise compared to a sampling PD. However, its noise can be effectively suppressed with the high-gain setting for the RSPD when the loop is in lock. The linear range of RSPD can be programmed to cover the quantization error in a frac-*N* mode without degrading the PLL in-band phase noise. To mitigate the nonlinearity of RSPD, the CDAC is implemented with a high-order cancellation scheme using only one capacitor array but multiple reference voltages. The prototype chip was fabricated in a 45-nm partially depleted silicon-on-insulator (PDSOI) CMOS process. The measurement showed an output frequency range covering 7.7–9.1 GHz with an integrated jitter (10 kHz–50 MHz) of 135 fs and an in-band fractional spur level of −55 dBc at an offset frequency of 50 kHz. The entire PLL consumes 4.5 mW and achieves an figure of merit (FoM) of −250.8 dB.**

***Index Terms*— Capacitor digital-to-analog converter (DAC), frac-*N*, phase noise, phase-locked loop (PLL), reference sampling, spur cancellation.**

I. Introduction

AS THE clock source for RF transceiver, phase-locked loop (PLL) jitter, and spurious tones plays a pivotal role in terms of the signal-to-noise ratio (SNR) performance of the entire RF chain. For the next-generation 5G RF transceiver design, the local oscillator (LO) needs to provide a clock over 28–40 GHz. It is very challenging to directly synthesize clock at this target frequency as the quality factor of integrated inductor and capacitor degrades quickly at millimeter-wave (mm-wave) frequency. Alternatively, using two cascaded synthesizer stages can generate a mm-wave clock with lower overall jitter and power consumption [1]–[3]. The first stage consists of a closed-loop structure to generate a clean intermediate frequency with a very fine frequency step. The second stage consists of an open-loop structure such as injection locking with a fixed frequency multiplication ratio to up-convert into the mm-wave frequency. This avoids power-hungry components such as divider at mm-wave frequency. As the second stage usually involves a small frequency multiplication factor, the phase noise of the final mm-wave clock is mainly determined by the intermediate clock from the first stage; thus, it is crucial for the first stage PLL design to be low-jitter and low-spur while providing a fine frequency resolution.

Sub-sampling PLL (SSPLL) [4] can achieve a very low in-band noise floor by directly sampling the voltage-controlled oscillator (VCO) output. The simplicity of using a sample and hold (S&H) circuit as phase detector (PD) not only contributes low noise (sampling noise kT/C) but also provides a large gain that helps suppressing the noises from subsequent stages including the charge pump (CP). Conventional PLL achieves fractional operation with delta-sigma modulator (DSM) controlled multi-modulus frequency dividers. The divider quantization error is pushed to higher frequency through DSM noise shaping and is further suppressed by the loop filter (LF). In this case, the PD needs to cover the residual phase error after lock-in which spans over several VCO periods. The same structure is difficult to be implemented with a sub-sampling phase detector (SSPD) since its detection range is only half the VCO period. In state-of-the-art frac-*N* SSPLL designs, an explicit alignment between the reference edge and the VCO edge is usually implemented before sampling as shown in Fig. 1. In [5], a digital-to-time converter (DTC) is used to cancel the quantization error. DTC suffers from nonlinearity issues and requires a large dummy loading capacitor to improve its linearity and noise. Placing delay lines on the reference path often deteriorates the PLL in-band noise performance, which is the main reason for using an SSPLL. Alternatively, Ru *et al.* [6] and Narayanan *et al.* [7] use a phase interpolator (PI) to generate sub-phases of the VCO clock. However, PI requires higher power consumption as it is operating at the VCO frequency. A passive PI can also be implemented to save power at the cost of the extra area from additional capacitors in PI [8]. In the aforementioned schemes, the frac-*N* induced quantization error is canceled in the time domain. In this article, we present a different approach where the quantization error is tackled in the voltage domain at PD output. Benefits of this approach include: 1) avoiding using DTCs before sampling and thus minimizing their noise contributions to frac-*N* in-band noise; 2) operating at reference frequency with low power; 3) sharing capacitors between the sampler and

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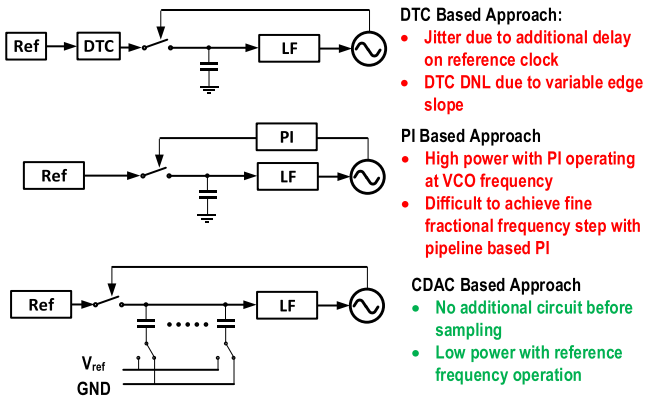


Fig. 1. Conceptual diagram of different approaches to achieve fractional-N operation for a sampling PLL.

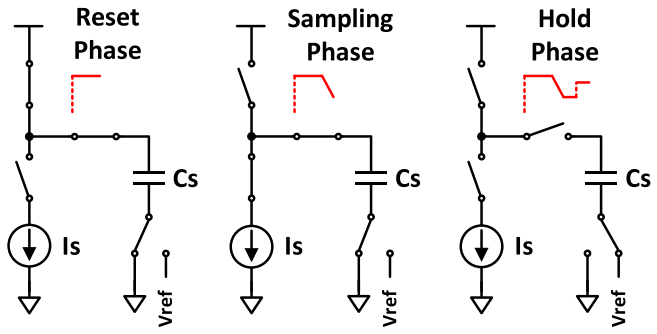


Fig. 2. Conceptual illustration of the proposed sampler and CDAC operation.

the quantization error canceller with low hardware overhead; and 4) achieving high linearity and thus low spur level with the capacitor-based digital-to-analog converter (CDAC) spur canceller.

This article is an extension of our previous conference article [9] and is based on an additional taped-out design with a revised PD structure that provides improved linearity and spur-cancellation. A CP is also implemented to replace the switch capacitor-based LF, shifting the loop from a type-I PLL presented in [9] to a type-II structure without intrinsic phase error. This article is organized as follows. Section II analyzes the impact of our proposed sampler and CDAC canceller on noise and fractional spur performances. Section III presents circuit implementation details of the proposed fractional-N PLL; the measurement results and conclusions are given in Sections IV and V, respectively.

II. Proposed Fractional Mode and Spur Mitigation

A. Operation of CDAC Based Fractional Spur Cancellation

An alternative approach for fractional SSPLL is to put the quantization error cancellation circuits at the sampler PD output. This has the benefit that noise in subsequent stages including canceller can be suppressed by the large sampler gain. However, this is difficult to accomplish due to the narrow detection range of SSPD which spans only half a VCO cycle. As the phase error exceeds this range, the loop will lock to the adjacent VCO zero crossings and cause locking to its harmonics. Using the reference sampling architecture [10], which is a variant based on SSPLL, the phase detection range can be adaptively adjusted and extended to one reference cycle, within which the polarity of instantaneous phase error can be correctly detected. Its bang-bang behavior beyond linear range helps to lock robustness and avoids using an extra frequency lock loop. However, the linear detection range of the reference sampling phase detector (RSPD) is still limited to the rising or falling time of its sampled edge. Its linear range can be extended by slowing down the reference edge.

Provided that the RSPD has enough linear range to cover the phase error caused by the frac-N operation, namely one VCO cycle, the RSPD can accurately convert the time domain phase error into voltage domain for frac-N operation. In general, the RSPD output voltage contains both random jitters due to loop phase error and deterministic jitter induced by divider quantization error. To suppress the fractional spur, the sampled voltage resulting from the deterministic jitter, revealed as a periodic ramp on the sampled voltage, needs to be removed. In our proposed design, a CDAC is implemented at the sampler output to compensate for the divider quantization error. The instantaneous divider quantization error obtained from the frac-N accumulator is fed into the CDAC controller to generate the anti-ramp waveform on the sampling capacitor. The mechanism that the CDAC is controlled is similar to that in a successive approximation (SAR) analog-to-digital converter (ADC) as elaborated below.

In the reset phase, the CDAC top plate is recharged to a fixed voltage while the switches on the bottom plate are reset and prepared for the next sampling cycle as shown in Fig. 2. In the sampling phase, the CDAC capacitor is discharged by the current source inside the sampler. The discharging starts at the reference edge and ends at the edge of a gated VCO clock. Thus, the instantaneous time-domain phase error between the VCO edge and the reference edge is converted to the voltage domain with a conversion gain, or the loop feedback gain, defined as follows:

$$\beta_{\text{sp}} = \frac{dV_{\text{Samp}}}{d\varphi_{\text{VCO}}} = \frac{S_{\text{samp}}}{\omega_{\text{vco}}} = \frac{I_S}{C_S}\frac{1}{2\pi f_{\text{vco}}} \tag{1}$$

where S_{samp}, I_S, C_S, and f_{vco} represent sampled waveform's edge slope, sampler discharge current, sampling capacitor, and VCO frequency, respectively. Assuming $I_S = 0.5$ mA, $C_S = 500$ fF, $f_{\text{vco}} = 8$ GHz, we can get a conversion gain β_{sp} of 0.02 and a S_{samp} of 1 GV/s. In the following analysis, we will use these assumptions.

In the hold phase, the top plate is disconnected from the sampler and the bottom plate is toggled between the ground and the reference voltage. An integrated CDAC control logic converts the instantaneous divider quantization error available from the fact-N accumulator into the digital control for each bit in the CDAC. An n-bit CDAC can generate a quantization error cancellation waveform for a fractionality lower than $1/2^n$, assuming the canceller gain is precisely calibrated. Thus, the residual voltage only contains a random phase error. Furthermore, in an analog PLL, the residual analog error voltage is not quantized to avoid ADC/time-to-digital converter (TDC) related quantization noise in contrast to the case of digital PLLs [11]–[13]. As the fractionality increases, the number of the bits in CDAC needs to be increased accordingly.

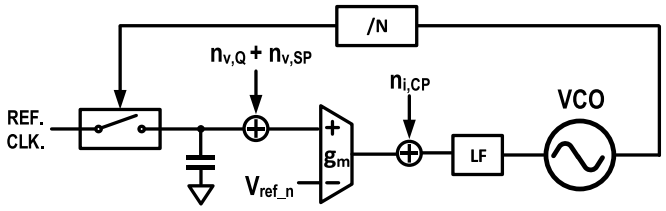


Fig. 3. In-band noise model of the proposed RSPLL.

Since the increase of CDAC bits is costly, for even finer fractionality, the truncation is required while converting the quantization error into CDAC control bits. Another benefit of choosing CDAC is to reuse its capacitor array for the sampling capacitor to save the die area. The extra circuits required are just switches and digital control logic to toggle the capacitors. Additional reference voltage generators are also required. However, compared to a full SAR ADC, this CDAC equivalently has only one conversion cycle over one reference period, allowing ample time for the reference voltage to settle after the switching.

B. PLL Noise Impact With Programmable Sample Edge Slope

As previously discussed, to enable quantization error cancellation at the RSPD output, the sampled reference edge slope needs to be slowed down in order to obtain a larger RSPD linear range. In this section, we discuss the effect of the sampled edge slope on the PLL phase noise. Referring to Fig. 3, the most significant PLL in-band noise contributors are the reference clock, sampler, and CP (differential g_m cell). The divided VCO clock is used to sample the reference clock edge. The sampled voltage is connected to the positive input of the CP, whereas the negative input is connected to an external bias voltage $V_{\text{ref\_}n}$. Assuming ignorable input offset voltage in g_m cell, the sampled voltage settles down to $V_{\text{ref\_}n}$ after lock-in. The sampler noise voltage at its output can be shown as follows:

$$n_{v,\text{Sp}}^2 = \frac{kT}{C_S} + \frac{4kT\gamma\, g_{m,\text{sp}} t_{\text{res}}}{C_S^2} \tag{2}$$

in which $g_{m,\text{sp}}$ and t_{res} represent the trans-conductance of the current source and the residual discharging time after lock-in. In (2), the first term represents the sampler noise as in an SSPLL and the second term represents the additional channel thermal noise from the discharging current source. The current source noise is a function of t_{res} as this is the result of integrating a white noise current into the sampling capacitor. As shown in Fig. 4, in every reference cycle, the sampler output is the first reset to an external voltage V_{charge}. At the falling edge of the reference clock, the sampler starts to discharge the sampling capacitor. The discharge stops at the falling edge of the divided VCO clock. When the loop is in lock, the sampler output is discharged to $V_{\text{ref\_}n}$ to maintain constant VCO tuning voltage. In this regard, a residual time interval $t_{\text{res}} = (V_{\text{charge}} - V_{\text{ref\_}n})/S_{\text{samp}}$ remains after lock-in. The PLL in-band noise contribution from the sampler can thus be found out as follows:

$$L_{\text{in-band,Sp}} = \frac{n_{v,\text{Sp}}^2}{2\beta_{\text{Sp}}^2 \frac{f_{\text{ref}}}{2}} = \frac{kTC_S\omega_{\text{vco}}^2}{I_S^2 f_{\text{ref}}} \cdot \left(1 + \frac{4\gamma\, g_{m,\text{sp}} t_{\text{res}}}{C_S}\right) \tag{3}$$

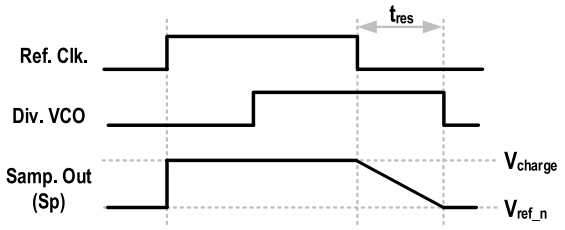


Fig. 4. Timing diagram of sampler input (reference clock and divided VCO clock) and sampler output after lock-in.

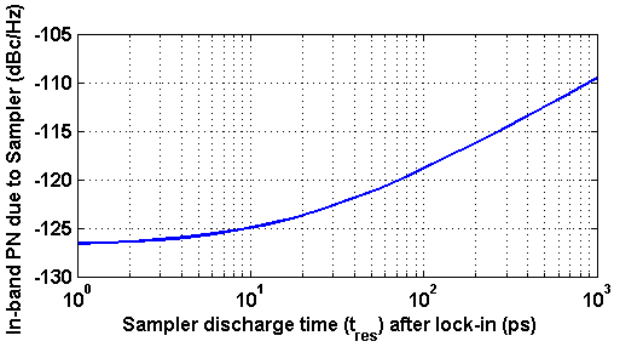


Fig. 5. PLL in-band noise floor at 8 GHz due to sampler versus residual sampler discharging time.

where f_{ref} denotes the reference clock frequency. With a f_{ref} of 100 MHz, the calculated sampler noise level is plotted in Fig. 5. With a t_{res} smaller than 10 ps, the sampler noise is dominated by the sampling noise kT/C, which is similar to an SSPD. As t_{res} keeps growing, the noise from discharge current source starts to dominate. In this case, the sampler noise's behavior is similar to a conventional phase frequency detector (PFD) and CP. However, there are a few distinct differences: 1) the minimum t_{res} in a conventional PFD is usually limited to five gate delays [14], or about 100 ps in this technology. In this design, t_{res} can be tuned close to zero by setting $V_{\text{charge}} = V_{\text{ref\_}n}$ as the clocks are directly applied to the sampling switches. In reality, V_{charge} needs to be slightly higher than $V_{\text{ref\_}n}$ to guarantee locking robustness; 2) as only discharging is needed in the proposed topology, the number of noise contributing devices is about half compared to that in a conventional CP. Furthermore, issues associated with a conventional CP such as up and down current mismatches no longer cause any problem; and 3) in some conventional CP PLLs, the sink and source current sources are always on for fast current switching [15]. In our case, the added current source is only enabled during discharging, which saves power. Even though there will be some delays at the beginning of the discharge due to finite current source turn-on time, its impact on our design is signal independent that is equivalent to adding a constant offset to the sampler output voltage. The foregoing analysis applies to integer mode only. In frac-N mode, as a residual phase error of one VCO cycle t_{vco}exists after lock-in, the sampler output fluctuates around $V_{\text{ref\_}n}$; thus, a minimum discharging time of $t_{\text{res}} = t_{\text{vco}}/2$ is required, or 62.5 ps at the 8-GHz output. However, the increase of t_{res} in frac-N mode only slightly degrades the in-band noise. The sampler noise at the PLL output is about -120 dBc/Hz in this design.

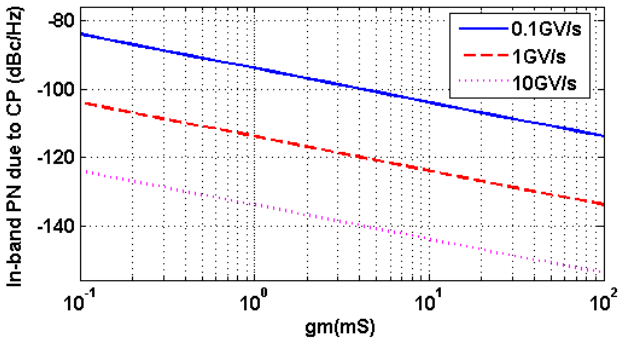


Fig. 6. PLL in-band noise floor at 8 GHz due to CP versus varying sampled edge slope and CP trans-conductance.

To achieve optimal cancellation, the reference voltage for CDAC can be tuned so that its full range equals the maximum residual voltage at sampler output in frac-N mode. The peak-to-peak residual phase error after lock-in is one VCO period $t_{\rm vco}$. Converting this to the voltage domain with the sampler gives a peak to peak residual voltage of $t_{\rm vco}\cdot S_{\rm samp}$. The quantization noise due to truncation in the CDAC equals

$$L_{\rm in-band,\,Q}=\frac{n_{v,Q}^2}{2\beta_{\rm Sp}^2\frac{f_{\rm ref}}{2}}=\frac{\frac{(t_{\rm vco}S_{\rm samp}/2^{N_b})^2}{12}}{\left(\frac{S_{\rm samp}}{\omega_{\rm vco}}\right)^2 f_{\rm ref}}=\frac{\pi^2}{3\cdot 2^{2N_b}f_{\rm ref}} \quad (4)$$

where N_b denotes the CDAC number of bits. Using the same parameter as in previous equations, an 8-bit CDAC can achieve a PLL in-band noise floor of -122 dBc/Hz.

Finally, the in-band noise floor due to CP can be shown as follows:

$$L_{\rm in-band,CP}=\frac{n_{i,\rm CP}^2}{2\beta_{\rm CP}^2}=\frac{n_{T,\rm CP}\cdot 4kT\gamma\, g_m D_{\rm CP}}{2\left(\frac{S_{\rm samp}}{\omega_{\rm vco}}g_m D_{\rm CP}\right)^2}=\frac{4kT\gamma\, n_{T,\rm CP}}{g_m D_{\rm CP}\left(\frac{S_{\rm samp}}{\omega_{\rm vco}}\right)^2} \quad (5)$$

where $n_{i,\rm CP}$ and $\beta_{\rm CP}$ represents the noise current at the output of the CP and the loop gain from the PLL output to the CP's output, respectively; g_m, $D_{\rm CP}$ denote the trans-conductance and the turn-on duty cycle of the CP, respectively. $n_{T,\rm CP}$ accounts for the number of noise contributing devices in the CP. Assuming $D_{\rm CP}=5\%$, $\gamma=1.1$, $n_{T,\rm CP}=9$. The calculated in-band noise results are shown in Fig. 6. Faster sampled edge slope $S_{\rm samp}$ leads to higher sampler gain and lower CP noise contribution. With an edge slope of 1 GV/s, or 1 ns rise/fall time, the in-band noise floor remains below -120 dB/Hz with a g_m larger than 4 mS. Assuming half of the edge transition time is utilized, this provides a linear range of 500 ps which is sufficient to cover a VCO frequency higher than 2 GHz for frac-N operation.

C. Sampler Linearity and Higher-Order Spur Cancellation

To improve the linearity of the sampler for frac-N spur cancellation, the reference buffer consisting of differential pair in our previous design [9] has been replaced with a current source-based sampler. Thus, instead of relying on a resistor to discharge the sampling capacitor, where the discharging

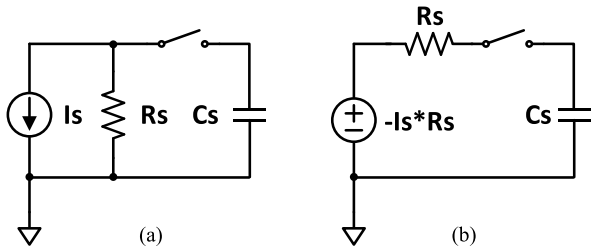


Fig. 7. (a) Simplified model of RSPD sampler. (b) Equivalent Thevenin model.

follows a nonlinear exponential function over time, a constant current is drawn from the sampling capacitor. The discharge current variation is hence minimized until the sampled voltage reaches the minimum $V_{\rm DS}$ voltage headroom ($\sim$100 mV) of the current source. Thus, the variation of the sampled edge slope is reduced by using the constant current source for discharging.

During the sampling phase, the current source in the sampler discharges the sampling capacitor. With an ideal current source, a constant current leads to a constant sampled edge slope, thus achieving linear conversion gain from phase error to sampled voltage. However, a real current source suffers from finite output impedance, thus introducing $V_{\rm DS}$ dependent nonlinearity. Discharging sampling capacitor with the current source-based sampler can be analyzed with the simplified model as shown in Fig. 7. Here, R_s represents the output impedance of the discharging current source. Converting to its equivalent Thevenin model, the voltage on the sampling capacitor can be shown as follows:

$$V(t)=(V_0+I_S R_S)e^{-\frac{t}{\tau}}-I_S R_S \quad (6)$$

where V_0 represents the initial voltage on the sampling capacitor, and τ means the sampler time constant $R_S C_S$. The exponential term in (6) can be expanded into its Taylor series expansion as follows:

$$V(t)=V_0-(V_0+I_S R_S)\left(\frac{t}{\tau}+\frac{t^2}{2!\tau^2}-\frac{t^3}{3!\tau^3}+\ldots\right). \quad (7)$$

Discharging starts from $t_0=0$ and stops when $V(t)$ reaches V_1 ($V_1<V_0$), or $t_1\approx C_S((V_0-V_1))/(I_S)=t_{\rm VCO}$. Assuming a fractionality of K, the actual sampled quantization error on Sp is the sampled voltage of (7) over reference cycles, namely

$$V_k=V_0-(V_0+I_S R_S)\left(\frac{\frac{k}{K}t_{\rm vco}}{\tau}+\frac{\left(\frac{k}{K}t_{\rm vco}\right)^2}{2!\tau^2}-\frac{\left(\frac{k}{K}t_{\rm vco}\right)^3}{3!\tau^3}+\ldots\right) \quad (8)$$

where $k=0$–$K-1$ for synthesizing frac-N frequencies. In the following analysis, the continuous approximation (7) is used for simplicity. Now integrating (7) over $t_0 t_1$, we can get the

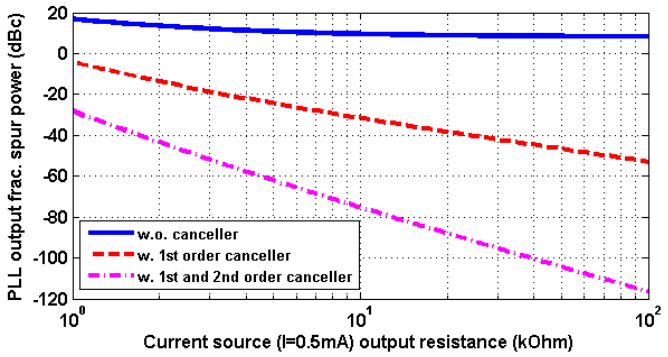


Fig. 8. Calculated total fractional spur power at PLL output with higher-order cancellation versus current source output resistance.

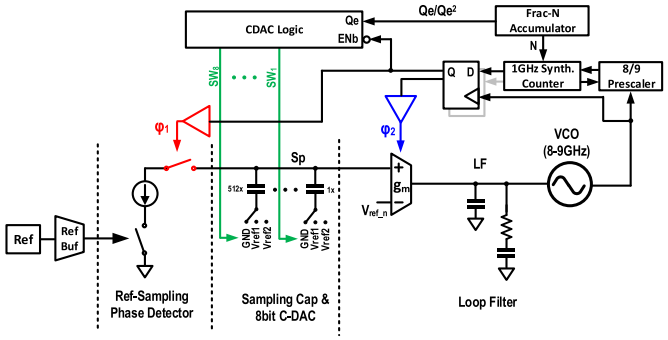


Fig. 9. Block diagram of the proposed frac-N type-II RSPLL architecture with CDAC quantization error cancellers.

rms power of each order as follows:

$$P_{1,\mathrm{rms}}{}^2 = \frac{(V_0+I_S R_S)^2}{t_1-t_0}\int_{t_0}^{t_1}\left(-\frac{t}{\tau}\right)^2 dt = (V_0+I_S R_S)^2\frac{t_{\mathrm{VCO}}^2}{3\tau^2} \tag{9}$$

$$P_{2,\mathrm{rms}}{}^2 = \frac{(V_0+I_S R_S)^2}{t_1-t_0}\int_{t_0}^{t_1}\left(\frac{t^2}{2!\tau^2}\right)^2 dt = (V_0+I_S R_S)^2\frac{t_{\mathrm{VCO}}^4}{20\tau^4} \tag{10}$$

$$P_{3,\mathrm{rms}}{}^2 = \frac{(V_0+I_S R_S)^2}{t_1-t_0}\int_{t_0}^{t_1}\left(-\frac{t^3}{3!\tau^3}\right)^2 dt = (V_0+I_S R_S)^2\frac{t_{\mathrm{VCO}}^6}{252\tau^6}. \tag{11}$$

Using a linear canceller only removes $P_{1,\mathrm{rms}}$ which still leaves a residual fractional spur power due to higher-order contributions. Thus, a higher-order canceling scheme removing second or even third order of quantization error is necessary for further lowering the fractional spur. The power calculated here represents the variation at the sampler output. It can be divided by the feedback gain $2\beta_{\mathrm{Sp}}^2$ as shown in (5) to calculate the total fractional spur power at PLL output. However, the total power will be spread over all harmonics of fractional spurs, making it difficult to precisely predict the exact spur level at each harmonic tone. Fig. 8 shows the calculated total fractional spur power at the PLL output versus current source output resistance when: 1) no cancellation applied at sampler output; 2) only canceling the linear term ($P_{1,\mathrm{rms}}$); and 3) canceling both the linear and the second-order term ($P_{1,\mathrm{rms}}$ and $P_{2,\mathrm{rms}}$). When no cancellation is applied, sampler output has a large residual frac-N induced voltage error. PLL is equivalently working under phase modulation (PM) mode which leads to total unfiltered spur power higher than 0 dBc. Cancelling the first- and the second-order terms progressively reduces the fractional spur power.

Another key factor for reducing the fractional spur is to improve sampler linearity or increase the output impedance (R_s) of the current source. As shown in Fig. 8, even with a linear canceller, fractional spur quickly decreases with higher output impedance. To improve the output impedance with a fixed output current, one way is to use cascode structure with the penalty of increased voltage headroom that causes the reduced sampled voltage range. Note that even though only the total fractional spur is calculated here, the fundamental fractional spur dominates the spur power for a frac-N accumulator output without DSM. As the technology node keeps scaling down to a deep sub-micrometer region, it will be more challenging to implement a linear current source. However, due to its static operation nature, the current sources do not need to be scaled down if its linearity is a priority for the design. In addition, the proposed higher-order cancellation scheme can be applied to maintain a low spur level. To further relax the requirement on sampler's linearity, a multi-phase VCO or a DTC at the divider output can be adopted to reduce the required linear range to sub-VCO cycle (lower equivalent t_{vco}).

III. Circuit Implementation

A. System Architecture

The block diagram of the proposed fractional PLL architecture is shown in Fig. 9. The VCO output is first divided down to 1 GHz with a high speed customized 8/9 pre-scaler. A digital counter synthesized with standard cells further divides the VCO frequency down to the reference clock frequency. Continuous programmability of the division ratio is supported by the loop divider. A finite state machine (FSM) is implemented in the digital counter to provide loop control signals (φ_1, φ_2, …) for clocking the RSPD and the CP. The loop divider is controlled by a fractional accumulator without any DSM to achieve fractional operation. The instantaneous divider quantization error (Qe) and its squared value (Qe^2) are also calculated with the fractional accumulator. The calculated linear and quadratic quantization errors are encoded by the CDAC control logic circuit to toggle the capacitors in the CDAC and hence generate cancellation voltage at the RSPD output. The divider output (φ_1) is resynchronized to the VCO clock to clean up accumulated jitter due to digital circuits. In the RSPD, the gated VCO clock (φ_1) is used to sample the buffered reference edge. A reference buffer is implemented to reshape the external sinusoidal reference clock into a rail-to-rail CMOS clock signal. The sampled edge slope can be adjusted by the current setting of the RSPD.

At the RSPD output, the sampling capacitor is reused as the capacitor array for an 8-bit CDAC with the bottom plate connected to either ground or different reference voltages. Two reference voltages are implemented to enable the first- or second-order fractional spur cancellers. The sampled

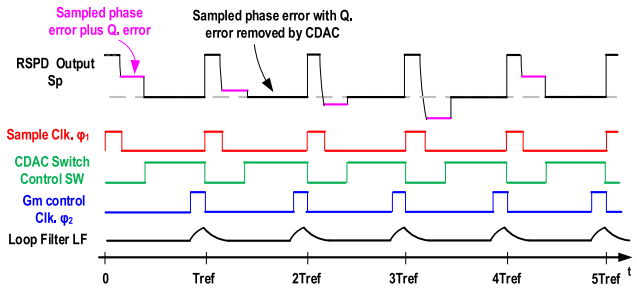


Fig. 10. Timing diagram of the fractional-N operation with the proposed CDAC spur cancellation technique.

voltage (S_p) captures the desired phase error information as well as the frac-N quantization error as illustrated in the timing diagram of Fig. 10. The CDAC is utilized to generate a reversed quantization error in the voltage domain during the hold phase. This cancels the deterministic quantization error due to the fractional-N operation in each sampled voltage while leaving the phase error from the loop feedback untouched. The CDAC bottom plate switch is toggled shortly after the RSPD goes into hold phase. After voltages on S_p settle down, the CP g_m connected to the sampling capacitor is triggered by another clock φ_2 that converts the sampled voltage into charges injected into the LF. The g_m cell in the CP is similar to that used in [4]. The LF consists of a small integrated capacitor (50 pF) and a large external capacitor. LF is connected to VCO tuning voltage and controls VCO output frequency. An *LC*-tank based class-C VCO is implemented for improved phase noise and power efficiency. Although spur cancellation using a current DAC at the analog PFD output has been reported in classic analog frac-N PLLs [15], this design proposed a CDAC spur cancellation scheme by combining the CDAC capacitors with the sampling capacitor for a reference sampling PLL (RSPLL) with adjustable sampler gain for simultaneous phase noise and spur reductions. All the CDAC charging and discharging activities operate at the reference frequency and consume low power. The CDAC gain calibration for spur reduction needs to be performed only for the lock state.

B. Reference Buffer and Sampling PD

As shown in Fig. 11, to reshape the external sinusoidal reference clock into a square wave rail-to-rail clock, a low-power CMOS buffer with pulsed reset is implemented [17]. To minimize the additional jitter due to reshaping, the first inverter stage needs to provide large g_m in order to minimize the conduction time of transistor channel thermal noise. This requires a large W/L ratio and consumes a large current during the transition edge. In this regard, only the NMOS is directly connected to the external reference clock. The PMOS is connected to a pulse generated by the delayed reference clock edge. In this way, the PMOS is turned off when M0 conducts current, minimizing the short circuit current. M0 is given a large W/L ratio to minimize the falling edge jitter of the reshaped reference clock. This circuit only guarantees low noise for the falling edge and the rising edge can be noisy. This is acceptable in our case as only the falling edge of the

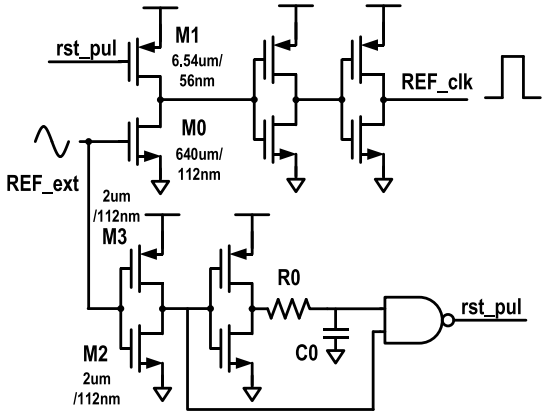


Fig. 11. Schematic of the reference clock buffer.

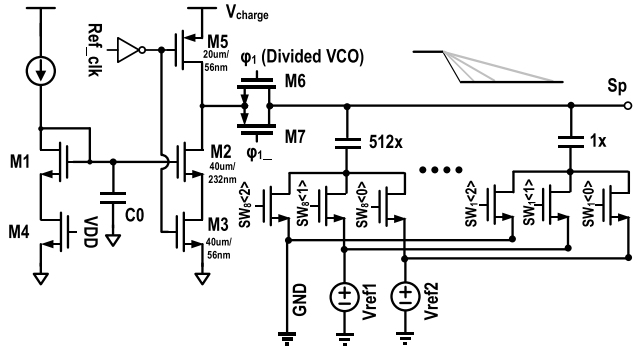


Fig. 12. Schematic of the RSPD consisting of the current source-based sampler and CDAC quantization error canceller.

reference clock is critical to the sampling operation in the RSPD.

In order to maintain a constant discharging current during sampling, a current mirror consisting of M1–M2 is implemented in the sampler as shown in Fig. 12. The inverter consisting of M3 and M5 is triggered by the reference clock to discharge and recharge the sampling capacitor. The current source M2 is inserted in series with M3 to keep a constant discharging current. During discharging, M3/M4/M6/M7 are working in the triode region as switches and contributing only thermal noise related to $R_{\rm ON}$ resistances. M1 and M2 are working in the saturation region, contributing channel thermal noise. Decoupling capacitor C0 is connected to the M2's gate to suppress the noise from M1 and M4. The sampling switches M6 and M7 form a transmission gate and is controlled by the gated VCO clock φ_1. The sampling cap consists of an 8-bit CDAC array with an LSB cap size of 1 fF; thus, the total sampling capacitance is 255 fF. The 1-fF LSB capacitor size was chosen in order to achieve high sampler gain with fast settling time. To minimize the parasitic influence and alleviate the parasitic noise coupling, the CDAC is isolated from other circuit components with sufficient spacing and guard-rings. Considering additional parasitic capacitance on net S_p, the total sampling capacitance C_s is about 500 fF. The bottom plate of each sampling capacitor is connected to either ground, $V_{\rm ref1}$ or $V_{\rm ref2}$. The highest reference voltage applied is less than 400 mV; thus, only NMOS is used for the switch. Two external tunable reference voltages are connected

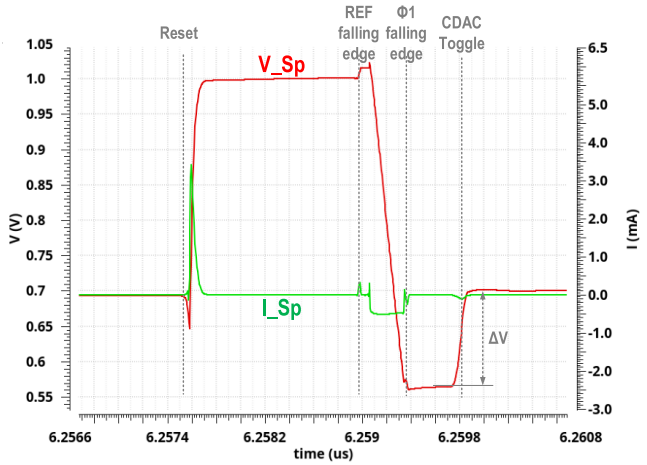


Fig. 13. Simulated sampler output (Sp) transient voltage and current in one reference cycle after lock-in. ΔV represents the cancellation voltage created by CDAC.

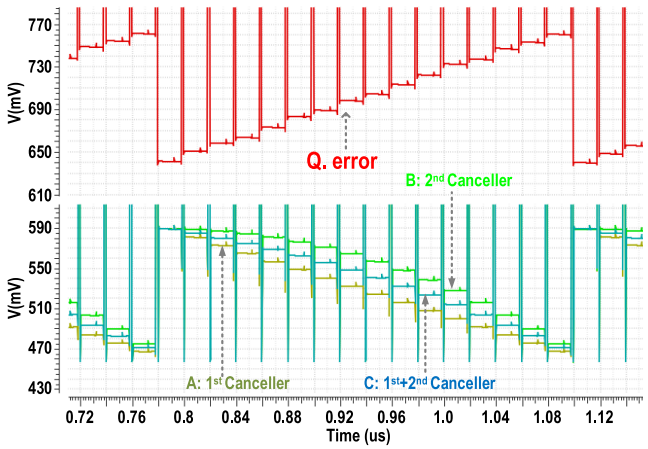


Fig. 14. Simulated sampler output voltage (Sp) over multiple reference cycles with PLL configured in open-loop mode. Top curve shows the quantization noise in frac-N mode. Bottom curves show the canceller waveforms generated by CDAC with (A) $V_{\text{ref1}} = V_{\text{ref2}} = 0.25$ V (first-order canceller only), (B) $V_{\text{ref1}} = 0$, $V_{\text{ref2}} = 0.25$ V (second-order canceller only), and (C) $V_{\text{ref1}} = 0.125$ V, $V_{\text{ref2}} = 0/25$ V (first- and second-order cancellers).

to CDAC for the second-order cancellation. Through tuning the external reference current I_{bias}, the discharging current and the sampled edge slope can be programmed.

Referring to Fig. 10, in each reference cycle (20 ns), 3 ns is assigned to the sampling phase (φ_1), 14 ns is assigned to the CDAC settling, and the CP (φ_2) is enabled only during the remaining 3 ns. In this way, ample time is given for CDAC voltage settling. As shown in the transient simulation result in Fig. 13, the sampling capacitor is reset at the rising edge of the reference clock. Discharging is triggered by the falling edge of the reference clock. A small amount of kickback charges and delay is present before discharging which is signal independent. The sampling capacitor is disconnected from the discharging current at the falling edge of the divided VCO clock φ_1. The discharging current I_s is set to 700 μA, giving a sampled edge slope of 1.4 GV/s, or a falling time of about 700 ps. Shortly afterward, the CDAC is toggled and the quantization error (ΔV) is removed from the sampled voltage Sp.

C. CDAC Based Quantization Error Canceller

The operational mechanism of the proposed CDAC canceller can be illustrated with a transient simulation where the PLL is configured in an open-loop mode. In this setup, the VCO tuning voltage is disconnected from LF and is set to a fixed voltage. For instance, the VCO frequency is fixed at 9 GHz + 3.125 MHz (fractionality = 1/16). The reference clock and the divided VCO clock φ_1 are manually aligned. Thus, the sampler output Sp reflects the fractional quantization error without the cancellation and the error from the PLL loop feedback as shown in the top part of Fig. 14, which follows a periodic ramp pattern over reference clock cycles. The turning point of each ramp corresponds to the division ratio toggling from N to $N+1$. As discussed in Section II-B, the peak to peak residual voltage at the RSPD output or the magnitude of ramp waveform equals to $t_{\text{vco}} \cdot S_{\text{samp}}$.

In the second simulation, the PLL is still configured in the open-loop mode but the VCO frequency is fixed at 9 GHz. Thus, the sampler output Sp shall be constant as only integer mode is used. After enabling the CDAC canceller, the generated anti-ramp canceller is superimposed on the originally sampled voltage. It can be observed as shown in the bottom part of Fig. 12. Referring to the CDAC control setup listed in Table I, Qe and Qe^2 represent calculated quantization error and its squared value, respectively. These two are calculated in real-time with the integrated frac-N accumulator. Both Qe and Qe^2 are truncated to 8-bit and the integrated CDAC logic converts them to the switch controls for each bit in CDAC following Table I. Through toggling CDAC switch between the sampling phase and hold phase, a canceller voltage ΔV is generated on Sp as shown in Fig. 13. In Fig. 14, curve (A), both V_{ref1} and V_{ref2} are set to 250 mV. The canceller ΔV on Sp depends only on Qe$< k >$; thus, it is a linear canceller. To achieve optimal cancellation with the first-order canceller, the magnitudes of the frac-N quantization error induced ramp waveform and the CDAC generated cancellation waveform need to match, namely

$$V_{\text{ref1}} = t_{\text{vco}} \cdot S_{\text{samp}}. \tag{12}$$

However, as previously discussed in Section II-C, the quantization error is not strictly linear due to the sampler's nonlinear behavior; thus, high order canceller is also implemented. In Fig. 14, curve (B), V_{ref1} and $V_{\text{ref2}}$are set to 0 and

TABLE I
CDAC SWITCHING CONTROL SETUP

Qe <k>	Qe^2 <k>	Switch Ctl. (SW_k)		ΔV on Sp	Note
		Sample Phase	Hold Phase		
0	0	GND	GND	0	No change
0	1	V_{ref2}	V_{ref1}	V_{ref2} -V_{ref1}	Second order canceller gain
1	0	V_{ref1}	GND	V_{ref1}	First order canceller gain
1	1	V_{ref2}	GND	V_{ref2}	Total canceller gain

250 mV, respectively. Again, referring to Table I, ΔV now depends only on Qe^2. Thus, the canceller waveform follows a quadratic pattern. In curve (C), V_{ref1} and $V_{\text{ref2}}$are set to 125 and 250 mV, respectively. Thus, ΔV depends on both Qe and Qe^2, enabling both first- and second-order canceller generates a waveform which stands between curves A and B. In this case, the canceller waveform can be expressed as follows:

$$V_{k,\text{canceller}} = V_{\text{ref1}} \cdot \frac{k}{K} + (V_{\text{ref2}} - V_{\text{ref1}}) \cdot \left(\frac{k}{K}\right)^2 \tag{13}$$

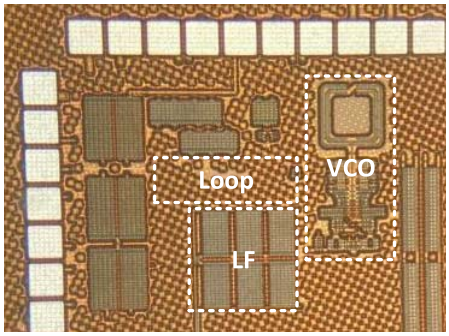
where K is fractionality and $k = 1 - K$. To achieve optimal cancellation, the coefficients of first- and second-order terms need to match that in the quantization error as derived in (7); thus, the following condition needs to be satisfied:

$$V_{\text{ref2}} = \left(1 + \frac{1}{2\tau}\right) V_{\text{ref1}}. \tag{14}$$

This scheme is equivalent to adding a pre-distortion on the CDAC to compensate the second-order non-linearity of the RSPD. The proposed CDAC canceller can be extended to even higher orders of cancellation in a similar fashion. Thus, through setting reference voltages according to (12) and (14), the proposed CDAC scheme can cancel the first- and second-order quantization errors at the sampler output. However, the estimated device parameters are not accurate and may vary over process-voltage-temperature (PVT) variations. In this work, for a proof-of-concept, the reference voltages are set externally. Thus, a manual reference voltage tuning can be applied if needed to fine-tune the optimal cancellation effect. This gain tuning mechanism can be implemented on-chip. For instance, an on-chip delta-sigma DAC can be implemented to generate the reference voltages. Using a background least mean square (LMS) based digital calibration scheme similar to [13], the reference voltage can be adaptively tuned for optimal fractional spur cancellation over PVT variations. In order to facilitate the prototype testing, we pulled the references V_{ref1} and V_{ref2} off-chip in this design. However, reference voltage sources can also be integrated on-chip. Since the reference is coupled to sampler output, its noise contribution will be suppressed by the sampler's high gain. Provided that the reference buffer and CDAC can settle within the assigned time window (14 ns), key performance metrics including noise and spur can still be maintained when integrated reference voltages are adopted.

IV. Measurement Results

The RSPLL prototype was fabricated in a 45-nm partially depleted silicon-on-insulator (PDSOI) CMOS technology with a core active area of 0.1-mm^2 excluding the integrated LF. The die photograph and power breakdown are shown in Fig. 15. The power consumption of the RSPLL is 4.5 mW in total under a 1-V power supply. Owing to the switched capacitor behavior in the reference buffer and the RSPD, the two modules consume a very low power of 0.2 mW each. With external reference voltages for the CDAC, the proposed quantization error canceller consumes zero dc power and ignorable dynamic power. With the high gain provided by the RSPD, the CP only burns 0.7 mA to keep its noise below PLL's in-band noise



Module	Power (mW)
Ref. Buffer	0.2
RSPD	0.2
CP	0.7
VCO& buffer	2.5
Divider	0.7
Digital	0.2
Total	4.5

Fig. 15. Die photograph and power breakdown of the prototype RSPLL chip.

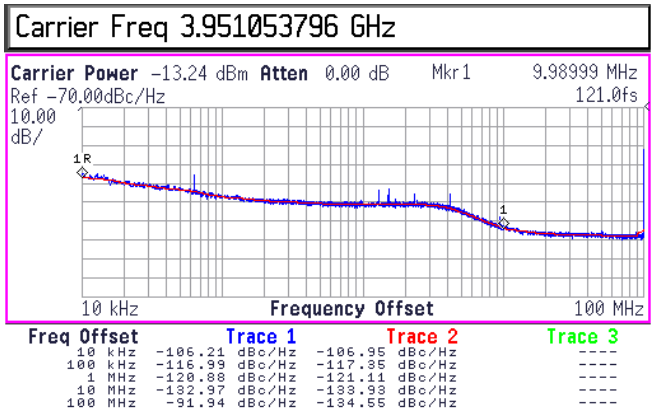


Fig. 16. Measured PLL output (divided by 2) phase noise in integer mode at 3.95 GHz (VCO running at 7.9 GHz).

floor. The majority of the power is consumed by the 9-GHz class-C VCO. An external sinusoidal low noise clock running at 100 MHz is used as the reference clock. The PLL can cover an output frequency range of 7.7–9.1 GHz.

The measured PLL output phase noise in integer mode is shown in Fig. 16. The PLL is running at 7.9 GHz and its output is divided down by 2 for the measurement. An in-band noise floor of -120 dBc/Hz has been achieved at 3.95-GHz divided output. The jitters integrated from 10 kHz to 10 MHz and from 10 kHz to 50 MHz (half of the reference frequency) are 108 and 121 fs, respectively. The measured reference spur at 100-MHz offset is -40 dBc. The high reference spur level is due to the on-chip as well as PCB coupling as a similar spur level is observed even when the CP is turned off. The reference spur level can be improved with better chip layout and PCB designs. As discussed in Section II-B, the sampler noise is a function of t_{res}. This relationship can be observed through increasing V_{charge} while keeping $V_{\text{ref\_}n}$ constant. With a larger difference $V_{\text{charge}} - V_{\text{ref\_}n}$, it takes longer for the sampler to discharge the sampling capacitor, leading to a prolonged t_{res}. In this setup, $V_{\text{ref\_}n}$ is set to 0.6 V (lower $V_{\text{ref\_}n}$ squeezes voltage headroom in g_m cell) and V_{charge} is toggled between 0.6 and 1.1 V. The measured integer mode phase noise is shown in Fig. 15. To demonstrate the noise effect due to the sampler, the discharge current is intentionally decreased to 300 μA and, thus, increases the noise contribution from the sampler as shown in Fig. 17. The in-band noise floor at 100-kHz offset degrades by about 4 dB when varying t_{res}

TABLE II
MEASURED PLL PERFORMANCES AND COMPARISONS

	ISSCC 2016 [11] X. Gao	JSSC 2016 [7] A. Narayanan	JSSC 2019 [5] W. Wu	JSSC 2017[18] C. Yao	JSSC 2018 [19] A. Elkholy	This Work
Technology	28nm	65nm	28nm	28nm	65nm	45nm
PLL structure	Digital Sub-sampling	Analog Sub-sampling	Analog Sub-sampling	Digital TDC	Digital ILCM	Analog Ref-sampling
Spur cancellation scheme	DTC	PI	DTC	Digital Cancellation	DTC	CDAC
Freq. (GHz)	2.7~4.33	4.34~4.94	6.33	2.69	6.75-8.25	7.7~9.1
Ref. (MHz)	40	40	52x2	26	115	100
In-band frac. spur (dBc)	-54	-59	-64	-78	-42	-55
Min. frac. freq. step size (kHz)	100	15	10	1	30	25
Integrated jitter (fs)	159 (10kHz-40MHz)	133 (10kHz-10MHz)	75 (10kHz-10MHz)	137 (10kHz-10MHz)	170 (10kHz-30MHz)	Integer mode: 121 Frac-N mode: 135 (10kHz-50MHz).
Power (mW)	8.2	6.2	18.9	13.4	3.25	4.5
FoM* (dB)	-246.8	-249.5	-249.7	-246	-250	Integer mode: -251.8 Frac-N mode: -250.8

*$\text{FoM} = 10\log_{10}(\sigma_{\text{jitter}}{}^2 * \text{Power}/1\text{mW})$

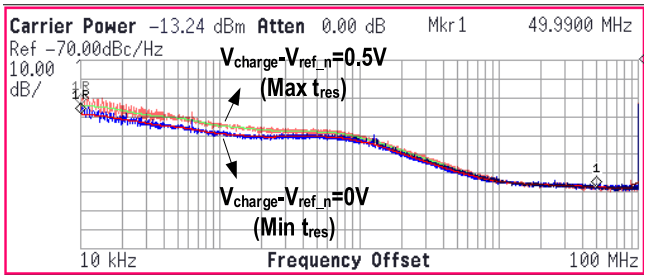


Fig. 17. Measured PLL output (divided by 2) phase noise with different sampler discharge time t_{res}.

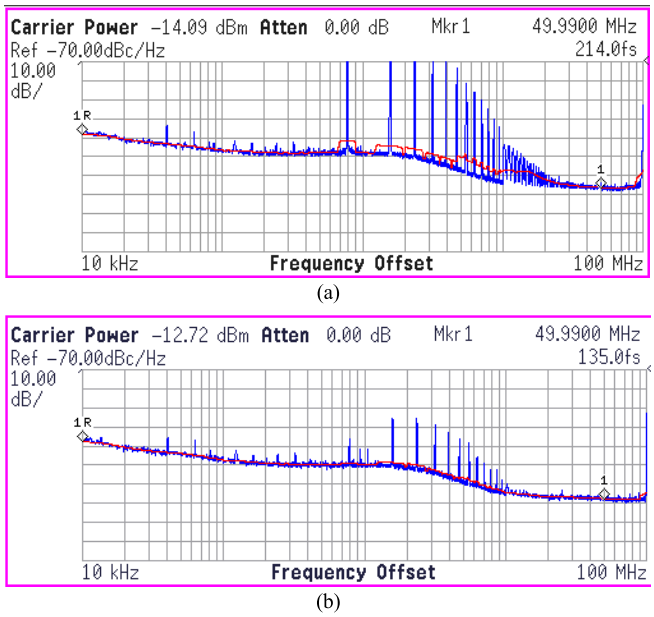


Fig. 18. Measured PLL output (divided by 2) phase noise in fractional mode (a) without quantization error cancellation and (b) with quantization error cancellation.

from its minimum value to its maximum value. The loop still managed to remain locked even though V_{charge} and $V_{\text{ref\_}n}$ are the same, which corresponds to the minimum t_{res}. This is due to the charge kickback which boosts the initial voltage on the sampling capacitor a little higher at the beginning of the discharge phase. Fig. 18 shows the measured PLL phase noise in fractional mode with a fractionality of 1/128, which corresponds to a fundamental fractional spur at a frequency offset of 781 kHz. In frac-N mode, when the CDAC canceller is turned off, the jitter integrated from 10 kHz to 50 MHz is measured at 214 fs. After enabling the canceller, the noise floor remains the same while all the fractional spurs are significantly reduced, resulting in an improved integrated jitter at 135 fs. This demonstrated the effectiveness of the proposed CDAC cancellation technique in reducing the deterministic jitter caused by frac-N quantization errors.

Furthermore, the improvement in fractional spur is also shown in the measured near-integer fractional spectrum in Fig. 19. In this case, the fractionality is set to 1/2048 with the fundamental fractional spur around 50 kHz. Without cancellation, the worst fractional spur reaches as high as −20 dBc. With the first-order canceller enabled, the worst spur is improved to −41 dBc. Further enabling both the first- and the second-order cancellers, the fundamental fractional spur is further reduced to −67 dBc, leading to a total 47-dB spur reduction using the proposed CADC spur canceller. However, the second-order harmonics at 100 kHz is only reduced to −55 dBc. The second harmonic is slightly higher due to the CDAC's differential nonlinearity (DNL). Errors were observed when the CDAC switches from one MSB capacitor to all the LSB capacitors (100…00 to 011…11), or when the cancellation voltage from CDAC crosses the middle point of its total range. Based on the measured results, the CDAC DNL at this point is estimated to be around 0.4 LSB, or 0.4 fF. Thus, the higher harmonic spurs are due to capacitor mismatch induced DNL in CDAC, and they can be improved with better CDAC matching. Without cancellation, the worst fractional spur level is around −20 dBc over fractional frequency. After enabling the proposed canceller, the measured fundamental fractional spur is suppressed below −60 dBc.

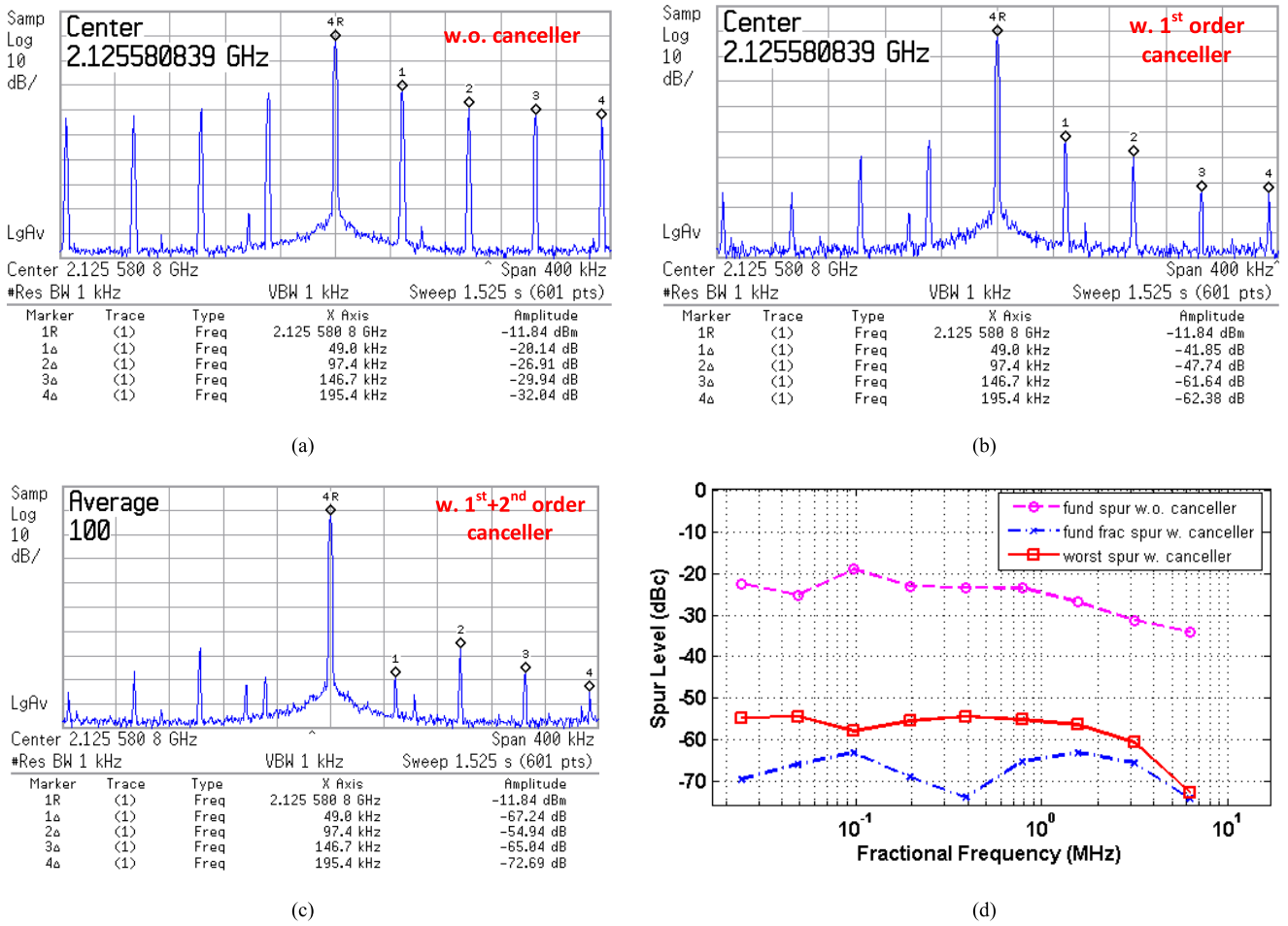


Fig. 19. Measured PLL output (divided by 4) fractional spur level. (a) Without canceller, (b) with first-order canceller only, (c) with first- and second-order canceller, and (d) over fractional frequency.

However, the remaining worst fractional spur is consistently the second-order fractional spur. It remains relatively flat around −55 dBc over the fractional frequency and only starts to decrease beyond PLL loop bandwidth due to the loop filtering effect. Although higher-order frac-*N* spurs sometimes increased slightly when the canceller is on and they are easier to be filtered. In all cases, the highest spur is always dominated by the fundamental or the second-order spurs.

The performance summary and the comparison to other state-of-the-art sampling or digital PLLs are given in Table II. Our proposed design has achieved low integrated jitter with low power even though the VCO is running at a higher frequency. This is due to the switching capacitor behavior of the critical loop components such as the reference buffer, the linearized sampler, and the CDAC spur canceller, which consume low power. This 7.7–9.1-GHz RSPLL design has achieved a power efficiency figure of merit (FoM) of −250.8 dB.

V. Conclusion

A fractional-*N* RSPLL has been presented in this article. The proposed reference sampler with a CDAC-based fractional spur canceller consumes low power owing to the switch capacitor circuit topology. Moreover, the proposed PLL achieves low noise for fractional synthesis as it avoids using noisy and power-hungry DTCs on reference path or phase interpolation at VCO output. The gain of the reference sampler can be adaptively tuned to achieve a wide detection range for acquisition and high gain for low phase noise after lock. Unlike the SSPLL, an additional frequency locking loop is not needed for the proposed RSPLL, leading to a simplified loop topology with improved stability. The current source based sampler provides a linear, high-gain, and low power conversion from the phase error in the time-domain to a voltage error. Although the current source in the sampler contributes extra noise compared to a pure SSPD, its overall noise is still lower than a conventional PFD/CP based PLL with less noise contributing sources and shorter residual turn-on time. In addition, the noise from the CDAC canceller can be further suppressed below the PLL noise floor by setting the RSPD in high gain mode through programming the slope of the sampled edge. The proposed high order quantization error canceller relaxes the requirement on the sampler's linearity. Applying multiple reference voltages to the CDAC, higher-order quantization error can be further reduced. Fabricated in a 45-nm PDSOI technology, the RSPLL prototype has achieved an integrated jitter from 10 kHz to 50 MHz of 121 fs in

integer mode and 135 fs in fractional mode, respectively. With a power consumption of 4.5 mW, the RSPLL achieves an FoM of −250.8 dB. With the proposed CDAC spur cancellation, the worst fractional spur, located well within the loop bandwidth, is measured to be lower than −55 dBc.

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