# An mm-Wave Synthesizer With Robust Locking Reference-Sampling PLL and Wide-Range Injection-Locked VCO

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***Abstract*— In this article, a two-stage millimeter (mm)-wave frequency synthesizer with low in-band noise and robust locking reference-sampling techniques is presented. Using a two-stage scheme allows separately dealing with the low phase noise (PN) frequency synthesis in the first stage and the mm-wave frequency multiplication in the second stage, achieving the best overall power efficiency. In the first stage, a voltage domain reference-sampling phase detector (RSPD)-locked loop (RSPLL) is adopted to achieve both low PN and robust locking without additional frequency locking loop. A reference reshaping buffer is implemented to improve the phase detector gain and in-band PN. The reference rising/falling time is programmable to achieve optimal RSPLL performance even under external disturbances. The second stage employs an injection-locked voltage-controlled oscillator (ILVCO) for 4× frequency multiplication. A low-power digital frequency tracking loop (FTL) detecting actual frequency errors is implemented in order to achieve wide operation range for the ILVCO while using a high $Q$ tank with low power. The prototype synthesizer was fabricated in a 45-nm partially depleted silicon on insulator (PDSOI) CMOS technology. The first stage 9-GHz RSPLL achieves 144-fs integrated jitter with 7.2-mW power consumption, achieving a figure of merit (FoM) of −248 dB and the overall mm-wave synthesizer achieves 251-fs integrated jitter with 20.6-mW power consumption at 35.84 GHz, achieving an FoM of −238.9 dB.**

***Index Terms*— Frequency tracking loop (FTL), injection-locked frequency divider (ILFD), injection-locked oscillator, millimeter (mm)-wave frequency generation, reference-sampling phase detector (RSPD)-locked loop (RSPLL), sub-sampling PLL (SSPLL).**

## I. Introduction

THE next-generation 5G network requires mobile transceivers to operate over millimeter (mm)-wave bands of around 28–40 GHz. Compared to its predecessor at the sub-6-GHz band, this giant leap in operating frequency presents new challenges to radio frequency integrated circuit (RFIC) designs. The wider channel bandwidth at the mm-wave frequency range is utilized to provide higher data rate. To support a more complicated modulation scheme including 256-quadratic-amplitude modulation (QAM), the local oscillator (LO) in the RF transceiver chain is required to achieve an integrated phase noise (PN) of less than −30 dBc at 5G mm-wave bands [1]. This puts more stringent restrictions on the amount of jitter produced by the integrated frequency synthesizer. Another major challenge is to minimize the increased power consumption of the mm-wave synthesizer. The fast deteriorating quality factor of the integrated *LC* tank at mm-wave frequency costs high power consumption in order to generate a low-noise carrier in mm-wave oscillator. In this regard, we have adopted a two-stage approach [1]–[3] where the second stage consists of a noisy but power efficient injection-locked voltage-controlled oscillator (ILVCO). The overall system PN will be dominated by the first stage where the PN of the mm-wave VCO is largely suppressed due to injection locking. Thus, a low-noise mm-wave synthesizer can be achieved with lower total power consumption. In addition, the adopted partially depleted silicon on insulator (PDSOI) CMOS process provides faster transistor with an $f_t$ reaching 290 GHz and inductors with high quality factor due to high substrate resistivity. All these are very beneficial for our mm-wave synthesizer performance.

To reduce the PN of the first stage phase-locked loop (PLL), a type-I reference sampling PLL (RSPLL) structure has been adopted. Compared to sub-sampling PLL (SSPLL) [4], the RSPLL [5] can extend the phase detector (PD) capture range from half VCO cycle to half reference cycle, thus not requiring additional frequency loops where the integration of two loops can be nontrivial [6]. Although RSPLL has adopted a similar voltage domain PD as in SSPLL where the phase error is first transferred to the voltage error, directly using reference edge as the sampled slope causes a much lower PD gain in RSPLL. This requires a much larger sampling capacitor in RSPLL to suppress the sampling noise compared to SSPLL.

In our proposed RSPLL design, a reference clock buffer has been introduced to reshape the external reference clock into a square wave with programmable rising/falling time. This helps boost the PD gain and isolate it from the external reference waveform. Since the large gain of voltage domain PD is maintained only within the rising/falling edge of the sampled waveform, its linear range is proportional to the edge transition time. Large external disturbance coupled into the loop might cause the gated VCO edge to fall out of the sampled edge, which degrades the actual PD gain and the

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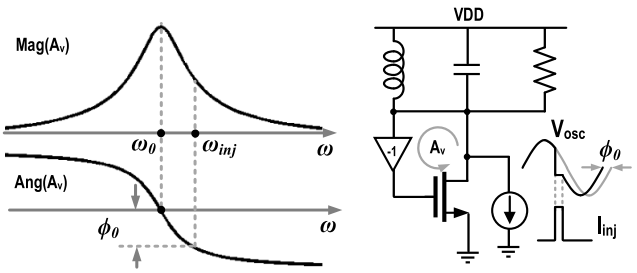


Fig. 1. Conceptual illustration of *LC* tank-based ILVCO.

in-band noise floor. Using the proposed reference reshaping buffer, the slope of the sampled edge becomes programmable: a faster slope leads to higher PD gain and lower PLL in-band noise floor, whereas a slower slope leads to wider linear range and thus improved robustness against external disturbances.

ILVCO gains attractions as the second stage for the mm-wave frequency synthesizer due to its low additional noise and power [7]–[9]. Depending on the ratio of input and output frequency, injection locking technique can be categorized into three cases. The working principle of the fundamental-frequency injection locking is illustrated in Fig. 1 [10]. Assuming the tank has a free-running frequency $\omega_0$, an external signal $\omega_{\rm INJ}$ is injected into the tank, introducing a phase shift $\varphi_0$; ILVCO will sustain oscillation at $\omega_{\rm INJ}$ if the total loop phase shift including $\varphi_0$ equals $2\pi$ to meet the Barkhausen oscillation criteria. The frequency locking range increases with higher relative injection strength, higher $\omega_0$, and lower tank $Q$. For sub-harmonic injection locking cases such as ILVCO, the *LC* tank will be locked to an oscillation frequency of $\omega' = n \cdot \omega_{\rm inj}$. On the other hand, in a super-harmonic injection locking case such as frequency dividers, $\omega_0$ is close to the $n$th sub-harmonic of the injection signal, and thus the locked tank oscillation frequency will be $\omega' = (1/n) \cdot \omega_{\rm inj}$.

For the ILVCO design, there are significant challenges to achieve a wide locking range with low power consumption, since a higher tank $Q$ leads to better PN and lower power but narrower frequency locking range. In [7], it was proposed to improve the locking range through a higher order tank. However, this leads to substantial penalty in lowered tank $Q$ and a much higher power consumption reaching 148 mW. Alternatively, methods to calibrate VCO free-running frequency were proposed to mitigate this problem: the envelope detection frequency tracking loop (FTL) proposed in [8] and [9] provides a power efficient method to detect frequency error. However, it is prone to miss the frequency drift after the initial lock. Another approach [9] based on the average phase detection FTL relies on a specific phase delay of quadrature VCOs (QVCO) and may limit the lock range since it only detects the phase deviation.

For our proposed ILVCO, a low-power auxiliary FTL which detects the actual frequency error to tune the VCO free-running frequency for robust injection locking is implemented. This method provides an effective approach that does not require any special VCO structure and can be applied in various mm-wave frequency multipliers. To minimize the power overhead of the FTL loop, an inductor-less injection-locked frequency divider (ILFD) is implemented as the first stage

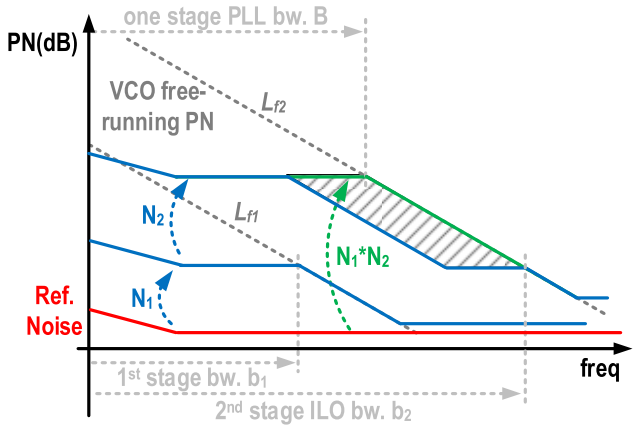


Fig. 2. Illustration of a two-stage PLL architecture PN upscaling compared to a single-stage PLL design.

mm-wave prescaler. Through tuning the delay of each stage in the ILFD, multiple integer division ratios can be achieved to extend the output frequency range when used as output divider, or allow frequency multiplication with other ratios when used in FTL loop for ILVCO.

This article is an extension of [11], with a more detailed theoretical analysis and circuit design. It is organized as follows. Section II discusses the advantage of multistage mm-wave synthesizers, along with theoretical analysis and simulation results for our presented RSPLL; Section III presents the implementation details of the entire synthesizer system; the measurement results and conclusions are given in Sections IV and V, respectively.

## II. Design of a Low-Noise mm-Wave PLL

### A. Multistage mm-Wave PLL Architecture

Since it is difficult to directly generate an mm-wave carrier and achieve overall good PLL figure of merit (FoM) with a single-stage frequency synthesizer, most recent publications rely on the two-stage architecture [2]. The FoM disadvantage from the single-stage architecture is mainly due to the dramatically degraded integrated VCO performance at the mm-wave frequency. As illustrated in Fig. 2, $L_{f1}$ and $L_{f2}$ represent the VCO free-running PN at an intermediate frequency $f_1$ and the mm-wave frequency $f_2$. In a two-stage PLL structure, the reference clock is first upscaled with a factor of $N_1$ to reach $f_1$. To achieve minimal integrated PN, the bandwidth of first-stage PLL is usually set at the intersection of $L_{f1}$ ($b_1$ as labeled in Fig. 2), and the elevated reference PN which is $N_1$ times larger due to frequency upscaling. At the second stage, this intermediate frequency is further multiplied by $N_2$ through a frequency multiplier such as ILVCO and reaches $f_2$. Due to the relatively high $f_1$, the close-in PN at mm-wave output is largely determined by the first-stage PLL. At far-out frequency $b_2$, which represents the bandwidth of the second-stage ILVCO, the output PN follows $L_{f2}$. Eventually the mm-wave VCO PN in the two-stage architecture can be suppressed with a narrow loop bandwidth $b_1$. Whereas for a single-stage design, the reference noise is directly multiplied by $N_1 \cdot N_2$ times, achieving similar in-band noise floor but requiring a higher loop bandwidth $B$ to suppress VCO PN. The shaded

part represents the additional noise from a single-stage structure for side-by-side comparison.

As a quantitative example, using a reference clock running at 80 MHz with a PN floor of −155 dBc/Hz beyond 100-kHz offset frequency, its contribution to PLL in-band noise floor after frequency multiplication by 100× ($N_1$) and another 4× ($N_2$), corresponding to first-stage PLL ($f_1$ = 8 GHz) and second-stage ILVCO ($f_2$ = 32 GHz), would be −115 and −103 dBc/Hz, respectively. This is under the assumption that second-stage ILVCO injects negligible in-band PN, which is verified in our measurement as shown later. In a two-stage configuration, using our measured first-stage VCO and second-stage mm-wave VCO data where $L_{f1}$ is −110 dBc/Hz (at 1-MHz offset) and $L_{f2}$ is −86 dBc/Hz (at 1-MHz offset) at 8.4 and 35.7 GHz, respectively, the loop bandwidth of first-stage PLL is set to 2 MHz ($b_1$) where in-band noise floor intersects $L_{f1}$ for optimal integrated PLL jitter. The second-stage ILVCO bandwidth is set wide enough where the mm-wave VCO reaches noise floor to avoid injecting additional noise, assuming 20 MHz ($b_2$) in this case. On the other hand, using a one-stage PLL architecture for a direct frequency multiplication of 400×, its loop bandwidth needs to reach about 5 MHz ($B$). Integrating the PN profile of both configurations from 1-kHz to 100-MHz offset frequency gives an integrated jitter of 157 and 107 fs at 32 GHz, or about 46% additional jitter from a two-stage to a one-stage architecture.

Despite the PN advantage of the multistage PLL architecture, having an additional stage in the frequency generation chain unavoidably leads to more hardware and higher power consumption. Fortunately, such penalties can be partially alleviated in the following ways.

1) Since the mm-wave PN profile largely depends on the first-stage output, the noise requirement on the mm-wave VCO (which usually dominates the power consumption of the entire synthesizer) can be relaxed, resulting in less power consumption.
2) Through reducing the second-stage frequency upscaling ratio $N_2$, a simpler loop architecture can be utilized in the second-stage PLL, reducing or even eliminating power hungry loop components like mm-wave dividers. Furthermore, by operating at this intermediate frequency rather than directly at the mm-wave frequency range, it is more power efficient to implement jitter reduction techniques in the first-stage PLL.

### *B. Reference Sampling With Programmable Sampled Slope*

Ever since the introduction of SSPLL several years ago [4], voltage sampling technique has attracted increasing attention in state-of-the-art PLL designs [11]–[15]. As shown in Fig. 3, the sub-sampling phase detector (SSPD) in an SSPLL measures the phase errors by sampling the fast VCO edge using the reference clock, achieving a large PD gain: $V_{\mathrm{PD}} = A_{\mathrm{VCO}}\varphi_e$, or the PD output voltage equals to VCO amplitude times phase error. This large gain consequently suppresses noise from the subsequent stages including charge pump (CP) and loop filter (LF). However, the detected voltage

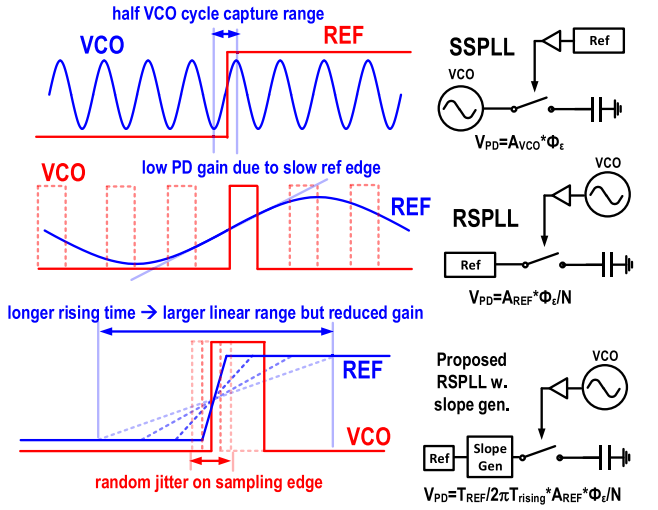


Fig. 3. Conceptual diagram for different sampling schemes in the voltage-mode PLL.

from the SSPD is valid only within the half-VCO cycle. On the other hand, RSPLL, proposed in [6], uses a gated VCO edge to sample the sinusoidal reference clock. The detected voltage remains roughly proportional to the phase error over half of the reference period. Thus, in terms of locking robustness, RSPLL is much more improved compared to SSPLL. However, the PD gain in this case is lower: $V_{\mathrm{PD}} = A_{\mathrm{ref}}\varphi_e/N$, or roughly $N$ times smaller than that of an SSPLL. Thus, it requires a large sampling capacitor to achieve similar in-band noise suppression. In sum, SSPLL and RSPLL represent two extreme phase lock topologies: SSPLL achieves large PD gain with small detection range, whereas RSPLL achieves large detection range with reduced PD gain.

In our proposed design, a programmable slope generator is added to the reference clock before it is sampled by the VCO edge for the tradeoff between the PD gain and the PD detection range. A similar slope buffer has been proposed for SSPLL [16], wherein a larger PD detection range can be achieved with RSPLL as it is not limited by the VCO period. As shown in Fig. 3, the transition time of the rising or falling edge after reshaping the reference waveform is largely determined by the $RC$ time constant at reference buffer output. Define a loop feedback gain $\beta$ as follows:

$$\beta = \frac{V_{\mathrm{PD}}}{\varphi_e} = T_{\mathrm{ref}}/(2\pi\cdot\tau_{\mathrm{rising}})\cdot A_{\mathrm{ref}}\cdot\frac{1}{N} \tag{1}$$

where $T_{\mathrm{ref}}$ and $\tau_{\mathrm{rising}}$ denote the reference period and the rising time of the reshaped reference waveform, respectively. Considering $(T_{\mathrm{ref}}/2\pi\cdot\tau_{\mathrm{rising}}) \gg 1$, the achieved PD gain is much greater than that in the original RSPLL without slope shaping. In addition, the locking range is kept as one reference cycle, leading to robust locking. Note that even though the polarity of the reference-sampling phase detector (RSPD) output is correct in one reference period (12.5 ns), the linear range is still limited to the sampled edge rising time (∼hundreds of ps). Outside the sampled edge, the RSPD saturates and causes much smaller PD gain, elevating the PLL in-band noise floor level. In normal integer operation, the phase error after lock should be ideally close to zero.

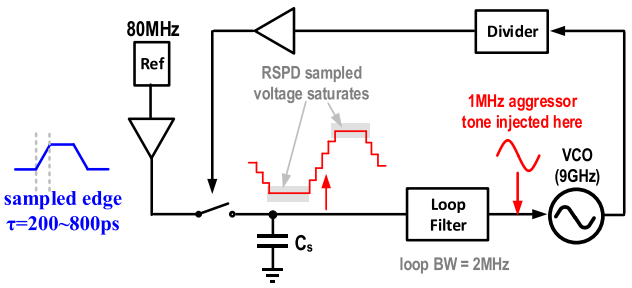


Fig. 4. Behavioral RSPLL model for external disturbance simulation. Large aggressor causes RSPD saturation, reduces PD gain, and degrades in-band PN in saturation regions.

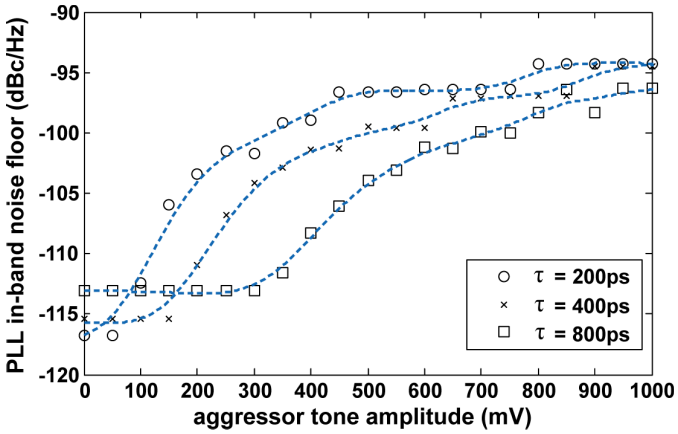


Fig. 5. Simulated in-band PN degradation with increasing aggressor tone amplitude. Simulation results are shown as symbols along with three interpolated curves for different rising times ($\tau$) of the reshaped reference edge.

However, under scenarios with large external disturbances, large jitter might occur on the sampling edge, forcing RSPD into saturation.

To understand this phenomenon, a simplified model for our proposed RSPLL design has been built as shown in Fig. 4. The reference clock is reshaped into a square wave with a limited rising/falling time of $\tau$. After being sampled by the divided VCO clock, the charge is stored in the sampling capacitor $C_s$. The external aggressor can be coupled into the system through several mechanisms such as layout parasitics or power line coupling, etc. In this model, aggressor tones at 1 MHz with various amplitudes are injected at LF output due to large layout area of the integrated LF. Large aggressor amplitude causes RSPD to saturate and clip to the rail on the RPSD output. In these shaded regions, the PD gain is largely suppressed, degrading both loop gain and in-band noise level. In Fig. 5, three levels of sampled edge time $\tau$ have been simulated over increasingly larger aggressor tone amplitudes. Larger $\tau$ causes RSPLL in-band noise to rise at higher aggressor power level, implying that it is less sensitive to external disturbances. On the other hand, a smaller $\tau$ results in better in-band noise floor in the absence of disturbances due to stronger suppression for RSPD and LF noise.

Since a type-I PLL structure is adopted for this design, the major in-band noise contributor is the slope generator and RSPD, which are implemented with a current mode logic

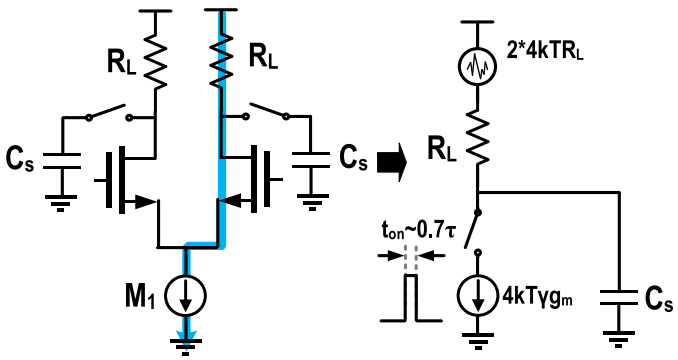


Fig. 6. Simplified noise model of the reference sampling PD.

(CML) buffer loaded by a sampling capacitor $C_s$ as shown in the simplified diagram (Fig. 6). Assuming that the differential input reference clock is switching relatively fast, such that the differential pair mostly stays in switching mode in which all the current flows through one branch, this allows us to make a simplification of dividing the left and right branches for noise analysis. Assuming the turn on time of current source connected to sampling capacitor is $t_{\text{on}} = 0.7\tau$ to reach 50% of output swing (here $\tau$ represents the time constant $R_L C_S$), the noise at RSPD output can be shown as follows [17]:

$$v_{n,\text{RSPD}}^2 = \frac{kT}{C_s}\left(2 + \gamma\, g_m R_L\left(1 - e^{-2t_{\text{on}}/\tau}\right)\right) \tag{2}$$

where $\gamma$ and $g_m$ represent the channel thermal noise coefficient and transconductance of current source $M_1$. The two terms in (2) represent contribution from load resistor $R_L$ and current source $M_1$, respectively. Dividing (2) over the loop feedback gain $\beta^2$ as in (1) gives the in-band noise contribution from RSPD, which is approximately proportional to $\tau_{\text{rising}}^2$. Thus, RSPD noise rises with slower reshaped reference edge.

## III. Implementation of a Two-Stage mm-Wave Frequency Synthesizer

The block diagram of our proposed two-stage cascaded PLL architecture is shown in Fig. 7. The first stage is a type-I low-noise RSPLL with reference reshape buffer, while the second stage is an mm-wave ILVCO. The injection ratio between the first-stage RSPLL and the second-stage ILVCO is chosen to be 4×. Therefore, the first-stage target frequency is 8–9 GHz and the second-stage target frequency is 32–36 GHz. This frequency plan relaxes the operating frequency of the first-stage RSPLL to allow using inductor with a higher quality factor and lower power to achieve better FoM. The ILVCO injection lock range is simulated to be around ±(40–60) MHz for a 4× injection ratio. As a comparison, a 3× injection ratio might obtain ±(100–150)-MHz lock range, but it would require the first-stage RSPLL to be running at 12 GHz with higher power.

### A. First-Stage Low Noise Type-I RSPLL

In the first-stage RSPLL, the external 80-MHz reference clock is multiplied to 9 GHz as an intermediate clock for the second stage. To avoid the noise and power due to CP, a type-I PLL structure was adopted. However, having one less pole

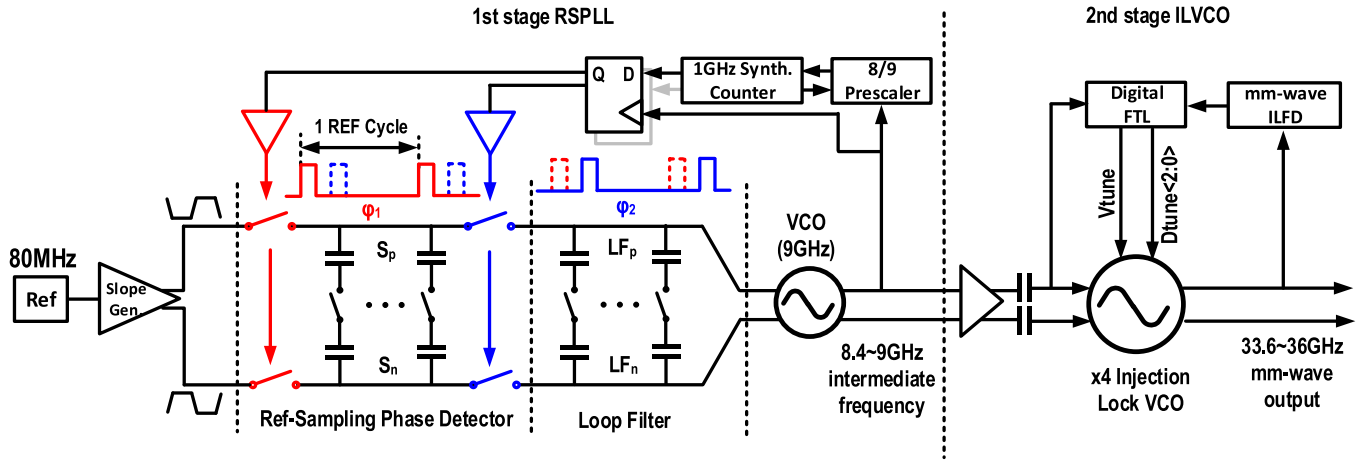


Fig. 7. Block diagram of the proposed two-stage mm-wave frequency synthesizer.

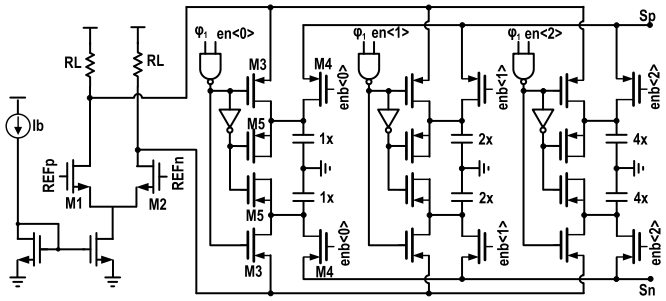


Fig. 8. Schematic of the reference sampling PD.

compared to a common type-II design leads to less in-band VCO PN suppression and a nonzero residual phase error. For PLL in-band noise, loop gain provides 20-dB/dec suppression which cancels the 20-dB/dec rising slope of VCO free-running PN, leading to a flat in-band VCO noise floor. However, for very small frequency offset, VCO PN enters the $1/f^3$ region and flicker noise starts to arise at PLL output. Thus, a larger loop bandwidth is required in a type-I PLL to suppress the VCO PN.

The loop divider adopted a pulse-swallow structure, consisting of an 8/9 prescaler running at VCO frequency (~9 GHz) followed by a synthesized digital counter running at the divided VCO frequency (~1 GHz). Division ratio at prescaler is controlled by a digital counter dynamically to provide continuous division ratio programmability. Due to the large loop division ratio (100–112), the pulse-swallow divider can continuously support all the ratios over the required range [18]. The synthesized digital counter generates two output pulses, $\varphi_1$ and $\varphi_2$, to control the RSPD and LF, each spanning over roughly 2 ns and separated by 1 ns to avoid charge kickback as shown in Fig. 7. The $\varphi_1$ and $\varphi_2$ are resampled by the VCO edge at divider output to clean up accumulated jitter going through digital logic.

The external reference clock is reshaped with a differential pair and a programmable binary capacitor array as shown in Fig. 8. The reshaped slope is then determined by the time constant of load resistance $R_L$ and total capacitance $C_s$ from the capacitor array. The sampling switch $M_3$ is driven by $\varphi_1$ gated with capacitor enable signal en $\langle 2{:}0 \rangle$. Another half-sized switch $M_5$ is driven by an inverted clock to neutralize the charge injected from turning off $M_3$. Switch $M_4$ driven by inverted capacitor enable signal enb$\langle 2{:}0 \rangle$ connects the activated capacitors to the output $S_p/S_n$. To implement a type-I PLL, a switched cap circuit is utilized as the LF. A capacitor array is built for programmable loop bandwidth. When $\varphi_2$ becomes high, charges stored in the sampling capacitor Cs are redistributed onto the capacitor array in LF. The equivalent filter *RC* time constant implemented with the switched capacitor circuit can be shown as follows:

$$R_{\mathrm{LF}}C_{\mathrm{LF}} = \left(R_{\mathrm{sw}} + \frac{1}{f_{\mathrm{ref}}C_s}\right) \cdot C_{\mathrm{LF}} \sim \frac{1}{f_{\mathrm{ref}}}\frac{C_{\mathrm{LF}}}{C_s} \tag{3}$$

where $R_{\mathrm{sw}}$ is the switch ON resistance and $C_s$ is the sampling capacitance in RSPD. Assuming $R_{\mathrm{sw}}$ is small, the LF pole frequency only depends on reference clock and capacitor ratio between the LF and the RSPD.

The RSPLL loop bandwidth for optimal total PN is around 2 MHz, where the in-band noise floor and VCO noise intersect. The RSPD load resistor is 400 Ω with a swing of 600 mV at CML buffer output. The sampling capacitor $C_s$ can be programmed from 0.25 to 1.75 pF, leading to a reference edge rising time of about 500 ps–2 ns. The LF capacitor $C_{\mathrm{LF}}$ is fixed at eight times the sampling capacitance, creating the second pole at 10 MHz. The RSPLL output PN is simulated for the fastest and slowest sampled edge as shown in Fig. 9. For the slow edge case, the loop bandwidth is about 500 kHz. The small loop bandwidth makes the in-band noise floor dominated by VCO PN due to the weak out-band noise suppression in type-I PLL. For the fast edge case, the loop bandwidth has reached 2 MHz, making the reference clock and VCO contribute equally to the PLL in-band noise floor, reaching an improved in-band noise floor of about −110 dBc/Hz at 8.4 GHz. Although the RSPD has contributed negligible PN, its noise contribution has increased by about 6 dB from the fast sampled edge to the slow sampled edge case, which agrees with our previous noise analysis for RSPD.

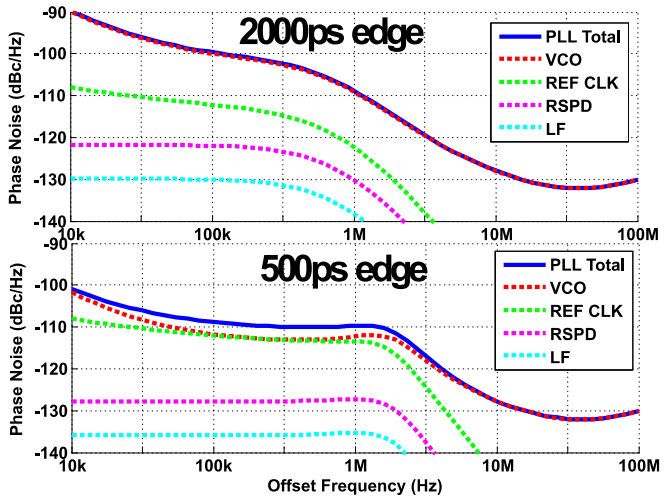


Fig. 9. Simulated RSPLL PN at 8.4 GHz with slow and fast reference sampled edges.

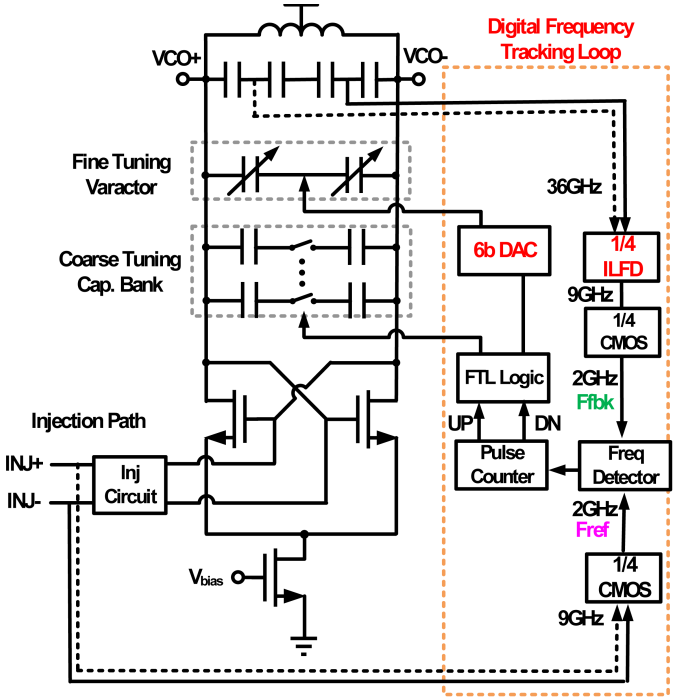


Fig. 10. Schematic of the second-stage injection-locked frequency multiplier with a digital FTL.

### *B. Second-Stage mm-Wave Injection-Locked Frequency Multiplier*

The proposed ILFM topology is shown in Fig. 10. It consists of an ILVCO and a low-power and low-area digital FTL with smooth lock transition. An inductor-less mm-wave ILFD has been adopted in FTL to save power and area. The FTL loop directly detects the actual frequency deviations rather than the envelope or the phase deviations as presented in [8] and [9], which relies on specific VCO or QVCO phase delay characteristics. The proposed digital FTL also resolves the dilemma between extending the injection locking for robust locking over larger frequency range, and increasing the tank $Q$ to achieve lower PN and power.

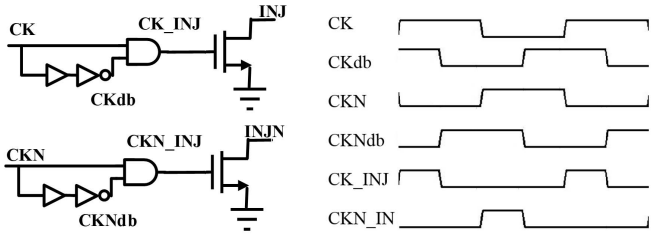


Fig. 11. Injection circuit and timing diagram.

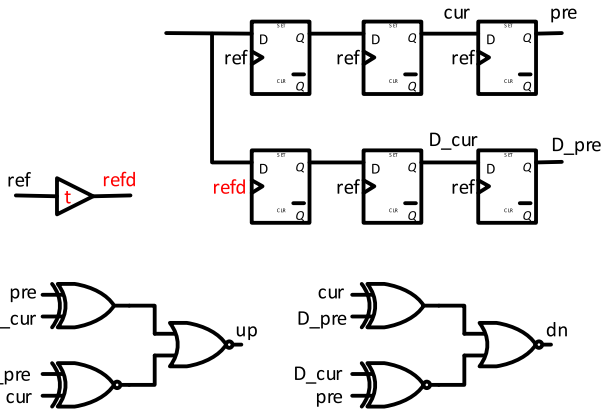


Fig. 12. Schematic of the simplified asynchronous sampling FD.

*1) ILFM Circuit Structure:* To meet the frequency tuning range requirement, the ILVCO is implemented with four binary weighted high-$Q$ metal–insulator–metal (MIM) capacitor banks for coarse frequency tuning (total 16 coarse frequency bands), and one varactor bank for fine frequency tuning. The tank inductor and the parasitic inductance on the interconnection between the inductor and the rest of the VCO have all been extracted in electromagnetic (EM) simulation to better predict the VCO frequency and $Q$-factor. A high $Q$ inductor ($Q \sim 19$ at 40 GHz) was achieved for the PDSOI process. The simulated PN was $-83.7$ to $-91.7$ dBc/Hz at 1-MHz offset for the highest VCO frequency around 36 GHz. The injection circuit (details shown in Fig. 11) is a pair of pulse generators with $\sim$20% duty cycle. It injects currents into the *LC* tank on both rising and falling input clock edges, reducing the effective internal frequency injection ratio to $2\times$.

The circuit in the dashed box in Fig. 10 is our proposed digital FTL. It consists of a wideband power-efficient ILFD, two divide-by-4 CMOS dividers, a low-power CMOS asynchronous sampling frequency detector (FD) [19], a pulse counter, the FTL logic, and a 6-bit voltage DAC. As illustrated in Fig. 12, the FD uses 6 D-flip-flops (DFF) to asynchronously sample the clocks and uses six gates to generate the up- and down-indication signals. Other low-power-type FDs may also be used. The DAC step size was designed for 20 MHz (1/4 of minimum injection lock range) to ensure lock. The frequency locking flow will be illustrated in Section IV. The voltage DAC was employed to provide smooth transition between the frequency lock with FTL and the phase lock through ILVCO. After the VCO is injection-locked, the FTL output codes settle to a constant value where both the MIM capacitor bank (coarse

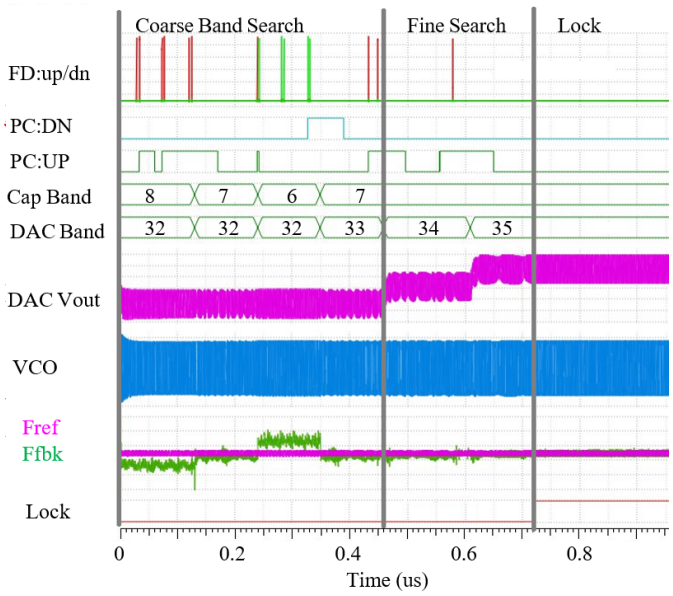


Fig. 13. Injection locking waveforms (from top to bottom): the FD outputs (the red line is "up" and the green line is "dn" pulses); the pulse counter output DN (down); pulse counter output UP (up); the coarse tuning capacitor bank code; the fine-tuning DAC code; the DAC output voltage; the VCO tank oscillation waveform; reference clock frequency (pink) and feedback clock frequency (green); and the lock signal.

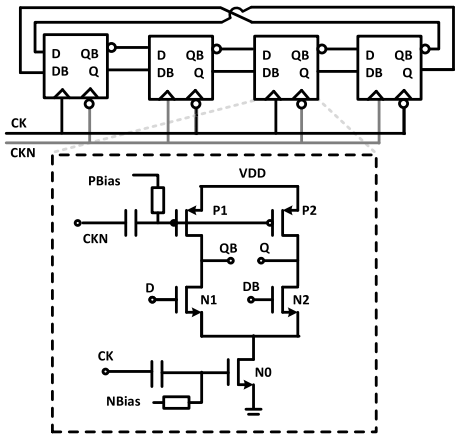


Fig. 14. Simplified schematic of a four-stage ILFD and CML latch in each stage.

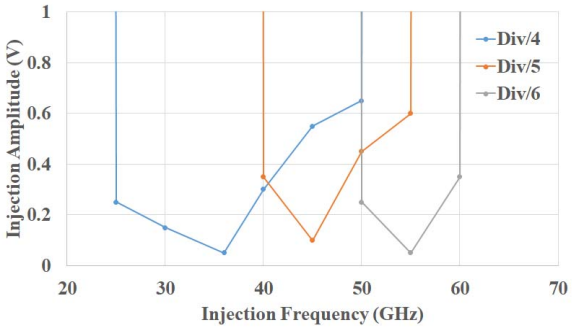


Fig. 15. Simulated ILFD injection strength required when biased for self-oscillation frequency ~9 GHz.

tuning) and the varactor biasing voltage (fine-tuning) remain constant, avoiding additional PN due to the FTL. On the other hand, when the ILVCO loses lock, the FTL FD can instantly detect the frequency deviation and enable FTL logic, bringing ILVCO back to injection lock state.

*2) Frequency Locking Flow:* The FTL logic performs the VCO frequency search in a two-step process, which can be illustrated with the simulated locking transient waveforms as shown in Fig. 13. First, it searches for the optimum coarse tuning capacitor bank that provides the closest free-running frequency to the locked frequency. At the end of each time window, the FTL logic examines the pulse counter outputs which acts as a digital low pass filter and determines the search direction of the coarse tuning code. The search starts from the middle coarse bank 8 in order to save time, then changes one band at a time while the DAC band is fixed in the middle band 32. The coarse band ramping process stops at band 6, where the pulse counter asserts the DN signal indicating that the VCO frequency is above the target. It then goes back one step to band 7 to start the second search for the DAC codes. In a similar fashion, the optimum DAC code controlling fine-tuning varactor biasing is stabilized at code 35 where the VCO's free-running frequency was in the injection locking range. Then the VCO will quickly injection lock to the $N$th harmonic of the reference frequency generated by the first-stage RSPLL (i.e., an injection ratio of 1:$N$). Later, the FTL can be turned off to save power, or stay alive to track any instantaneous disturbances or voltage and temperature variations in normal operation. Note that all initial settings and the time window are made programmable for test flexibility. In the presence of beat frequency, the instant and average frequency will be higher than $\omega_{\text{inj}}$ for low-side injection case (or lower than $\omega_{\text{inj}}$ for high-side injection case) [10]. In Fig. 13, the last few fine band search steps actually illustrate this scenario, where the VCO frequency is not far away from the lock range (as indicated by $F_{\text{ref}}$ and $F_{\text{fbk}}$ lines). The phase-frequency detector (PFD) is able to detect the frequency difference, enable the FTL make correct up/down decision, and drive the VCO frequency to fall into final injection lock.

*3) mm-Wave ILFD:* To reduce the power consumption of our proposed digital FTL, an inductor-less mm-wave ILFD comprising of four-stage cascaded CML latches [20] has been utilized as the first stage mm-wave prescaler, as shown in Fig. 14. When a sufficiently strong external clock is injected, the ILFD would be pulled away from its self-oscillation frequency and lock to one of the sub-harmonics of the injected clock. For steady-state injection-locked operation, both loop magnitude and phase need to satisfy Barkhausen criteria (loop gain $\geq$ 1 and loop phase $= 2k\pi$). For the divide-by-$N$ operation, the total loop delay equals to $N$ times the injected clock period. Simulation showed our ILFD's self-oscillation frequency without external excitations to be 7.3–15.4 GHz for the optimized bias condition range, which is mainly determined by the delay in each stage. Fig. 15 shows the simulated injection strength required when biased for self-oscillation frequency ~9GHz as an example.

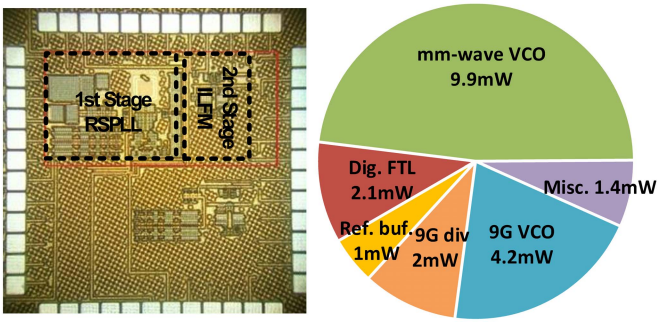


Fig. 16. Die photograph and the power breakdown of the proposed synthesizer.

Each latch stage comprises of a differential input pair $N_1/N_2$, a tail current source $N_0$ and a pair of PMOS loads $P_1/P_2$. The injected differential clock signal CK is ac-coupled to the gate of $N_0$ and CKN is ac-coupled to the gates of $P_1/P_2$. The gate dc biasing level can be externally tuned: the gain of each stage can be adjusted through gate biasing on $N_0$ which tunes the biasing current of the differential pair, whereas the phase delay can be adjusted by the load PMOS ($P_1/P_2$) gate biasing voltage for tuning the load time constant. The two-point injection scheme (at $N_0$ and $P_1/P_2$) helps extend the locking range. Through tuning these two biasing points, the ILFD in our design is able to provide a division ratio of 4/5/6 as long as the phase and magnitude conditions are satisfied at the divided frequencies. The dynamic latch may be viewed as a conventional static CML latch without the regenerative cross-pair to minimize output capacitance and thus achieves high-speed operation. Note that since CK/CKN of the ILFD drive odd/even latch stage's CK/CKN alternatively, the total loading of CK/CKN is actually symmetric so as not to degrade the preceding VCO's PN performance.

## IV. Measurement Results

### A. mm-Wave Synthesizer Measurement Results

The proposed mm-wave synthesizer MMIC was implemented in a 45-nm PDSOI CMOS process with the die photograph and power breakdown chart shown in Fig. 16. The core active area is only 0.41 $mm^2$. The entire two-stage mm-wave synthesizer system consumes 20.6 mW from 1.1/0.9-V power supply. The first and second stages consume 7.2 and 13.4 mW, respectively. The measured PN of the first-stage RSPLL with slow and fast reference sampled edge is shown in Fig. 17. The PLL output frequency was divided by 4 before output for the measurement. Due to the type-I architecture, VCO flicker noise rises along with the loop flicker noise at close-in offset frequency. Using faster sampled edge of 500 ps, a higher loop bandwidth can be achieved, improving VCO noise suppression and in-band noise floor compared to the 2000-ps sampled edge case. The PN was measured as −123 dBc/Hz at 1-MHz offset frequency, achieving an integrated jitter of 144 fs (10 kHz–10 MHz) at 2.24-GHz test frequency, which corresponds to the PLL output at 8.96 GHz. The first-stage RSPLL achieves an FoM of −248 dB as shown in the performance Table I.

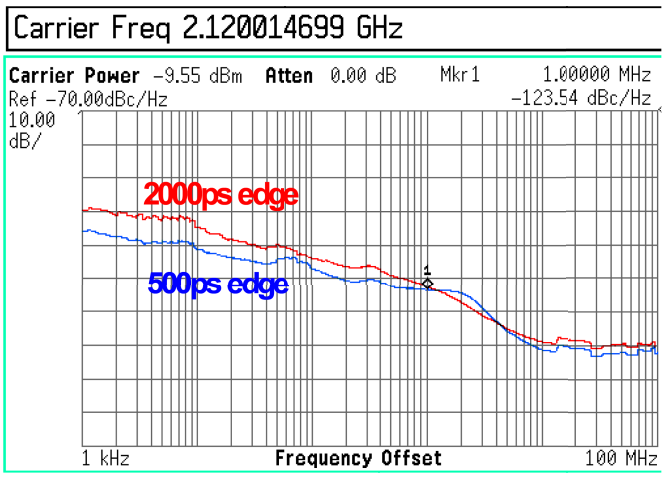


Fig. 17. Measured RSPLL PN with slow/fast sampled edge rising time; faster edge helps suppressing VCO in-band noise contribution, leading to lower in-band noise floor. VCO output frequency has been divided by 4 for measurement.

TABLE I
MEASURED RSPLL PERFORMANCES AND COMPARISONS

| | Gao [4] JSSC-10 | Dongyi[6] JSSC-17 | Jahnavi[5] ISSCC-18 | This work |
|---|---|---|---|---|
| Architecture | SSPLL type-II | SSPLL type-II | RSPLL type-I | RSPLL type-I |
| Tech | 180nm | 130nm | 65nm | 45nm |
| Ref. (MHz) | 55.25 | 50 | 50 | 80 |
| Output Freq. (GHz) | 2.21 | 2.3-2.4 | 2.05-2.55 | 8.4-9 |
| Int. RMS Jitter (fs) | 150 (10k-40M) | 158 (10k-10M) | 110 (10k-10M) | 144 (10k-10M) |
| Ref. Spur (dBc) | -46 | -72 | -63 | -48 |
| Power (mW) | 7.6 | 21 | 3.7 | 7.2 |
| FoMp* (dB) | -247 | -243 | -253 | -248 |

FOMp= 20log10(jitter)+10log10(Pdc[mw])

Similarly, the second-stage mm-wave output was divided 16 times to around 2.24 GHz for the measurement. The first-stage RSPLL output showed about 2-dB in-band PN degradation due to loading and parasitic coupling from the second-stage ILVCO. As shown in Fig. 18, the close-in PN profile closely follows that of the first-stage RSPLL (for frequency offset < 1 MHz), and becomes gradually worse than the RSPLL but still better than the mm-wave VCO between 1 and 30 MHz, then reaches flat noise floor beyond 30 MHz. The injection lock range of the second-stage ILFM is about 10–30 MHz. A higher injection lock bandwidth could further lower the mm-wave synthesizer PN closer to the RSPLL PN in the 1–30-MHz offset range. Note that the measured PN of the ILVCO includes the inductor-less divider noise. Thus, the PN of the implemented ILVCO should be better than what was measured using the divider. The second-stage ILFM achieved an integrated jitter (10 kHz–10 MHz) of 251 fs at 35.84 GHz, reaching a jitter FoMj of −238.9 dB as shown in the performance Table II. The back-calculated PN at 35.84 GHz is −94.9 dBc/Hz at 1-MHz offset. Through adopting the proposed FTL structure for mm-wave ILVCO, our design has achieved good PN, low power, and good overall PLL FoM performance.

TABLE II
MEASURED mm-WAVE SYNTHESIZER PERFORMANCES

| | Alvin JSSC-14 [7] | Tee. JSSC-16 [21] | Ying RFIC-17 [22] | Waleed TMTT-17 [2] | Nagarajan TMTT-17 [23] | Zunsong ISSCC-19 [24] | Ahmed ISSCC-17 [25] | This work |
|---|---|---|---|---|---|---|---|---|
| Topology | PLL + 3step ILFM | SSPLL + 1step ILFM | Single stage PLL | PLL + SSPLL | Single stage PLL | Single stage iSSPD PLL | Single stage ADPLL | RSPLL + 1step ILFM |
| Tech. | 65nm | 65nm | 250nm | 65nm | 0.18um SiGe | 65nm | 65nm | 45nm |
| Ref. (MHz) | 100 | 36/40 | 50 | 230 | 120 | 103 | 100 | 80 |
| Output Freq. (GHz) | 20.6-48.2 | 55.6-65.2 | 37.2-40 | 26-32 | 29.5-33.4 | 25.4-29.5 | 50.2-64.8 | 33.6-36 |
| PN @ 1MHz (dBc/Hz) | -108.1 | -91 | -100.7 | -116.2 | -97 | -112.8 | -92.7 | -94.9 |
| Int. RMS Jitter (fs) | - | 290 [10k-40M] | 104 [100k-1M] | 63.6 [1k-10M] | 189 [10k-10M] | 71 [1k-100M] | 223 [1k-40M] | 251 [10k-10M] |
| Ref. Spur (dBc) | - | -73 | <-73 | -63.2 | -40 | -63 | <-59.1 | -60 |
| Power (mW) | 148.3 | 32 | 323-380 | 26.9 | 63 | 10.2 | 46 | 20.6 |
| FoMp (dB) | -179 | -171.6 | -170.5 | -191.3 | -168.5 | -191.1 | -170 | -172.8 |
| FoMj (dB) | - | -236 | -234 | -249.6 | -237 | -252.9 | -236.5 | -238.9 |

FOMp=PN-20log10(f/f0)+10log10(Pdc[mw])
FOMj=20log(Jitter[s])+10log10(Pdc[mw])

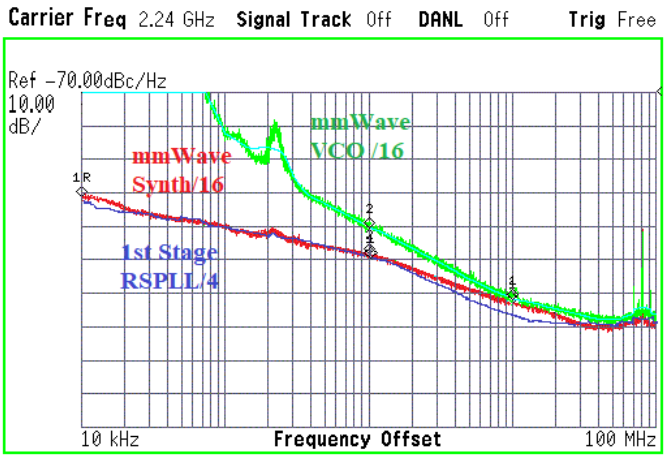


Fig. 18. Measured PN of the divided mm-wave output overlaid with the first-stage output and the second-stage mm-wave VCO free-running PN.

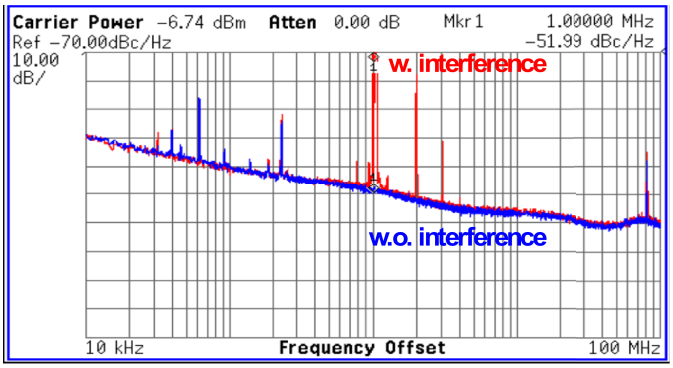


Fig. 19. Measured spectrum of the mm-wave output in the presence of external disturbances; the large spur at 1 MHz corresponds to the injected disturbance (output frequency was divided by 16 for the measurement).

To test the locking robustness of the RSPLL, a 1-MHz 50-mV peak-to-peak sinusoidal disturbance was injected onto the power supply of the first-stage VCO. The mm-wave synthesizer output spectrum in the presence of this disturbance is shown in Fig. 19. Due to its large programmable capture range, the RSPLL remains locked without using an auxiliary frequency lock loop, which is usually required for conventional SSPLLs. The in-band noise floor remains the same as in the case without disturbance. Only a spur corresponding to the injected signal was present in the measured spectrum as an evidence of the disturbance.

### *B. ILFD Measurement Results*

In Section IV-A, the ILFD is embedded in the FTL loop to lower the input frequency of the PFD and thus lower power consumption. It may also be used outside the loop in the output path to divide down the clock frequency to provide multiple frequency bands by utilizing its multiple

TABLE III
MEASURED PN AT THE INJECTION-LOCKED DIVIDER OUTPUTS

| Input Frequency (GHz) | Division ratio | Output Frequency (GHz) | Phase noise @1MHz offset (dBc/Hz) |
|---|---|---|---|
| 43.81 | 4 | 10.95 | -101.2 |
| | 5 | 8.76 | -103.3 |
| | 6 | 7.30 | -104.7 |

division ratios. To test the programmable division ratio of our implemented ILFD, the divider is configured in an open-loop testing setup in which the mm-wave VCO free-running output clock is directly divided by the ILFD in a separate prototype chip. The ILFD was followed by a CMOS divide-by-4 circuit and a differential CML output buffer for testing purposes. This second mm-wave VCO was measured to operate at 41.2–43.9 GHz. Fig. 20(a)–(c) shows the measured output spectra at the buffered output with division ratios of 4/5/6 when the VCO was tuned to 43.8 GHz. Fig. 20(d) shows the division ratio versus PMOS gate voltage $|Vgs|$. It was noticed that the range of the bias voltage of the load PMOS was about 20 mV. Table III summarizes the

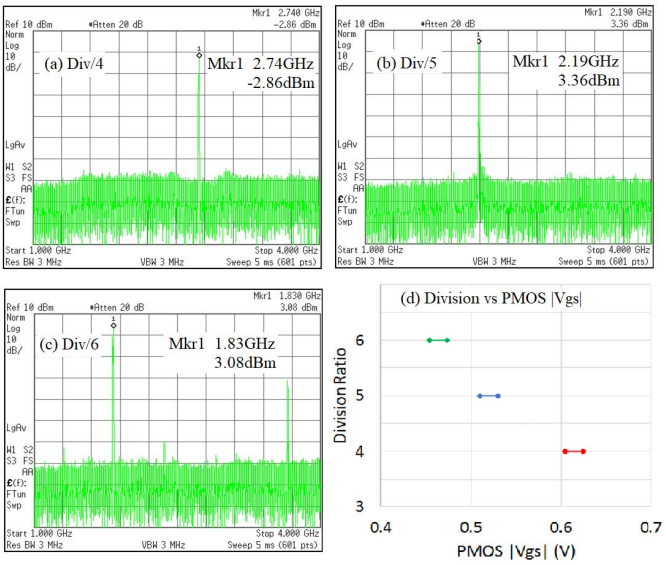


Fig. 20. Measured ILFD (with additional Div/4 buffer) output spectra with different divide ratios at input frequency 43.8 GHz. (a) Divided-by-4. (b) Divided-by-5. (c) Divided-by-6. (d) Division ratios versus PMOS $|V_{gs}|$.

TABLE IV
MEASURED RESULTS AND COMPARISON TO OTHER mm-WAVE DIVIDERS

| Ref | Ghilioni [26] JSSC-13 | Mostajeran [27] MTTS-17 | Hara [28] ASSCC-09 | This work |
|---|---|---|---|---|
| Fin Max | 70GHz | 61GHz | 11.4GHz | 43.8GHz |
| Division ratios | 4 | 2 | 2/3/4/6 | 4/5/6 |
| Supply Voltage | 1.0V | 1.6V | 1.2V | 0.94V |
| Power | 4.8mW | 10.4mW | 1.3mW | 2.4mW |
| Area [$\mu m^2$] | 3000 | 1600 | - | 1368 |
| Technology | 32nm CMOS | 0.13um CMOS | 90nm CMOS | 45nm SOI CMOS |

measured PN for different division ratios. Table IV compares this ILFD with other published mm-wave frequency dividers. Note that this power is slightly higher than reported in the mm-wave synthesizer power breakdown (Fig. 16), due to the higher operating frequency quoted in Table IV. It achieved the highest input frequency and the lowest power consumption among these programmable frequency dividers.

## V. CONCLUSION

An mm-wave two stage frequency synthesizer has been presented in this article. To reduce the PN of the first-stage PLL, a type-I RSPLL has been implemented. Compared to an SSPLL, the RSPLL can achieve similar in-band PN performance, yet with greatly improved locking robustness without using additional frequency locking loop. Unlike prior RSPLLs, a reshaping reference clock buffer has been proposed to adjust the reference slope. This scheme balances the detectable range and the gain of the sampling PD, leading to optimum PLL PN performance and robust loop dynamics under external disturbances. Using a type-I PLL, the LF size can be greatly reduced, leading to a compact fully integrated mm-wave PLL design. The second-stage ILFM uses an ILVCO to provide a four times higher frequency for mm-wave frequency generation. A low-power FTL-detecting frequency deviation was proposed in order to calibrate the VCO free-running frequency and improve the locking robustness of the ILVCO with a high $Q$ tank against process-voltage-temperature (PVT) variations. The FTL was assisted with an mm-wave injection-locked divider capable of multi-modulus integer divisions. The first-stage RSPLL achieved a high FoM of $-248$ dB at 8.96-GHz output and the overall mm-wave synthesizer achieved an FoM of $-238.9$ dB at 35.84 GHz.

## ACKNOWLEDGMENT

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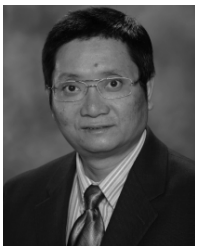

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