A 7.7~10.3GHz 5.2mW −247.3dB-FOM Fractional-N Reference Sampling PLL with 2nd Order CDAC Based Fractional Spur Cancellation In 45nm CMOS

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***Abstract*—In this paper, a fractional-N reference sampling PLL (RSPLL) is presented. To mitigate the frac-N induced quantization error, a capacitor digital-to-analog converter (CDAC) based canceller has been implemented at the reference sampling phase detector (RSPD) output. The RSPD is programmed to provide a detection range of one VCO cycle which is enough to cover the quantization error in frac-N mode. The CDAC is also reused as the sampling capacitor for RSPD. Additionally, a second order cancellation scheme is implemented with only one capacitor array and two reference voltages to compensate for the nonlinearity from RSPD. The prototype chip was fabricated in a 45nm partially-depleted silicon-on-insulator (PDSOI) CMOS process. Measurement showed an output frequency range covering 7.7~10.3GHz with an integrated jitter (10kHz-10MHz) of 190fs and an in-band fractional spur level of -56dBc at an offset frequency of 625kHz. The entire PLL consumes 5.2mW and achieves a FoM of -247.3dB.**

Keywords—PLL; reference sampling; CDAC; frac-N; spur cancellation.

I. Introduction

Conventional PLLs detecting phase error in time domain using phase frequency detector (PFD) suffer from poor in-band phase noise due to limited phase detector (PD) gain. Through detecting phase error in the voltage domain, a sub-sampling PLL (SSPLL) [1] achieves a high PD gain that greatly suppresses the PD and charge pump (CP) noise, thus improving in-band noise floor. However, the SSPD has a limited linear range of less than half VCO period, which is not a problem for an integer-N PLL. However, in frac-N mode, the instantaneous phase error can span over several VCO periods, thus the reference clock edge and the VCO edge need to be aligned so that the sampling point falls inside the SSPD linear range. As illustrated in Fig. 1, the reference edge can be adjusted with a digital-to-time converter (DTC) in accordance with the instantaneous quantization error. DTC suffers from nonlinearity issues due to different slope with various delays and usually requires calibration or large parallel loading capacitor that needs to be charged and discharged every cycle [2]. Moreover, as at least one complete VCO cycle of delay needs to be covered by DTC, larger capacitor array is needed to reduce the noise contribution from DTC. Alternatively, one can utilize a phase interpolator (PI) to generate multiple sub-phases of VCO clock, thus narrowing down the quantization error. Using PI significantly relaxes the amount of required additional delay compared to DTC. However, PI requires higher power consumption as it is operating at VCO frequency.

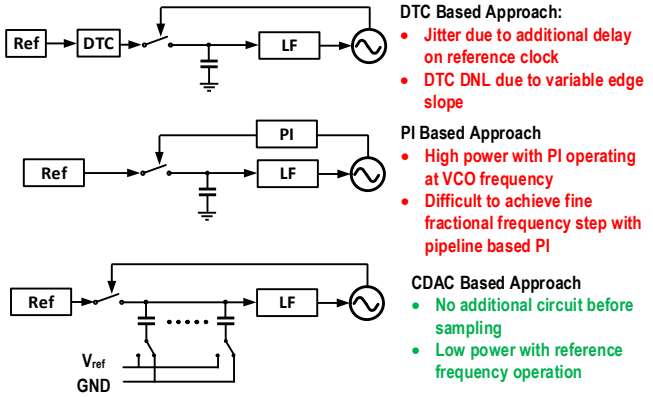

Fig.1. Conceptual diagram of different approaches to achieve fractional-N operation for a reference sampling PLL.

Depending on specific architecture, a current mode PI [3] suffers similar DNL issue as in DTC due to varying slope whereas a pipeline based PI can be very challenging as circuit complexity quickly grows with finer fractional frequency step [4]. Additionally, quadrature output is usually needed from VCO for interpolation which also increases VCO design complexity.

In the aforementioned two schemes, the instantaneous frac-N induced quantization error is cancelled in the time domain using additional circuits on the reference path or at the VCO output, which contribute extra noise and power consumption. In this paper, we present a third approach where the quantization error is tackled in the voltage domain at SSPD output. Three key benefits of this approach are: 1. Additional delay generating circuits before sampling can be avoided to reduce noise overhead in frac-N mode; 2. Low power and hardware overhead with reference frequency operation and shared circuitry between sampler and quantization error canceller; 3. Higher linearity can be obtained with a voltage domain digital-to-analog converter (DAC) compared to a time domain DTC, thus achieving better cancellation results.

II. Proposed Frac-N RSPLL Architecture

A. Frac-N Operation with Reference Sampling

Instead of sampling the VCO edge using the reference edge as in SSPLL, one can reversely sample the reference edge using the VCO as the clock, namely the reference sampling phase detector (RSPD) in [5]. As shown in Fig. 2, a

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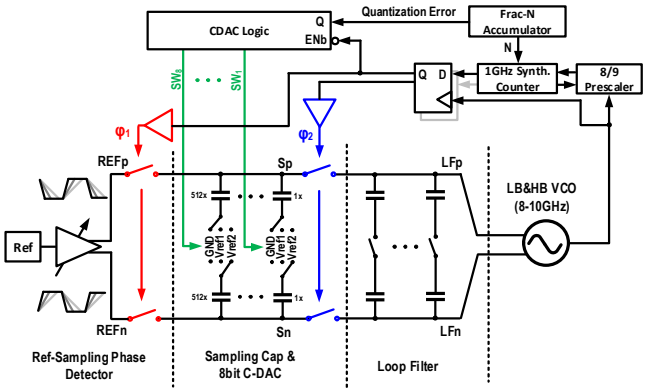


Fig.2. Block diagram of the proposed frac-N type-I reference sampling PLL architecture with CDAC quantization error cancellers.

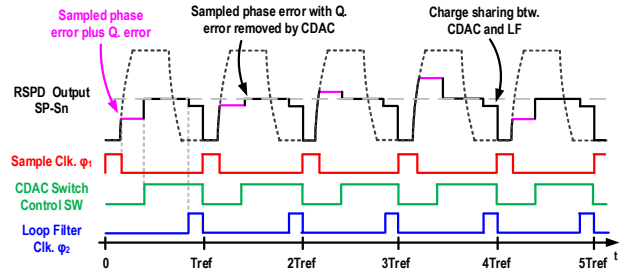


Fig.3. Timing diagram of the fractional-N operation with proposed CDAC spur cancellation technique.

reshaping buffer has been implemented on the reference clock to tune its edge slope (REFp/REFn) before being sampled by the VCO clock. The sampled reference slope can be adjusted to achieve larger RSPD linear detection range but at the cost of lower RSPD gain. In this design, RSPD is tuned to achieve a sufficient linear range of one VCO cycle to handle the fractional phase error, while still maintaining a reasonably large PD gain to achieve low in-band noise floor. In addition, the reference slope can be adaptively tuned with a wide detectable range (slow slope) during acquisition and a high gain (sharp slope) at the lock to achieve fast locking and low noise simultaneously.

At the output of sampling switch, the sampling capacitor is broken down into multiple small units, forming an 8-bit CDAC with switches at the bottom plate connecting to either ground or reference voltages. The sampled voltage (Sp/Sn) captures the desired phase information as well as its quantization error as illustrated in the timing diagram of Fig. 3. Leaving the quantization error uncompensated, large fractional spurs will arise at the PLL output. Therefore, the CDAC is utilized to generate a reversed quantization error in the voltage domain during the hold phase to cancel the quantization error from each sampled voltage. The CDAC bottom plate switch is toggled shortly after RSPD goes into hold phase. After voltages on Sp/Sn settle down, the loop filter is connected to update the VCO tuning voltage (LFp/LFn). Thus with ideal cancellation, the VCO will only see constant tuning voltage in frac-N mode, eliminating fractional spurs.

Although using a current DAC at the analog PFD output has been reported in classic analog frac-N PLLs, our approach

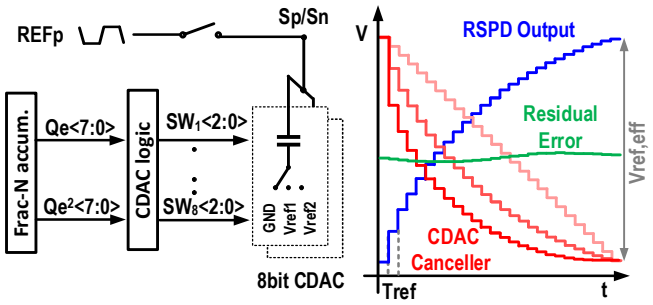


Fig.4. Nonlinearity of the reference sampling phase detector with the CDAC spur canceller; Second order nonlinearity of the CDAC canceller can be tuned with Vref1 to achieve optimal cancellation.

TABLE.I CDAC SWITCHING CONTROL LOGIC.

Qe<k>	Qe²<k>	Switch position (SW_k) in sample phase	Switch position (SW_k) in hold phase
0	0	GND	GND
0	1	Vref2	Vref1
1	0	Vref1	GND
1	1	Vref2	GND

is more elegant when combined with a voltage domain RSPLL in a way that the CDAC and the sampling capacitor are naturally merged into one capacitor array similar to a SAR ADC. Compared to the time-domain quantization error reduction techniques using a DTC or a PI, the proposed CDAC approach adds negligible noise and power by avoiding additional circuits on the critical signal path before sampling. All the CDAC charging and discharging activities operate at the reference frequency, consuming ignorable power. The CDAC gain calibration for spur reduction needs to be performed only for the lock state. In addition, the CDAC related noise including sampling noise and noise from reference voltages is also suppressed by the high PD gain.

B. Second Order CDAC based Quantization Error Canceller

To cancel the frac-N quantization error at the sampler output, two factors need to be considered. Firstly, the magnitude of the CDAC canceller needs to match that of the quantization error. As shown in Fig. 4, the effective CDAC reference voltage $V_{ref,eff}$, which determines the magnitude of the CDAC canceller, should be set to $T_{vco} \cdot S_{ref}$, namely, the VCO period times the slope of the reshaped reference edge. Secondly, the Ref slope approximately follows a single pole RC charging/discharging profile, thus it presents nonlinearity. The integral nonlinearity (INL) can be reduced by making the reference slope slower. However, this would reduce the RSPD gain and increase the in-band noise.

In this regard, a high order canceller is implemented to simultaneously cancel the first and the second order quantization errors using only one sampling capacitor array with three switchable voltage levels for each control bit as shown in Fig. 4. Each bit can be switched to ground, V_{ref1} or V_{ref2} ($V_{ref2} > V_{ref1}$). Two 8-bit digital words representing the instantaneous divider quantization error (Q_e) and its square term (Q_e^2) are calculated based on the on-chip fractional

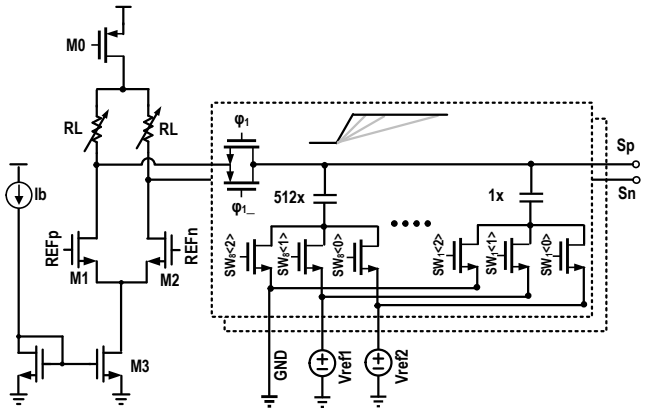
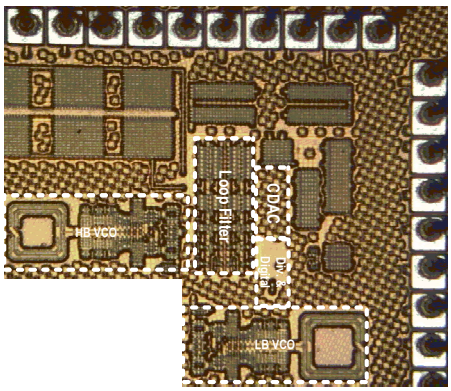


Fig.5. Schematic diagram of the RSPD consisting of programmable reference reshape buffer with CDAC quantization error canceller.



Module	Power (mW)
RSPD	0.5
VCO	3.3
Divider	0.7
VCO buffer	0.5
Digital	0.2
Total	5.5

Fig.6. Die photo and power breakdown of the prototype RSPLL chip.

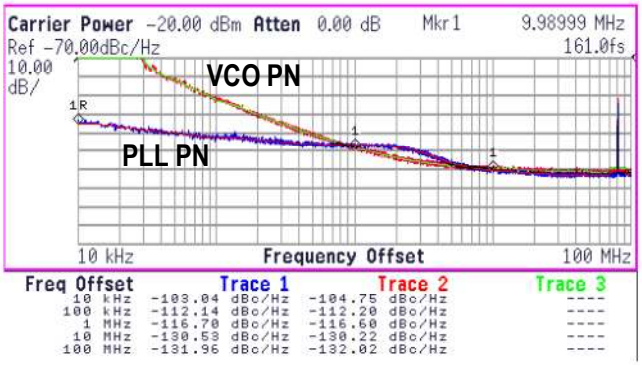


Fig.7. Measured VCO free-running phase noise and PLL output phase noise in integer mode at 4.12GHz (VCO running at 8.24GHz).

accumulator outputs. Next, an integrated CDAC decoder converts every bit of the quantization error into the actual switch control signal SW1~SW8, corresponding to each control bit in the CDAC. The switch position is toggled accordingly between the sampling phase and the hold phase to generate the precise anti-RC-ramp cancellation waveform as shown in table I. The magnitudes of the first and the second order canceller are determined by V_{ref1} and $V_{ref2} - V_{ref1}$, whereas the total magnitude of the combined canceller equals to V_{ref2}, or simply:

$$V_{canceller} = V_{ref1} \cdot Q_e + \left(V_{ref2} - V_{ref1}\right) \cdot {Q_e}^2 \quad (1)$$

Thus, through setting V_{ref2} to $V_{ref,eff}$ (the effective reference DAC voltage) for gain matching and sweeping V_{ref1}, the proposed CDAC scheme can cancel the second order distortion of the RC ramp for optimal fractional spur reduction. This scheme is equivalent to adding a pre-distortion on the CDAC to compensate the 2nd order non-linearity of the RSPD. The proposed CDAC canceller can be extended to even higher orders of cancellation in a similar fashion. In this work, for a quick proof-of-concept, the reference voltages are set externally. For a more complete design, they can be implemented with an on-chip sigma-delta DAC. Using a background least-mean-square (LMS) based digital calibration similar to [6], the reference voltage can be dynamically tuned for optimal fractional spur cancellation under PVT variations.

III. CICRCUIT IMPLEMENTATION

Referring back to Fig. 2: the loop divider consists of a high-speed 8/9 prescaler which divides VCO frequency down to 1GHz and is followed by a synthesized digital counter to support continuous loop division ratio. The digital counter also works as an integrated finite state machine (FSM) which provides various control signals to RSPD, CDAC and loop filter (LF). To implement frac-N operation, the loop divider is controlled by a fractional accumulator, or a first order sigma delta modulator, to achieve fractional division with a maximum quantization error of one VCO cycle. The fractional accumulator also calculates the instantaneous quantization error which is further encoded by the integrated CDAC logic circuit to control switches in the bottom plate of CDAC. The counter output is retimed with VCO clock to clean up accumulated jitter from digital circuits. The retimed divider output φ_1 is used to sample the reference edge. The LF after the RSPD is implemented with a switch capacitor circuit. A pulse φ_2 generated by the digital counter controls the switch for charge sharing between the sampling capacitor and the LF capacitor, making it a type-I PLL. The RSPD and the LF are implemented with fully differential topology for better common mode noise rejection. Two class-C VCOs covering low band (LB) and high band (HB) frequency ranges have been implemented, yet only one VCO is enabled at a time.

As shown in Fig. 5, the reference reshaping buffer which is implemented with current mode logic (CML) adjusts the reference slope in order to achieve the desired RSPD gain with a proper detectable range. The slope is controlled through tuning the CML load resistors RL which is programmable from 100Ω to 1.2kΩ. The CDAC has a total of 2pF capacitor on each side, thus the time constant at Sp/Sn can be programmed from 200ps to 2.4ns. The edge rising time at Sp/Sn is desired to be longer than the VCO period (~120ps) to reduce the higher order terms in the sampled RC-ramp for better cancellation result. Tail current source M3 is also tuned with RL accordingly to maintain a constant swing of about 600mV at RSPD output. Duty cycle has been implemented with M0 such that RSPD is only enabled during sampling phase to save power. Two external tunable reference voltages are connected to CDAC for second order cancellation. In each reference cycle

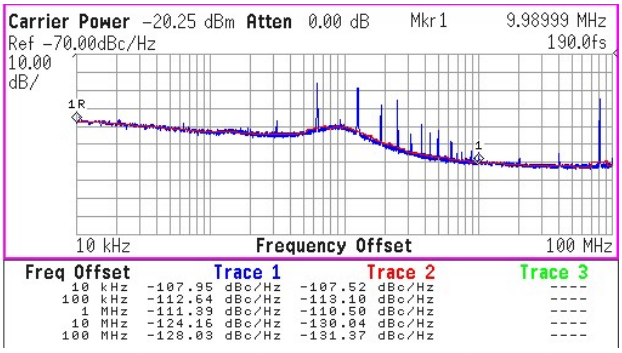


Fig.8. Measured PLL output phase noise in frac-N mode around 4.12GHz with a fractional frequency of 625kHz.

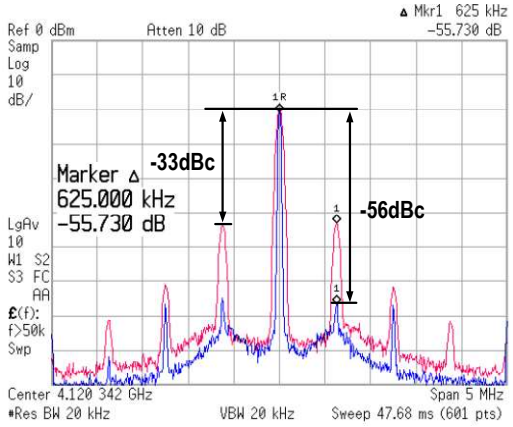


Fig.9. Measured PLL fractional spur level using 1st and 2nd order CDAC quantization error canceller.

(12.5ns), 3.5ns is assigned to sampling phase (φ_1), 7ns is assigned to CDAC settling and the loop filter (φ_2) is connected only during the remaining 2ns. In this way, ample time is given to CDAC to relax the driving strength of reference buffers.

IV. Measurement Results

The RSPLL prototype was fabricated in a 45nm PDSOI CMOS technology with an active area of 0.19mm^2 (Fig. 6). It uses a reference clock frequency of 80MHz. The LB/HB VCO frequency ranges cover 7.7~8.9GHz and 8.9~10.3GHz, respectively. The PLL output was divided by 2 for measurement. As shown in the power breakdown chart, the entire PLL consumes 5.2mW under a 1V supply, where majority of the power was consumed by the VCO. As shown in Fig.7, integer-N mode was measured at 4.12GHz (VCO running at 8.24GHz), achieving an integrated jitter of 161fs (10kHz-10MHz). The frac-N mode was measured with a fractional frequency of 625kHz (fractionality of 1/128 with spur located inside the loop bandwidth). The integrated phase noises in fractional-N mode is measured as 190fs (10kHz-10MHz) including all the spurs as shown in Fig. 8. Using the 1st order CDAC canceller only, the fractional spur reduces to -33dBc. After enabling the 2nd order cancellation, the spur is further improved to -56dBc as shown in Fig. 9. With both CDAC cancellers turned off, the in-band frac-N spur reaches -10dBc (not shown here). The performance summary and comparison table are given in Table II. This 7.7~10.3GHz RSPLL design has achieved a FoM of -247.3dB.

TABLE.II Measured PLL Performances and Comparisons.

	ISSCC 2016 [7] X. Gao	JSSC 2016 [4] A. Narayanan	This Work
Technology	28nm	65nm	45nm
PLL structure	Sub-sampling	Sub-sampling	Ref-sampling
Frac-N tech.	DTC	PI	CDAC
Freq. (GHz)	2.7~4.33	4.34~4.94	7.7~10.3
Ref. (MHz)	40	40	80
In-band frac. spur (dBc)	-54	-59	-56
Integrated jitter (fs)	159 (10kHz-40MHz)	133 (10kHz-10MHz)	190 (10kHz-10MHz)
Power (mW)	8.2	6.2	5.2
FoM* (dB)	-246.8	-249.5	-247.3

*FoM $= 10\log_{10}(\sigma_{\text{jitter}}{}^2 * \text{Power}/1\text{mW})$

V. Conclusions

A fractional-N RSPLL has been presented in this paper. Tackling quantization error at phase detector output in the voltage domain through CDAC offers the advantage of not introducing extra delay and its associated accumulated jitter in the critical loop path before sampling. Additionally, using CDAC canceller only consumes small amount of power overhead as it is only operating at reference frequency. Reusing the sampling capacitor as the CDAC also reduces the extra circuit and silicon area required from integer mode to frac-N mode. The second order quantization error cancellation implemented further helps suppressing frac-N spurs due to nonlinear RSPD output. Fabricated with 45nm PDSOI process, our prototype RSPLL chip has achieved an integrated jitter of 190fs at 8.24GHz while consuming 5.2mW in total with an in-band frac-N spur level of -56dBc, achieving a FoM of -247.3dB.

Acknowledgment

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