A 280MS/s 12b SAR-Assisted Hybrid ADC with Time Domain Sub-Range Quantizer in 45nm CMOS

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***Abstract*— This paper presents a successive approximation register (SAR) assisted hybrid analog to digital converter (ADC) that uses a time domain quantizer for sub-range quantization. The proposed hybrid ADC utilizes an 8b 2bit-per-cycle SAR coarse ADC pipelined with a 6b 2-dimensional Vernier time-to-digital converter (TDC) as the fine quantizer for high-resolution and high conversion rate. Different from the conventional approach, the voltage residue is converted into time domain for fine quantization which greatly relaxes the power-to-noise requirement of the comparator for high-resolution. Moreover, the 8b coarse quantization stage greatly reduces the range of the residue signal and thus dramatically relieves the linearity requirement of the voltage-to-time (V-T) conversion. The LSB of the TDC is digitally calibrated thus the gain accuracy of the pipeline stage is relaxed. The prototype was fabricated in a 45nm CMOS process, and the ADC core dissipates 3.66 mA from a 1-V supply with an active area of 0.08mm^2. The prototype chip achieves a measured peak SNDR of 65.7dB and SFDR of 80.7dB at conversion rate up to 280MS/s. The calculated Walden and Schreier figures-of-merit (FoM) are 8.4fJ/conv.-step and 171.5dB, respectively.**

Keywords*— Hybrid ADC, SAR, 2b/c SAR, 2D Vernier TDC.

I. Introduction

The successive approximation register (SAR) ADC has gained increasing popularity due to its high-power efficiency for moderate resolutions (8-12 bits). While the speed of a single channel SAR ADC is approaching Giger-Hertz bandwidth, their signal-to-noise-ratio (SNR) performance hardly exceeds 60dB [1], mainly limited by the comparator noise. The power consumption of the comparator grows exponentially with increased resolution requirement. Pipelined SAR ADC [2-3] does not require a low noise comparator by inserting gain stages. However, such amplifier normally has stringent gain (large and accurate) and linearity requirements. In advanced CMOS technology node, the design of a high-performance voltage amplifier becomes rather challenge. Instead of processing the signal in voltage domain, quantization using time domain signal processing thus became attractive, where conversion can be done using time-to-digital converters (TDC) with much lower power. Although time-domain quantization is inherently low noise, the prior-art TDC based ADCs have limited resolutions due to the linearity issue associated with the TDC and the voltage-to-time converter (VTC). Coarse-fine ADC architecture using a time domain quantizer for fine quantization were proposed in [1] [4] [5], yet their conversion speed hardly exceeds 100MS/s due to the speed limit of the time-quantizers.

This paper presents a coarse-fine pipelined hybrid ADC that utilizes a SAR ADC for coarse quantization and a high-performance TDC for fine quantization. The operational principle is illustrated in Fig. 1. The proposed architecture provides following advantages. 1. The SAR ADC is only used for coarse conversion; thus, the comparator noise is greatly relaxed, and power efficiency is improved. 2. After the coarse quantization process, the residue signal is contained within a relatively small range which dramatically relaxes the linearity requirement of the VTC stage. 3. Unlike traditional ADCs that need to deal with the fine voltage signal while balancing the noise in comparators, the time-based signal processing circuits such as TDCs have better noise tolerance. The noise immunity for time-domain signal processing can be understood by considering AM versus PM/FM in communications. In addition, TDC designs benefits from the technology scaling achieving fine resolution due to fast transition, small area, and low power, where the fast transitions reduce the circuit susceptibility to noise, especially transistors' flicker noise. With advanced CMOS technologies, resolution of the time interval measurement using TDC can reach sub-picosecond (ps) range [6]. The design requirements of TDC delay stages, as well as its comparators, are therefore much relaxed with smaller feature size. 4. Unlike voltage domain ADCs, the TDC does not requires extra references, which leads to less power consumption. The LSB in the voltage domain and the MSB in the time domain do need to be aligned, and it can be digitally calibrated easily.

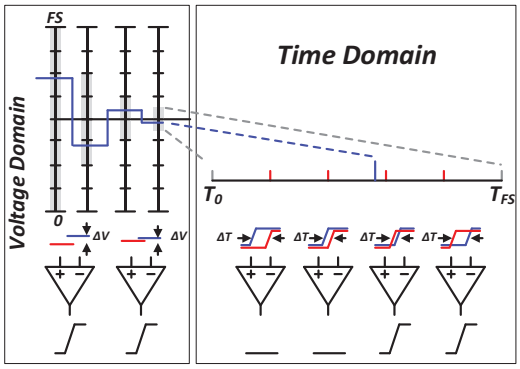

Fig. 1. Illustration of a hybrid ADC consisting of a SAR coarse ADC pipelined with a time domain fine quantizer.

A 12b hybrid coarse-fine hybrid SAR ADC prototype is developed based on the proposed hybrid data-converter scheme. To further improve the speed and linearity performances, the coarse ADC is implemented as an 8b 2-bit-per-cycle SAR ADC and the time domain quantizer is implemented as a 6b 2D Vernier TDC. The architecture and circuit designs are discussed in Section II. A calibration scheme for this architecture is illustrated in Section III, followed by the measurement results and conclusions.

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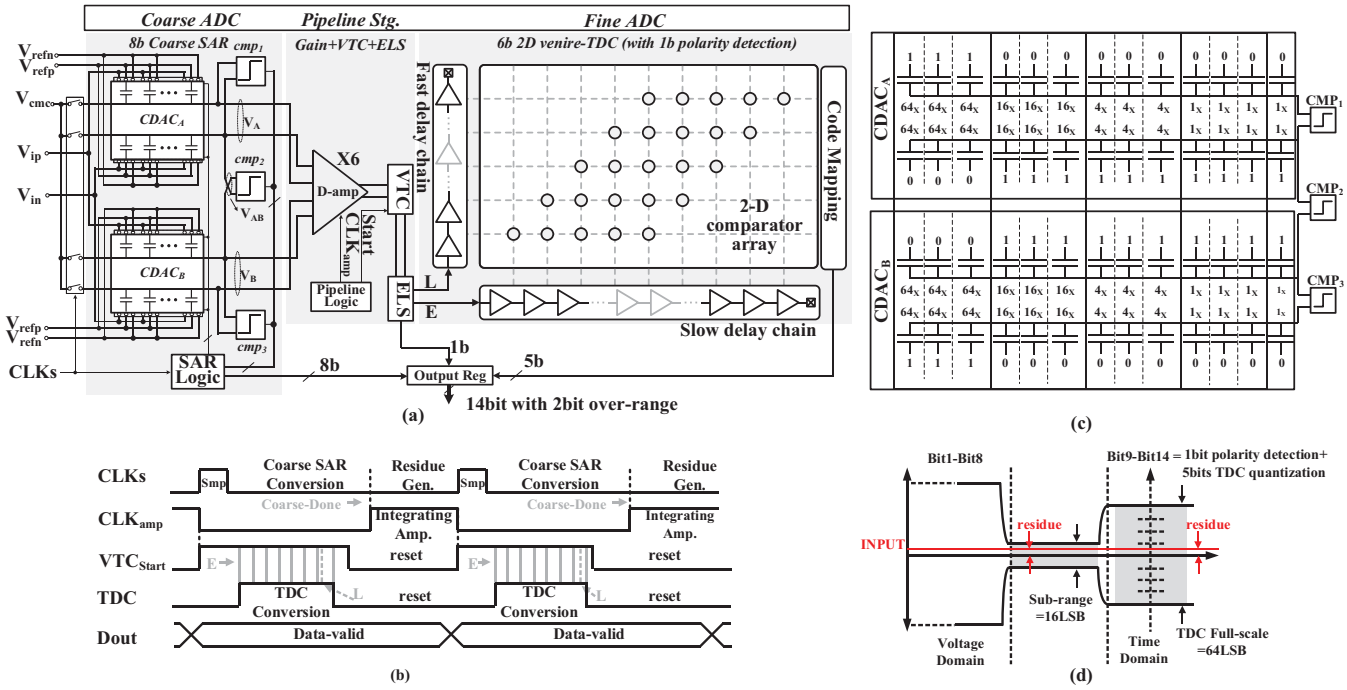

Fig. 2. (a) Block diagram of the proposed 12b hybrid pipelined two-stage ADC with an 8b SAR ADC as the coarse stage and a 6b 2D Vernier TDC as the fine stage. (b) Timing diagram. (c) CDAC implementation with first conversion state illustrated. (d) Over-range illustration.

II. Architecture and Circuits

Fig. 2 (a) shows the block diagram of the 12b ADC consisting of an 8b coarse SAR ADC with 2b/cycle, a pipelining stage, and a 6b sub-ranging fine TDC with 2b over-range.

In the coarse SAR, two capacitive digital-to-analog converters (CDACs), i.e., $CDAC_A$ and $CDAC_B$ generate two corresponding threshold references ($1/4V_{ref}$, $3/4V_{ref}$). For 2b quantization, the mid-reference ($1/2V_{ref}$) is generated by interpolating the two CDAC outputs. In the sampling phase (CLKs high), two differential input signals are sampled by bottom-plate sampling scheme for better linearity. During the conversion phase (CLKs low), zero crossing (ZX) signals are generated at the CDAC top plate by capacitor switching. Comparators $cmp_{1\text{-}3}$ detect the ZX signals and determine in which subrange the finer ZX signals are generated. After four conversion cycles, 8 bits are resolved by the coarse SAR; and in the meantime, the interpolated residue (the difference between the input and the mid-threshold) are sent to the pipeline stage, while the coarse SAR stage is ready for converting next sampled data. The conversion times spent by the coarse and fine stages are carefully balanced to be approximately equal in order to achieve the maximum overall conversion speed.

The pipeline stage consists of a dynamic integrating amplifier (DIA), a VTC and an early-late selection (ELS) circuit. As shown in Fig.2 (b), at the end of the 4th coarse conversion, a coarse-done signal will trigger the DIA clock CLK_{amp}, which is designed with a controlled pulse width to ensure a constant gain, to start the integration and amplification of the residue. The falling edge of CLK_{amp} indicating a successful integration will then trigger the VTC clock VTC_{Start} to further convert the residue

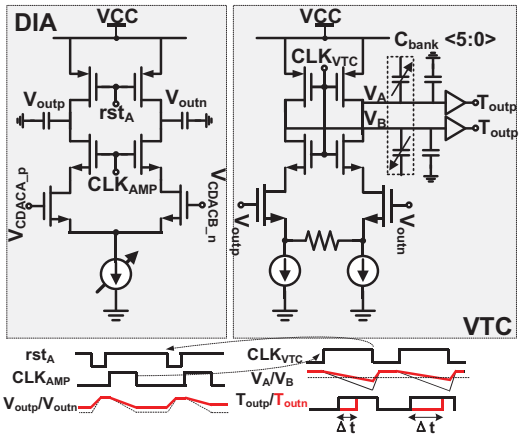

Fig. 3. Simplified circuits and timing diagrams of the DIA and the VTC.

into time domain. Two edges occurring at different time instances will be generated at the VTC output and fed to the ELS circuit. The ELS circuit determines the polarity of the input time signals, i.e., who is lead and who is lag. It separates the input edges into an early edge E and a late edge L, which will be applied to the inputs of TDC's slow and fast chains, respectively. Note that since the sign of the polarity represents the MSB of the time domain quantization. The actual core TDC only needs to resolve 5 bits that are thermometer coded. The 5b TDC results will be mapped together with the polarity bit to form 6b TDC outputs. Unlike voltage domain conversion, the TDC quantization time is input dependent and bounded by the maximum detectable range, which makes quantization process more power efficient on average since it starts once the early

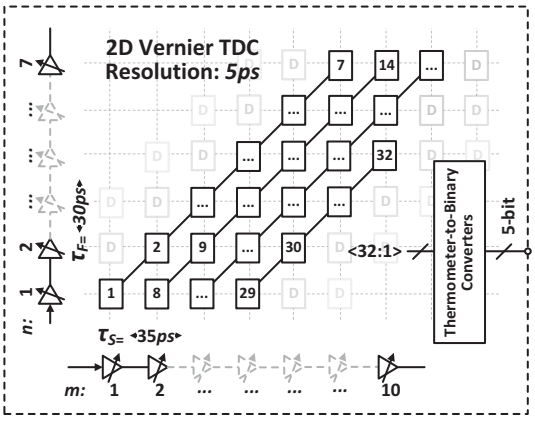

Fig. 4. Block diagram of the 5-bit 2D Vernier TDC with delay calibration.

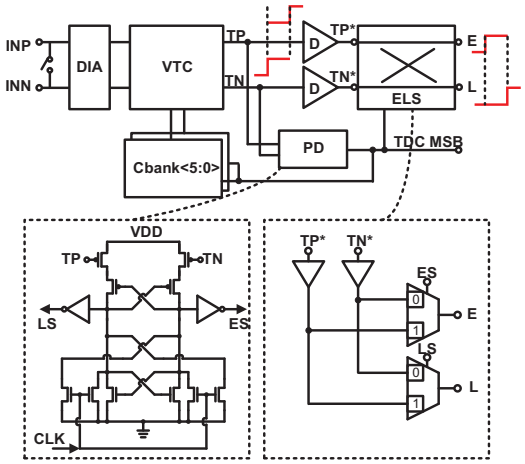

Fig. 5. Pipeline stage offset calibration scheme and circuit implementation of the ELS and phase detector.

edge arrives and stops right after the late edge catches up with the early edge through the delay chains.

Fig. 2 (c) shows the CDAC implementation with its first conversion state. The capacitors are switched as shown to generate the required zero crossing signals for quantization. The CDAC will be then switched accordingly based on the quantization results to shift the thresholds for the next step. The entire CDAC is sized to match the 12bit resolution requirement with unit capacitor sized around 4fF.

2-bit over-range is implemented so that the coarse quantization error due to comparator offset, noise, and incomplete voltage settling on CDACs can be better tolerated in the proposed ADC. The over-range in this design is achieved by expanding the full range of the time domain quantization to 4 times larger (64 LSB) than the original one (16LSB) as shown in Fig. 2 (d), meaning any errors within +/- 24LSB (approximately 8mV) range can be corrected. The final output digital bits include 8 bits coarse SAR data and 6 bits fine TDC data with 2-bit over-range.

Fig. 3 presents the circuit implementation of the pipeline stage. The entire stage is designed based on dynamic architectures and asynchronized logic. The DIA in this design is implemented based on an integrator with constant integration time. Since the residue is amplified and stored at the load capacitors for V-T conversion, the clock for DIA is separated into a reset clock rst_A and an integration clock CLK_{AMP}. The reset phase occurs after the 4th cycle of the coarse conversion and occupies about 150ps. The rst_A's rising edge triggers the integration process which is designed to be around 300ps, resulting in a gain of 6. A successful integration is indicated by the falling edge of CLK_{AMP} which further triggers the CLK_{VTC} to start the V-T conversion. The VTC is also implemented based on integrating scheme with a pseudo-differential structure for better linearity. The VTC reset itself when two edges with time difference are both generated. Two capacitor banks with 6-bit resolution are connected at the load node for offset calibration.

The fine time-domain quantizer is implemented using a 2-D Vernier TDC, as shown in Fig. 4. It comprises two slightly different delay lines and a 2-D comparator array, covering 160 ps range at a resolution of 5 ps. Two edges with their time interval proportional to the coarse SAR ADC's residue magnitude are fed into fast and slow delay chains, while the time interval is quantized by interpolating the position where the late edge propagating in the fast chain captures the early edge propagating in the slow chain. When the position is detected by the comparator array, the TDC automatically stops the quantization process and starts its reset. In a Vernier TDC, the resolution is defined by the difference between delay cells in fast- and slow-chains, which naturally cancels its first order nonlinearity. Compared with other TDC architecture (single-chain or 1D Vernier TDCs), the 2D-vernier scheme provides best performance in terms of conversion speed, resolution and linearity. To further compensate the PVT variations, each delay cell is designed to be tunable within a range of 25 ps to 50 ps. The cells in fast and slow delay chain are tuned to 30 ps and 35 ps, respectively. The output code is translated into binary code through an on-chip thermometer-to-binary converter.

III. Error Corrections

Offset errors in the comparators and the pipeline stages need to be corrected to approach 12b resolution. Due to the over-range technique, the coarse comparator offsets would not cause any ADC output error if the error is limited within the designed error correction range, namely 3 x $FS/2^8$ (16 mV). The coarse comparators are implemented with conventional strong-Arm latch topology, and their offsets are corrected by tuning a capacitor array attached to each intermediate node with the ADC input differentially shorted. The pipeline stage calibration scheme is shown in Fig. 5. The offset is calibrated by adjusting the 6-bit capacitor bank at the output of the VTC with the DIA input shorted with differential zero. The phase detector (PD) embedded in ELS is re-utilized as the tuning indicator for the calibration. The calibration is performed once every conversion period. The figure also shows detailed circuit implementation for PD and ELS.

Though the TDC does not require extra references, the LSB in voltage domain and the MSB in time domain need to be aligned. During the calibration mode, a full-scale voltage difference of the sub-range (64LSB) is generated at the coarse DAC and be quantized by the TDC. The digitally tuned the DIA current source for a full-scale (all-ones) output at the TDC is used for alignment and TDC delay cells are also calibrated to minimize its nonlinearity. To achieve better accuracy TDC

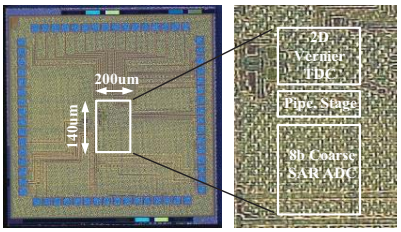

Fig. 5. Die photo of the ADC prototype chip.

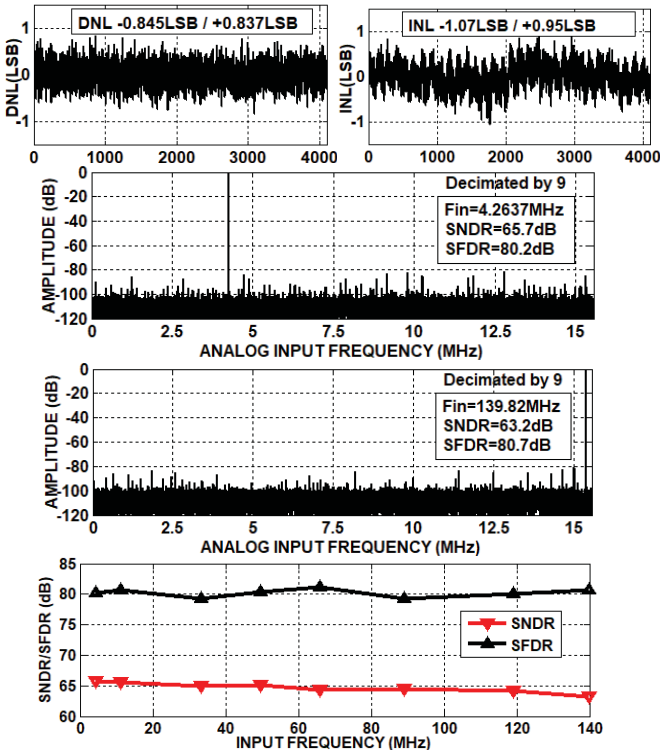

Fig. 6. Measured ADC performaneces (output decimated by 9, 32768 bins).

calibration is performed after all other offset calibrations is done.

IV. Measurement Results

Fabricated in a 45nm SOI CMOS process, the 12b ADC prototype occupies 0.08mm^2 active area as shown in the die photo in Fig. 5. The input swing is approximately 1.4Vpp with all offset and TDC full range calibrated foreground for the setup. The chip achieves a measured INL of -1.07/+0.95-LSB and a DNL of -0.84/+0.83-LSB. At 280MS/s sampling rate, the measured SNDR and SFDR reach 65.7dB, 80.2dB, respectively, with low input frequency. When the input is close to Nyquist frequency, the measured SNDR and SFDR reach 63.2dB and 80.7dB, respectively. The ADC core dissipates 3.66 mA from a 1-V supply. The calculated Walden and Schreier FOM are 8.4fJ/conv.-step and 171.5dB at low input frequency, and 11.2fJ/conv.-step and 169dB at Nyquist input frequency, respectively. The figure also shows the SNDR and SFDR dependence on the input frequency. Table I summarizes the measured ADC performance in comparison with the state-of-art ADCs.

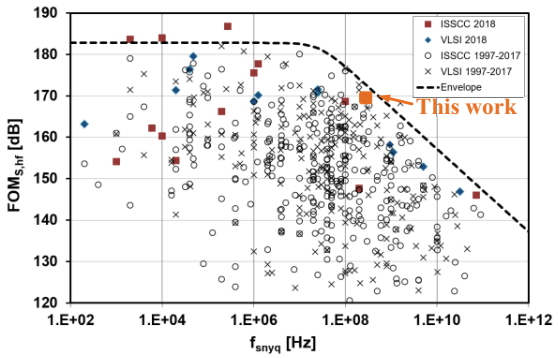

Fig. 7. Comparison of Schreier FoM for this design and the ADCs published at ISSCC and VLSI between 1997 to 2018 based on B. Murman's summary.

V. Conclusions

This work demonstrates a high-resolution, high-speed pipelined hybrid ADC design with a time domain fine quantizer. The 12b prototype ADC implemented in a 45nm SOI CMOS process achieves comparable performance with state-of-art ADCs as shown in Fig. 7.

Acknowledgment

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TABLE I. Performance Summary and Comparison

	This work	[1]	[2]	[3]	[4]
Process [nm]	**45**	28	65	28	130
Resolution [bit]	**12**	12	12	12	12
Supply [V]	**1**	0.9	1.3	0.7	1.3
Fs [MS/s]	**280**	100	330	160	70
SNDR$_{LF}$ [dB]	**65.7**	65.67	67.7	62.0	69.3
SNDR$_{HF}$[dB]	**63.2**	64.43	63.5	61.1	64
Power [mW]	**3.66**	0.35	6.23	1.9	6.38
FoM$_{Walden\ LF}$ [fJ/c.s.]	**8.4**	2.2	9.5	11.5	38.2
FoM$_{Schreier\ LF}$[dB]	**171.5**	177.2	171.9	168.2	166.7
FoM$_{Walden\ HF}$ [fJ/c.s.]	**11.2**	2.63	15.4	12.8	67.9
FoM$_{Schreier\ HF}$[dB]	**169**	176	167.7	167.3	161.7

References

[1] C. Liu, M. Huang and Y. Tu, "A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2941-2950, Dec. 2016.

[2] H. Huang, S. Sarkar, B. Elies and Y. Chiu, "28.4 A 12b 330MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*.

[3] K. Yoshioka *et al.*, "28.7 A 0.7V 12b 160MS/s 12.8fJ/conv-step pipelined-SAR ADC in 28nm CMOS with digital amplifier technique," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 478-479, San Francisco, CA, 2017.

[4] T. Oh, H. Venkatram and U. Moon, "A Time-Based Pipelined ADC Using Both Voltage and Time Domain Information," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 961-971, April 2014.

[5] Y. Chen, K. Chang and C. Hsieh, "A 2.02–5.16 fJ/Conversion Step 10 Bit Hybrid Coarse-Fine SAR ADC With Time-Domain Quantizer in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 357-364, Feb. 2016.

[6] H. Wang, F. F. Dai and H. Wang, "A Reconfigurable Vernier Time-to-Digital Converter With 2-D Spiral Comparator Array and Second-Order ΔΣLinearization," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 738-749, March 2018.