A 3.8 mW Sub-Sampling Direct RF-to-Digital Converter for Polar Receiver Achieving 1.94 Gb/s Data Rate with 1024-APSK Modulation

Hechen Wang[1,2], Zhan Su[1], Haoyi Zhao[1], Yanjie Wang[2], and Fa Foster Dai[1]
[1.] Dept. ECE, Auburn University, Auburn, AL, USA, [2.] Intel Labs, Intel Corporation, Hillsboro, OR, USA

Abstract

This paper presents a direct RF-to-digital converter (RDC) for polar RX. It consists of a pair of TDCs, an ADC, and a precise sampling position control system. Unlike conventional direct-RF sampling receivers, the RDC samples the input RF signal at baseband rate. It is capable of directly digitizing the phase and amplitude of the received modulated RF signals. It is compatible with a variety of modulations and has advantages of relaxed system requirements on phase noise and linearity when APSK is used. The RDC achieves a max rate of 1.94 GB/s with 1024-APSK at a carrier of 6 GHz, consuming only 3.8mW.

Introduction

The next generation portable wireless communication systems are expected to support expanded constellation modulation schemes to achieve multi Gb/s data throughput with restricted power resources. Complex modulation schemes normally come with high-density constellations, such as 256-QAM and 1024-QAM, which demand extremely stringent on both the phase noise (PN) of the PLL, and the linearity of the PA in a conventional Cartesian based I/Q TRX system. In order to meet the requirement, advanced techniques, such as sub-sampling PLLs, and nonlinear compensated PAs have been introduced, which barely support the high-density modulations and leave limited design margin for the overall system. A polar based TRX and modulation scheme require fewer data converter number of bits (NoBs) to reconstruct signals with the same SNR level and have better PN and nonlinearity tolerance due to the nature of the polar coordinate. Although polar TXs have been intensively studied, polar RXs have few successful implementation reports. Meanwhile, the direct-RF schemes have seen increased adoption in both TX and RX of wireless communication systems, due to their unparalleled bandwidth and flexibility. Compared with conventional TRX, the direct-RF gains advantages of less hardware, wider bandwidth, less imaging and aliasing issues. To enable the direct-RF, ultra-high-speed high performance ADCs running at multiple GS/s are indispensable [1-3], however, which consume several hundred mWs or even several Watts of power.

Architecture and Implementation

We propose a direct-RF sampling polar architecture without using high-speed ADCs as shown in Fig. 1. The core of the polar direct RF-to-digital converter (RDC) consists of a pair of reconfigurable TDC and ADC for resolving the phase ($\boldsymbol{\varphi}$) and amplitude ($\boldsymbol{r}$) of the modulated RF signals, respectively. Taking a 64-QAM signal as an example, the proposed RF conversion procedure is illustrated in Fig. 2. The received RF signal is split into two paths: one goes through a limiting amplifier to extract the $\boldsymbol{\varphi}$ information by detecting the rising and falling edges using two TDCs; another goes through an ADC to resolve the amplitude bits $\boldsymbol{r}$. After band limiting filters, the $\boldsymbol{\varphi}$ and $\boldsymbol{r}$ of a modulated RF signal gradually change from one symbol to another over one baseband period as shown in Fig. 2. To ensure an error-free detection, a valid sample position is located within $\pm\lambda/4$ window centered at the baseband transition point, where λ is the carrier period. The prototype RDC consists of an injection-locked multi-phase clock generator providing 64 uniformly distributed phases to cover one baseband symbol period ($1/f_{BB}$), among which five adjacent phases are selected based on a phase selection calibration loop. A 16x ratio is chosen between baseband and carrier frequencies for high data rate applications. The phase selection calibration loop provides fine tuning for the sampling points such that the center of the five phases aligns with the baseband transition point of the received modulated RF signal. The 1st *phs* clock edge resets the TDCs and ADC. The 2nd *phs* edge enables the TDCs to sense the rising and falling zero-crossing points of the modulated signal. The two TDCs detect the time interval between the zero-crossing point and the following clock edges of either *phs*3 or *phs*4. The resolution and NoB of the two TDCs are 2ps and 5bits covering a maximum range of 64ps. The two most significant bits of the TDC are obtained as follows: the 7th bit is 1 when the rising edge TDC revolves the result first, otherwise the result is 0; the 6th bit is 1 when the *phs*3 clock is used for comparison, otherwise the result is 0. The symbol amplitude $\boldsymbol{r}$ is represented by the peak of the waveform, which occurs at the time $\lambda/4$ prior or after the detected zero-crossing point. The ADC sampling points are aligned based on the measured $\boldsymbol{\varphi}$ result. However, in order to place the sampling points within the $\pm\lambda/4$ detection window, amplitude detection may need to happen before the $\boldsymbol{\varphi}$ detection is completed. Therefore, we decide to transmit every symbol twice. The first one is used for $\boldsymbol{\varphi}$ detection and the result is used to adjust the sampling point for $\boldsymbol{r}$ detection in the second cycle as shown in the lower part of Fig. 2. Note that only one sample is needed per symbol due to TDC assisted amplitude sample point alignment. In this design, a 200MS/s symbol rate is achieved, which is limited by the sample rate of the ADC. With the aid of the TDC and the ADC sampling position adjustment system, a sub-sampling process is applied to the modulated RF carrier to detect the baseband information without down-conversion.

The proposed polar RDC is compatible with polar based modulations. Fig. 3 compares the constellations between Cartesian based QAM and polar based amplitude and phase shift keying (APSK) modulation. The APSK is presented with less NoB in a polar system. Additionally, the error span due to PN and nonlinear distortion is proportional to the distance from the origin to the constellation point. For QAM, the outer points are much more sensitive to phase variations and nonlinear distortions. In contrast, the APSK modulation has a larger impairment tolerance margin and better efficiency for implementation in polar systems.

A low power high-speed 2D Vernier TDC is adopted in the proposed RDC (Fig.4) providing 4 or 5 bits for $\boldsymbol{\varphi}$ detection. The resolution is adjustable between 2ps (5-bit) and 5ps (4-bit) by tuning the delay cells and rearrange the comparator array. For amplitude detection, a 2-stage hybrid ADC is implemented consisting a 2-bit per cycle SAR-ADC and a 4-bit (2 redundant bits) sub-ADC. The adopted ADC is also reconfigurable by controlling the number of SAR conversion cycles to produce 4, 6, or 8 bits amplitude output. The configurability allows improved power efficiency for detection of different modulation types at various data rates.

Measurement Results

Measurements were taken to compare the performances of QAM and APSK using our proposed polar RDC in presence of commonly seen impairments such as PN and nonlinear distortion characterized in SNR. Modulated signals from a signal generator source are presented in Fig. 5 together with the measured reconstructed digital data points of the polar RDC output. Although the proposed RDC can detect both QAM and

APSK waveforms, Cartesian QAM modulation is shown to be more sensitive to errors. The performance was evaluated with BER. As expected, the APSK outperforms the QAM modulation when PN and nonlinear distortion are presence. To achieve the same BER, 1024-APSK relaxes the requirement of PN by 6dB and the distortion by 8dB, respectively, compared with 1024-QAM. Blocker tolerance is also measured. As shown in Fig. 6, the APSK modulation has better in-band blocker tolerance when using RDC for conversion. APSK's BER is apparently independent to the blocker location and is lower than that of the QAM signal when the blocker is close to the wanted signal, which is more challenge for filtering. Moreover, the decay of the APSK error is much faster than the error of the QAM as the power of the in-band blocker declines. These comparisons legitimate the use of polar modulated data receiving and conversion proposed in this paper. Fig. 6 summarizes the performance of RDC and Fig. 7 gives the die photo of the prototype and the measurement setup.

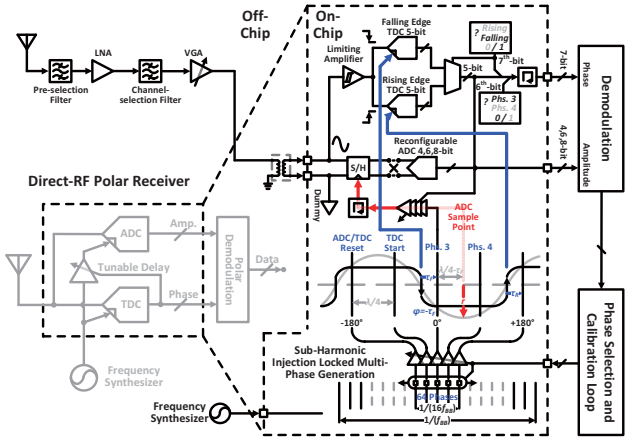


Fig. 1. Proposed polar RX architecture with direct-RF data conversion using a TDC/ADC based RF-to-Digital polar data converter.

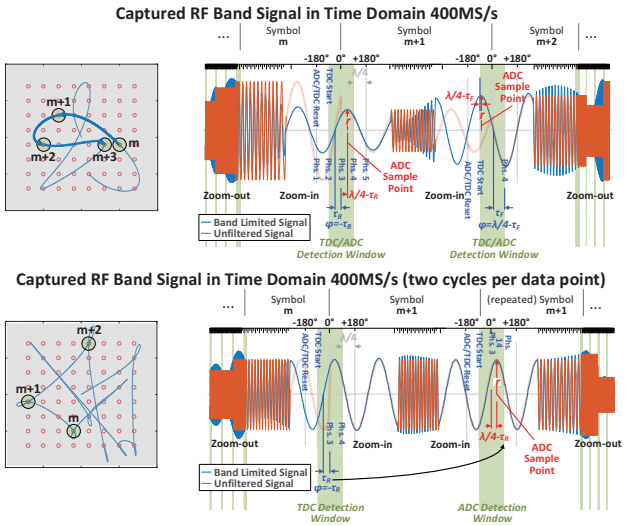


Fig. 2. Illustration of RF-to-digital conversion for a 64-QAM signal using TDC and ADC for phase (φ) and amplitude (r) conversions.

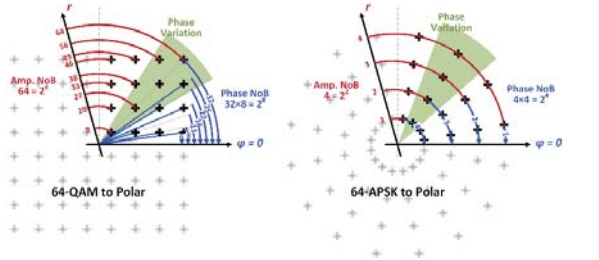
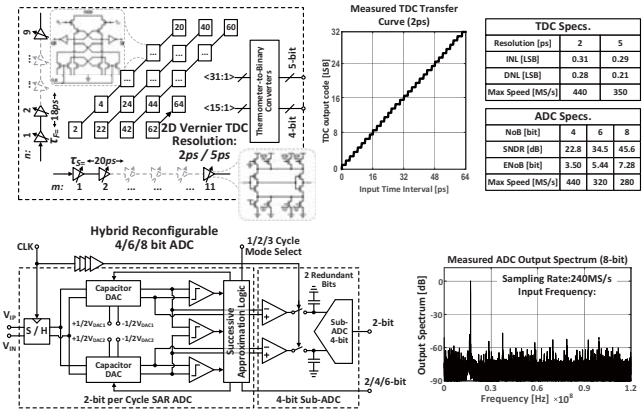


Fig. 3. Comparison of error tolerance between QAM and APSK.



TDC Specs.		
Resolution [ps]	2	5
INL [LSB]	0.31	0.29
DNL [LSB]	0.28	0.21
Max Speed [MS/s]	440	350

ADC Specs.			
NoB [bit]	4	6	8
SNDR [dB]	22.8	34.5	45.6
ENoB [bit]	3.50	5.44	7.28
Max Speed [MS/s]	440	320	280

Fig. 4. Architectures and measured performances of the 2D Vernier TDC and the two-stage ADC with 2bit/cycle SAR and 4bit sub-ADC.

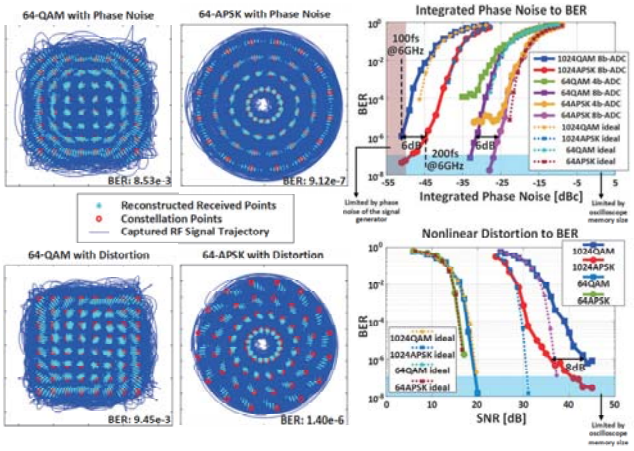


Fig. 5. Comparison of measured BER versus phase noise and nonlinear distortion (SNR) for 64- 1024-QAM and 64- 1024-APSK modulations.

Parameter	This Work			[1] ISSCC' 17	[2] JSSC' 15	[3] JSSC' 16
Technology Process	45 nm CMOS			55nm CMOS	65nm CMOS	28nm CMOS
Die Size	3.0 mm²			8.6 mm²	2 mm² (core)	1 mm²
Supply Voltage	1.1 V			1.8-3.3 V	1 V	1.8 V
Architecture	RF sub-sampling polar			RF sampling	RF sampling	RF sampling
Supporting Modulation	QAM APSK-16/64/256/1024			Impulse	Impulse	QAM-256
Tested Modulation Schemes	QAM-64	APSK-64 Low Power[4]	APSK-64 High Perf.[5]	APSK-1024 Biphase-Coded Impulse	Impulse	QAM-256
Input Frequency [GHz]	6.2[3]	4.4[3]	6.8[3]	6.2[3]	7.3 / 8.7	Up to 12	1
Sampling Rate [GS/s]	0.3875	0.275	0.425	0.3875	1.944×12	666	2.7
Date Rate [Gb/s]	1.16	0.83	1.28	1.94	-	-	10
ADC ENoB [bit]	7.27	7.54	7.11	7.27	-	7.3	12 (NoB)
TDC ERes.[4] [ps]	2.62	6.35	2.81	2.62	-	10.5[5]	-
RF Conv. Power [mW]	3.7	2.7	4.0	3.8	14.0[6]	46.7[6]	300 (w/PLL)

1. Low power mode: 4bit ADC; TDC resolution 5ps.
2. High performance mode: 8bit ADC; TDC resolution 2ps.
3. Maximum frequency with BER < 10^{-6}.
4. Effective Resolution (Eres) = resolution×(INL_{MAX}+1)
5. Digital-to-Time Converter (DTC)
6. Equivalent parts total power.

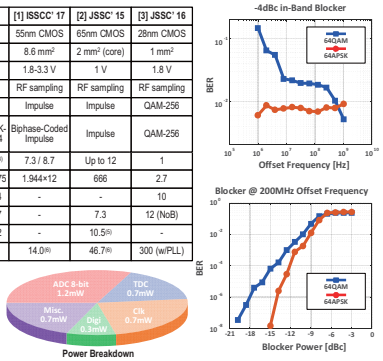


Fig. 6. Performance comparison and blocker tolerance for APSK and QAM as well as power breakdown of the RDC prototype IC.

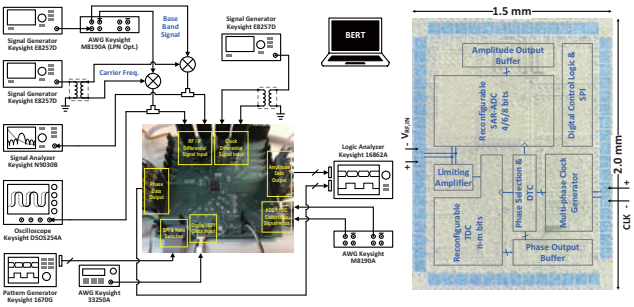


Fig. 7. BER and constellation measurement setup with the capability of phase noise and nonlinearity implantation. And die photo.

References

[1] Y. Kao, *et al.*, *JSSC*, vol.50, no.11, Nov. 2015.
[2] N. Andersen, *et al.*, *ISSCC*, Feb. 2017.
[3] J. Wu, *et al.*, *JSSC*, vol.51, no.4, Apr. 2016.