A Reconfigurable Vernier Time-to-Digital Converter With 2-D Spiral Comparator Array and Second-Order ΔΣ Linearization

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***Abstract*— This paper presents an 8-bit 1.25-ps resolution reconfigurable Vernier time-to-digital converter (TDC) with a 2-D spiral comparator array and ΔΣ modulators for linearization. The proposed spiral 2-D comparator array improves both linearity and detection range of the TDC. The quantization errors introduced by digitally tuning delay cells are minimized by using a 2nd-order ΔΣ modulator. The folding point errors commonly seen in 2-D comparator arrays are randomized by using a reconfigurable comparator array controlled by the output of a 2nd-orderΔΣ modulator. The prototype TDC fabricated in a 45-nm silicon on insulator technology consumes 70- to 690-μW power under a 1-V supply at 80-MHz conversion rate. The measured maximum differential nonlinearity/integral nonlinearity across its detectable range are 1.35/1.03 ps without the linearization techniques and 0.31/0.4 ps with the proposed linearization techniques, respectively.**

***Index Terms*— ΔΣ modulation, autocalibration, differential nonlinearity (DNL), digital phase-locked loop (DPLL), integral nonlinearity (INL), linearization, time-to-digital converter (TDC), Vernier TDC.**

I. Introduction

As CMOS processes keep scaling down in modern deep sub-micrometer technologies, digital phase-locked loop (DPLL) [1]–[3] becomes more prospective than their analog counter parts [4]–[7] due to its capability of programming the loop parameters on the fly, performing direct digital modulations through the PLL, calibrating the loop for superior linearity performance, and its scalability with technology migration. In DPLL designs, time-to-digital converter (TDC) is one of the key building blocks [8], which directly affects the in-band phase noise and fractional spurious level [9]. The in-band phase noise of a DPLL is related to the TDC quantized resolution as

$$\mathcal{L} = \frac{(2\pi)^2}{12}\left(\frac{\tau_{\mathrm{TDC}}}{T_{\mathrm{DCO}}}\right)^2 \frac{1}{f_{\mathrm{ref}}} \tag{1}$$

where τ_{TDC} is the TDC resolution, T_{DCO} is the oscillation period of the digitally controlled oscillator (DCO) output, and f_{ref} is the reference frequency of the DPLL [10]. In order to lower in-band phase noise, the TDC resolution has been reduced to around 1-ps level according to the recently reported data [11]–[14]. However, improving TDC's linearity performance faces increasing challenges particularly for high-resolution TDC. The TDC nonlinearity not only jeopardizes DPLL's in-band phase noise, but also leads to deteriorated fractional spur level in fractional-N DPLLs. When operating in a fractional-N mode, a multi-modulus divider toggles the division ratio between N and $N+1$ and generates a gradually increased phase difference between reference signal and divided feedback signal [15]. Quantized by the TDC, a staircase ramp signal is generated at TDC output, as shown in Fig. 1. Directly feeding this signal into DCO through the loop filter may lead to an unacceptable spur level or unstable loop dynamics. In order to reduce the fractional spurious tones, a digital ripple cancellation technique is often employed [16]. As illustrated in Fig. 1, an ideal staircase ramp is generated following the variation of loop division ratio in fractional mode. This ideal staircase ramp is subtracted from the TDC raw output to cancel its staircase signal while extract the needed dc component. As a result, a less rippled TDC output for DCO tuning is generated, leading to an improved fractional spur performance. However, this spur suppression technique is highly sensitive to TDC's linearity.

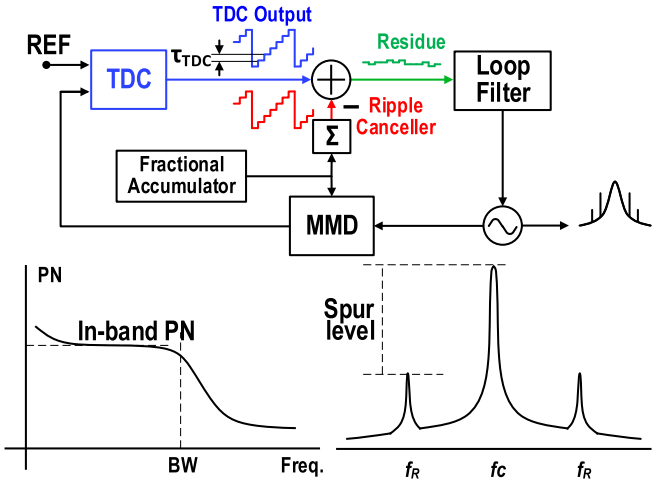

Fig. 1. Illustration of in-band phase noise and fractional spur level related to TDC performance in a DPLL with ripple canceller.

Various TDC architectures for DPLL applications have reported recently. A single delay line TDC or a flash TDC

Manuscript received July 20, 2017; revised September 30, 2017 and November 21, 2017; accepted December 17, 2017. Date of publication January 18, 2018; date of current version February 21, 2018. This paper was approved by Guest Editor Rikky Muller. *(Corresponding author: Hechen Wang.)*

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Digital Object Identifier 10.1109/JSSC.2017.2788872

is the most basic architecture, which quantizes input time interval information using a single chain of inverters. Although it can be easily implemented and has high conversion speed, its time resolution is limited by the CMOS gate delay that is sensitive to process-voltage-temperature (PVT) variations [17]. Vernier TDC formed by two delay chains with slightly different delays can achieve sub-gate delay resolution with improved linearity since the 1st-order mismatches are automatically cancelled [18]. However, its detectable range and conversion rate are greatly limited due to the reduced conversion step size. Consequently, a large number of delay stages are needed to cover the detection range, resulting in high power consumption. Vernier ring TDC achieves fine resolution and large detectable range simultaneously with a reduced hardware configured in a ring structure [19], [20], yet its conversion rate is low for large time intervals. ADC-based TDCs and $\Delta\Sigma$ TDCs achieved good linearity and resolution with even poorer conversion rate [21], [22]. Time amplifier TDC can achieve fine-time resolution and high conversion rate, yet it suffers from limited detection range and high power consumption [23], [24]. Gated-ring-oscillator TDC achieves fine resolution with large range, while its nonlinearity is a drawback due to the device leakage issue [25].

This paper presents an 8-bit 1.25-ps resolution reconfigurable TDC based on the conventional 2-D Vernier TDC topology [26]. The proposed TDC utilizes a novel 2-D spiral comparator array with its folding points reconfigured following the output sequence of a 2nd-order $\Delta\Sigma$ modulator in order to randomize the folding point errors occurred when the comparator lines transit from one to another. The desired delays are interpolated using digital-to-time converters (DTCs) and the delay quantization errors are also randomized with a 2nd-order $\Delta\Sigma$ modulator. Fabricated in a 45-nm CMOS silicon on insulator (SOI) technology, the prototype TDC consumes 70- to 690-μW under 1-V power supply at 80-MHz conversion rate and achieves 0.4-ps maximum integral nonlinearity (INL), which compares favorably among the state-of-the-art TDCs.

The remainder of this paper is structured as follows. Section II discusses the issues associated with conventional 2-D Vernier TDC architecture. A spiral 2-D comparator array arrangement is presented in Section III. Two different $\Delta\Sigma$ linearization techniques are introduced in Section IV to address the linearity issues associated with delay quantization error and folding error in 2-D Vernier TDCs. The measurement results and comparisons are reported in Section V, and conclusions are drawn in Section VI.

II. Linearity Issues Associated With 2-D Vernier TDC

To achieve reasonable in-band noise and fractional spur performances in DPLL designs, TDCs are required to have sub-gate delay resolution according to (1), while its detection range should cover at least one DCO oscillation cycle (i.e., 500 ps for a 2-GHz DPLL) with a reference frequency normally around 50 MHz. Considering all those constraints, the 2-D Vernier TDC is a preferred candidate architecture.

In order to achieve improved detection range with fine resolution, a Vernier TDC with a 2-D comparator array [26],

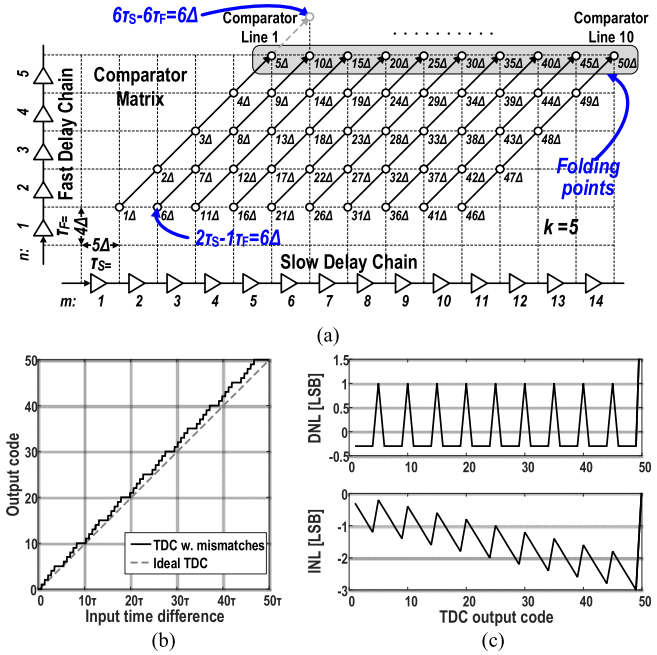

Fig. 2. Illustration of a conventional 2-D Vernier TDC. (a) TDC topology with Vernier delay lines and a 2-D comparator array. (b) Simulated TDC transfer curve. (c) Simulated DNL and INL with 4% delay mismatch.

as illustrated in Fig. 2(a), is evolved from a prior-art Vernier TDC with a 1-D comparator line. The 2-D Vernier TDC has reduced number of delay elements and much higher conversion rate compared with other types of Vernier TDCs. However, the linearity of a 2-D Vernier TDC is more sensitive to delay variations compared to 1-D Vernier TDCs [27], [28].

With a closer look of Fig. 2(a), the TDC consists of two delay chains with two different unit delays τ_S and τ_F, respectively. The resolution is defined by the delay difference, for instance, $\tau_S - \tau_F = 5\Delta - 4\Delta = \Delta$ in this case. The 2-D Vernier TDC breaks the comparator line into multiple sections and forms a 2-D comparator array instead of forming a long single comparator line. The 2-D Vernier TDC uses less delay stages to cover the same detection range. However, each of the segmented comparator line contains k comparators, e.g., k is equal to 5 in this case. The folding points cycled by the gray box in Fig. 2(a) indicate the comparison signal's transition locations into the next comparator lines. The extended sixth comparison point in the first comparator line is equal to $6\tau_S - 6\tau_F = 6\Delta$, while the first comparison point in the second line is equal to $2\tau_S - 1\tau_F = 6\Delta$. In order to ensure a smooth transition between each comparator lines, the two comparisons should produce identical delay response to the input signals, namely, $6\tau_S - 6\tau_F = 2\tau_S - 1\tau_F$. In general, a linear conversion using 2-D comparator array topology requires that

$$k(\tau_S - \tau_F) = \tau_S. \tag{2}$$

This condition demands precisely matched delays in both delay chains against the PVT variations. A small delay deviation can lead to large periodic nonlinearity. Mismatches introduce slope errors, gaps, or overlaps between the comparator lines, producing periodic errors in both differential

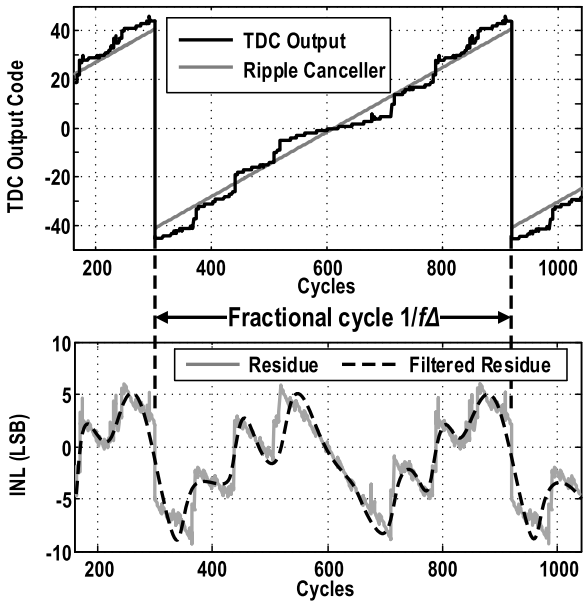

Fig. 3. Measured TDC transfer functions and TDC outputs after the digital ripple canceller, still showing TDC nonlinearity caused by periodic folding errors of the 2-D comparator array.

nonlinearity (DNL) points of the 2-D comparator array topology. To illustrate the problem, a 4% delay mismatch is assumed in the simulation. Fig. 2(b) and (c) presents the simulated TDC transfer curve, DNL, and INL. These plots illustrate that a small delay mismatch could lead to a large nonlinearity in the 2-D Vernier TDC. Indeed, the number of periodic cycles in the nonlinearity plots corresponds to the number of comparator lines with their peaks located at the folding points of the comparator array.

A nonlinear TDC transfer curve can lead to high fractional spur level in a fractional-N DPLL. A 2-D Vernier TDC-based DPLL with digital ripple canceller was presented in [28]. Fig. 3 gives the measured TDC output in its fractional-N operation. The signal has a periodic cycle of $1/f_\Delta = 1/(F \cdot f_{\text{ref}})$, where f_Δ is the closet fractional spur offset frequency and F is the fractionality. In this case, the DPLL is running with a division ratio of $29 + 1/64$ and a reference frequency of 80 MHz. The synthesized frequency is centered at 2.32125 GHz. The closest spur is located at $f_\Delta = 1/64 \times 80$ MHz $= 1.25$ MHz. The 2-D folding point errors can be clearly seen from the measured waveform given in Fig. 3. Subtracted from the ideal staircase waveform generated by the fractional accumulator, the measured TDC residue error, and its filtered version are shown in Fig. 3. Note that the residue error represents the TDC's INL. Even with the digital ripple cancelling technique, the filtered TDC residue error still shows nonlinearity associated with the folding point errors caused by TDC 2-D comparator array, which will be addressed later.

The fractional spurs are affected by TDC nonlinearity and can be analyzed taking Fourier transform of the DCO control signal as illustrated in Fig. 4. The smoothed residue error in time domain is mapped into frequency domain as multiple tones located at f_Δ, $2f_\Delta$, $3f_\Delta$, etc. The DCO output in the loop is modulated by the filtered residue error signal.

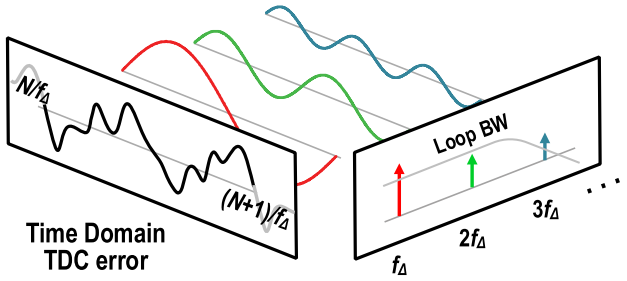

Fig. 4. Fourier transform reveals the relationship between filtered TDC output and up-converted fractional spur components at the DPLL output.

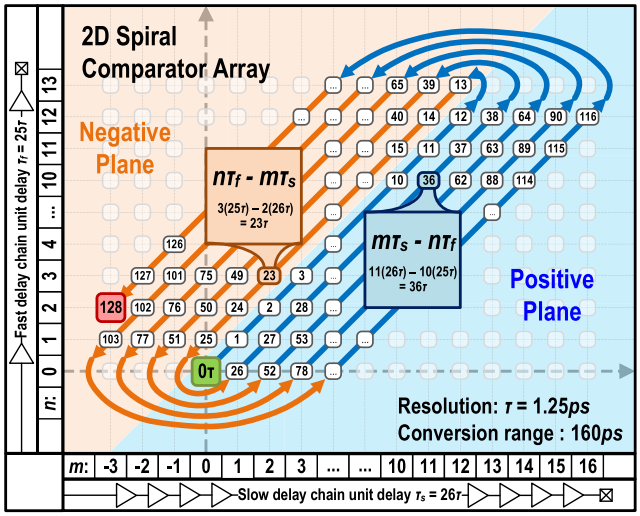

Fig. 5. Proposed Vernier TDC with a 2-D spiral comparator array.

The frequency components of this filtered control signal will be up-converted to DCO's output, showing as fractional spurs. Due to the TDC nonlinearity, the fractional spur level is only around -40 dBc. The fractional spur level can be estimated based on TDC nonlinearity as

$$P_{\text{frac}}(\text{dBc}) = 20 \cdot \log_{10}\left(\frac{K_{\text{DCO}} \cdot A_{f_\Delta}}{2f_\Delta}\right) \tag{3}$$

where K_{DCO} is the DCO gain and A_{f_Δ} denotes the amplitude of the error signal's fundamental tone f_Δ [28].

III. 2-D Spiral Comparator Array Arrangment

Previous discussion reveals that 2-D Vernier TDC peak nonlinearity appears at folding comparator line folding locations. By following a saw-tooth arrangement in the traditional 2-D array, the last comparator in nth comparator line faces much larger accumulated delay mismatches comparing with the first comparator in the $(n+1)_{\text{th}}$ comparator line, leading to a discontinuous transfer curve. To break this trend, we thus propose to configure the 2-D comparator array in a spiral arrangement as shown in Fig. 5 [29]. In this arrangement, instead of folding the comparator line in a saw-tooth form in one direction, we rearrange the comparator path in a spiral shape. Referring to Fig. 5, the comparison points start with climbing up along the comparator line from node "0" in a

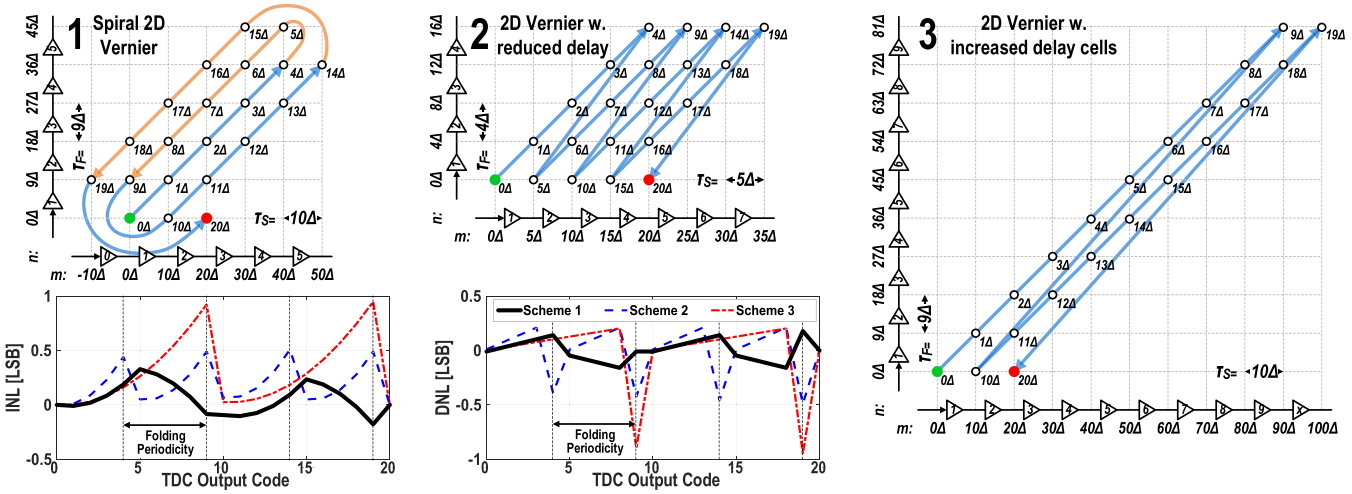

Fig. 6. Comparisons among the proposed 2-D spiral comparator arrangement (scheme 1) and conventional 2-D comparator arrangements (scheme 2 and 3), indicating a better linearity achieved by using the spiral comparator array formation with less delay elements.

similar way to the conventional 2-D Vernier TDC. When reach the folding point, the comparison folds back counterclockwise to the left side and continuous downward, as shown in Fig. 5. The separated two sides of the comparator array have opposite comparison mechanisms: on the right-hand side, it satisfies that $m\tau_S - n\tau_F$ and defined as positive plane, while on the left-hand side it meets that $n\tau_F - m\tau_S$ and defined as negative plane, where n and m are the unit delay index of the fast and slow delay chains, respectively. As a result, the mismatches along the comparison path are partially compensated, resulting in an improved linearity performance.

To compare different comparator arrangements, we use reduced numbers of delay cells to illustrate the proposed spiral arrangement in comparison with other two conventional 2-D arrangements. Scheme "1" shows the proposed 2-D spiral comparator array and is used as the benchmark for evaluation. Schemes "2" and "3" provide two options that achieve the same resolution of "1τ" and conversion range of "20τ" by using conventional arrangements. Scheme "2" uses the same amount of unit delay cells as that of the scheme "1." However, in order to maintain the "1τ" resolution, the temporal delay of its unit delay cells has to be reduced to 5τ comparing to 10τ in scheme "1." Thus, scheme "2" is more sensitive to delay mismatches and parasitic effects. Scheme "3" is built with the same temporal unit delay as that of scheme "1," yet its comparator line length is doubled to fulfill the 2-D TDC linear requirement given in (2), resulting in degraded nonlinearity and increased power consumption due to longer delay lines.

From topological point of view, the comparison path in our proposed 2-D spiral Vernier TDC forms a spiral shape. The comparison starts from the center of the comparator array and gradually fans out to the outer lines, alternately across the positive plane on the right and the negative plane on the left when the input time interval increases. If there are mismatches, the errors accumulated on positive and negative planes will partially cancel with each other. In contrast, in the conventional 2-D comparator arrays, the comparison path follows a saw-tooth shape, moving in one direction on the positive plane, which accumulates mismatch errors.

To further analyze the nonlinearity of the above three schemes, a theoretical model is built based on the theory presented in [26]. Two kinds of errors, absolute delay error $\varepsilon_{\text{Absolute}}$ and local delay error $\varepsilon_{\text{Local}}$, are added, where $\varepsilon_{\text{Absolute}}$ is fixed delay error applied to all the unit delay cells in the delay chains and $\varepsilon_{\text{Local}}$ is a gradually increased delay error along the delay chains, which models the unevenly distributed on-chip doping level. The simulated TDC INL in Fig. 6 reveals that scheme "1" has two opposite INL slopes alternatively appears along the TDC detectable range. As a result, its INL is bounded around zero. The INL slope of scheme "2" is the largest due to the reduced temporal delay of unit delay cells. The scheme "3" ends up with the largest INL due to its longest delay lines along one direction. Moreover, the transitions between comparator lines are much smoother in spiral arrangement comparing with the traditional saw-tooth cases, which end up with much improved DNL as shown in Fig. 6.

Among all these three options, the proposed spiral 2-D scheme achieves the best INL and DNL performance and has the least number of unit delay cells, which indicates less mismatches and fast conversion speed.

IV. Proposed TDC Linearization Techniques and Its Circuit Implementations

A. Delay Interpolation of Unit Delay Cells

Vernier TDCs' nonlinearity mainly comes from the temporal delay errors of the delay units. Minimizing the delay error is the prerequisite for improving its linearity. The unit delay cell in the delay chain comprises a pair of cascaded inverters as shown in Fig. 7(a). To reduce mismatch, both fast and slow delay chains employ identical unit delay cells. In this design, the unit delay is tunable from 19 to 43 ps with seven digitally controlled bits to obtain digital calibration compatibility and meet tuning requirements against PVT variations. The seven delay tuning bits are constructed with six pairs of NMOS and PMOS transistors sized with binary weights. The 1st and 2nd least significant bits (LSBs) of the tuning bits share

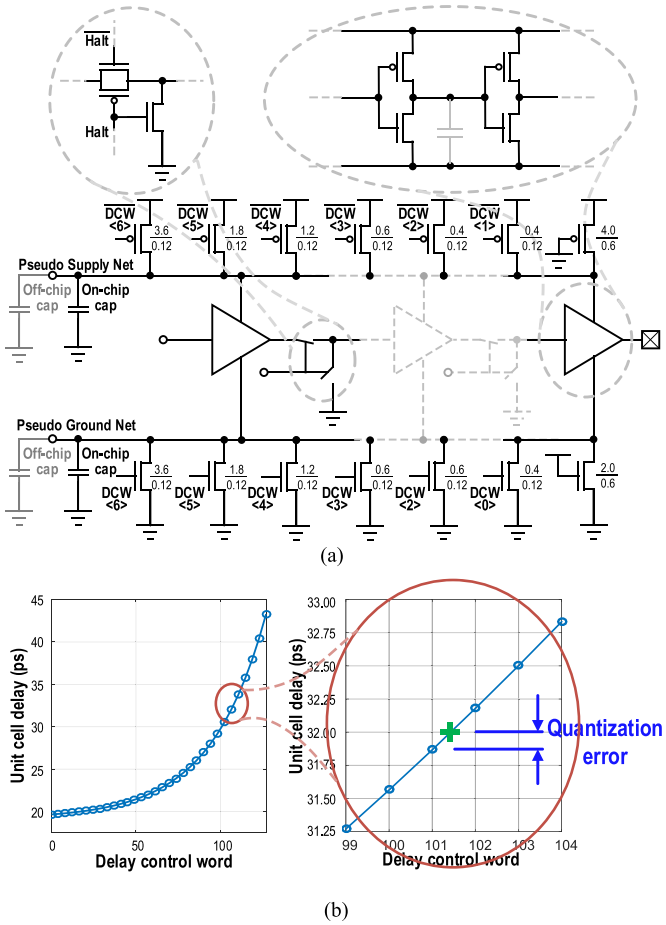

Fig. 7. Seven-bit digitally controlled tunable unit delay cell. (a) Circuit diagram. (b) Its delay tuning transfer function.

the same transistor pair. A pair of keep-life NMOS and PMOS transistors is connected in parallel with delay tuning transistors. The median value of the delay tuning range can be varied by adjusting the size ratio between keep-life transistors and the tuning transistors. Overall, each tunable delay cell is a 7-bit DTC with quantization errors due to its digitized tuning steps. Moreover, the quantization granularity is not evenly distributed due to the intrinsic nonlinearity of the MOSFETs. Indeed, the transfer curve of the delay cell follows an exponential curve approximately, as shown in Fig. 7(b). For instance, to achieve a 32-ps time delay, the closet reachable delay in the DTC is 31.9 ps as shown in Fig. 7(b). This 0.1-ps time difference introduces a 0.3% delay error that leads to an INL of more than 1.5 LSB according to simulations.

To deal with this issue, we propose to interpolate the precise delay amount by using $\Delta\Sigma$ modulation. The delay interpolation with $\Delta\Sigma$ noise shaping is illustrated in Fig. 8, where the unit delay cells can be digitally tuned to four adjacent reachable discrete delays. To obtain the desired interpolated delay of 32 ps, a 2nd-order $\Delta\Sigma$ output sequence is used to sequentially select these four delays as the timing diagram shown in the bottom of Fig. 8, where the time-average value of the temporal delay amount is 32 ps. The static delays corresponding to the four-digital delay-controlled-words (DCWs) vary among four reachable levels. Controlled by the 2nd-order $\Delta\Sigma$ modulator, the

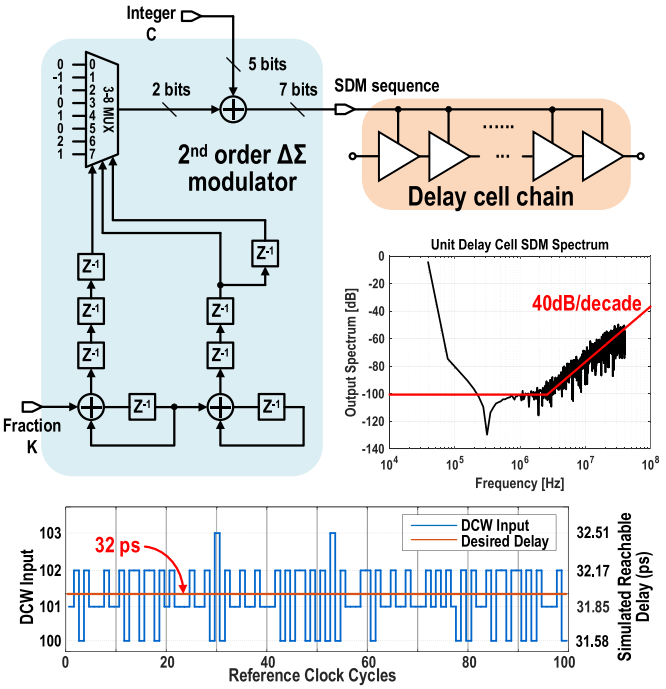

Fig. 8. Second-order $\Delta\Sigma$ modulator used for DTC delay interpolation with quantization error noise shaping.

spectrum of the delay sequence demonstrates 40 dB/dec noise shaping effect. The loading on the pseudo-supply and ground lines of the delay cell [see Fig. 7(a)] naturally provides a low-pass filter with about 2-MHz bandwidth that helps removing the shaped high frequency noise, leading to a smooth time-averaged interpolation delay value. Note that this delay tuning bandwidth is determined by the loading of pseudo-supply and ground lines and is not related to the TDC conversion bandwidth since the signal bandwidth of the delay cells are related to the inverter speed only.

The architecture of the 2nd-order $\Delta\Sigma$ modulator is also shown in Fig. 8 [30], [31]. In our case, the integer value C is set to be 101. The fractional value K is determined by the distances between two adjacent quantized delay steps as well as the accumulator size, which has 10 bits in this design. Additionally, the adjustable fractional value K is used to compensate the mismatch between the seven digital controlled switches and the nonlinearity of the DTC transfer curve in this design.

The delay chain contributes more than 80% of the total power in a Vernier TDC design. The unit delay cells use only parasitic capacitance to generate the delay and are optimized for noise, mismatch, and power consumption. In traditional Vernier TDC designs, with a short time interval inputs, the conversion completes after the signal passed just a few number of delay cells. However, signals still propagate along the delay lines until they reach the end of each line. In this design, transmission gates are used to switch OFF the signal propagation through the remaining delay cells and dump it to the ground once the comparison is completed. This adaptive power control scheme reduces the TDC power consumption by about 50% in fractional-N mode, where the input time interval

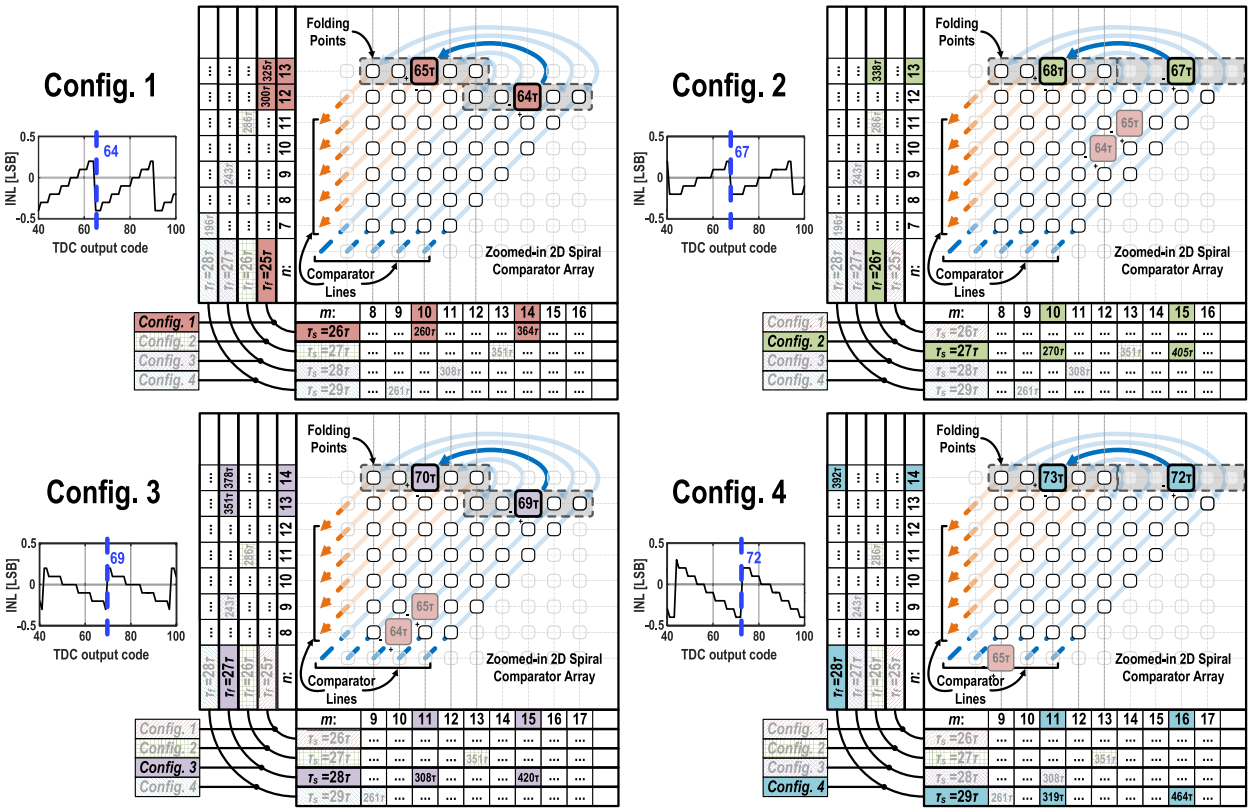

Fig. 9. Four sets of delay settings used for folding error randomization and the resultant INLs. Also shown are four sets of spiral comparator array configurations that meet the delay requirement and their corresponding folding point locations.

sweeps over the TDC detection range in one fractional cycle. As a result, the TDC average power can be estimated as 50% of the power consumed by the peak amount of delay cells. In integer-N mode, the TDC input time interval is around zero when the loop is locked, leading to a very short conversion time and a power saving for more than 90%.

B. 2-D Comparator Array Folding Error Randomization

As discussed in Section II, 2-D Vernier TDCs suffer from periodic nonlinearity due to the transition errors at the folding points between different comparator lines in a 2-D array (see Fig. 3). Even with delay calibration and the spiral comparator arrangement, the delay mismatch between the delay lines still cannot be eliminated completely. As a result, the folding errors are inevitable and periodic INL peaks at the folding locations are still present, which results in high fractional spur level at the DPLL output.

Comparator folding locations are fixed in hardware once the delay chains and comparator parameters are chosen. To reduce the nonlinearity, we propose to randomize the folding locations using multiple comparator configurations. If there are multiple sets of comparator line folding locations that can satisfy (2), we can choose different folding points in each comparison cycle, leading to a reconfigurable comparator array architecture that randomizes the mismatch errors. Fig. 9 illustrates four valid configurations of a spiral 2-D comparator array, in which "configuration 1" is the first arrangement with delay $\tau_f = 25\tau$ and $\tau_s = 26\tau$. The enlarged squares labeled with "64τ" and "65τ" indicate one of comparator line folding locations in configuration 1, where the maximum periodic error occurs. In "configurations 2, 3, and 4" with different delay settings, the "64τ" nodes are moved to different locations and the corresponding folding points in the simulated INL curves are shifted to TDC output code 67, 69, and 72, respectively, while the time resolution settings of "1τ" among all configurations are kept the same. The randomization block diagram is shown in Fig. 10(a). With the tunable delay cell and reconfigurable comparator array, only one set of hardware is required. A $\Delta\Sigma$ output sequence generated by a 2nd-order $\Delta\Sigma$ modulator preloads one of the four configuration settings to the TDC at each reference cycle and selects their corresponding output by controlling a 4-1 multiplexer. Fig. 10(b) presents four standalone TDC configurations' INL nonlinearity results as well as the result randomized with the $\Delta\Sigma$ modulations.

Delay variation increases with the length of the delay chain. A signal goes through a longer delay chain will have a larger delay variation, as illustrated in Fig. 11. Moreover, due to layout geometry, the comparison points close to the end of transfer curve, which corresponding to large input time interval, face larger delay deviation from layout mismatches and parasitics. When combined with the spiral comparator array architecture, the randomization level is automatically adapted to input signals' time interval. As shown in Fig. 11,

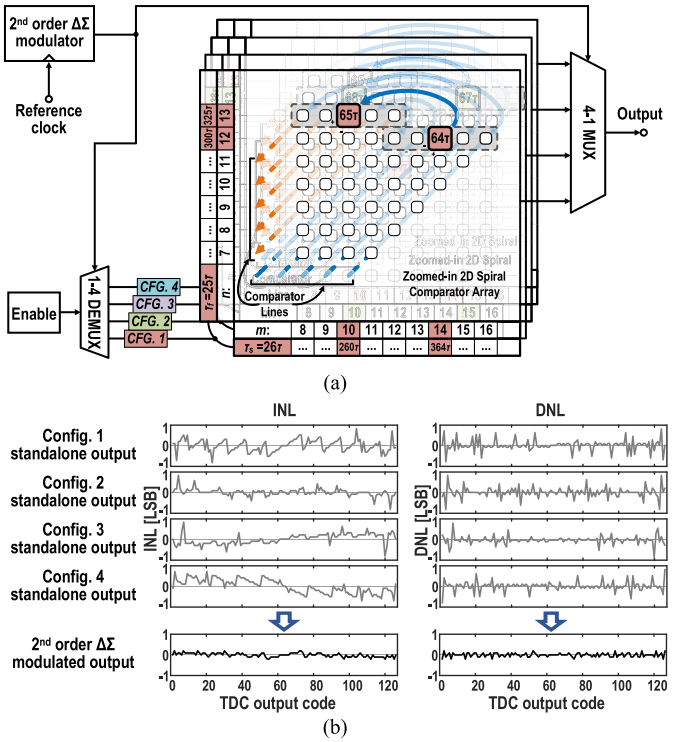

Fig. 10. (a) 2-D folding point randomization with tunable delay and reconfigurable comparator array controlled by 2nd-order $\Delta\Sigma$ modulators. (b) TDC output periodic errors for individual configurations.

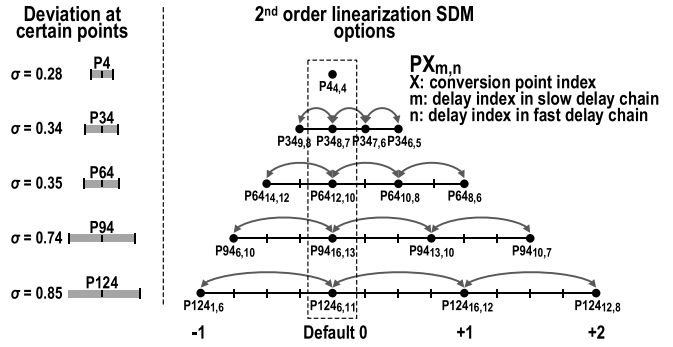

Fig. 11. Delay variations and 2nd-order $\Delta\Sigma$ randomization points.

comparison point P4 located in the first comparator line has the same location among four different configurations. In other words, it experiences no $\Delta\Sigma$ randomization effect. The other three comparison points P34, P94, and P124, all have four different locations in four configurations. The second point among the four points is selected to be the default "0" point of a 2nd $\Delta\Sigma$ output sequence. And the other three points are assigned to "−1," "+1," and "+2," correspondingly. The distance between each randomization point increases when comparison points move away from its nominal location.

The four configurations have the same resolution, namely, they have the same amount of quantization error. The difference of their nonlinearity characteristics lies upon the folding locations, namely, where the error peaks. Selecting different configurations using a $\Delta\Sigma$ modulator, the folding locations can be randomized, while the quantization noise

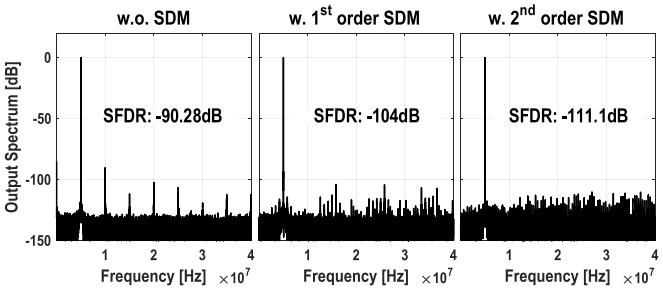

Fig. 12. Simulated TDC output spectrum without, with the 1st-order and the 2nd-order $\Delta\Sigma$ modulators for folding error randomization.

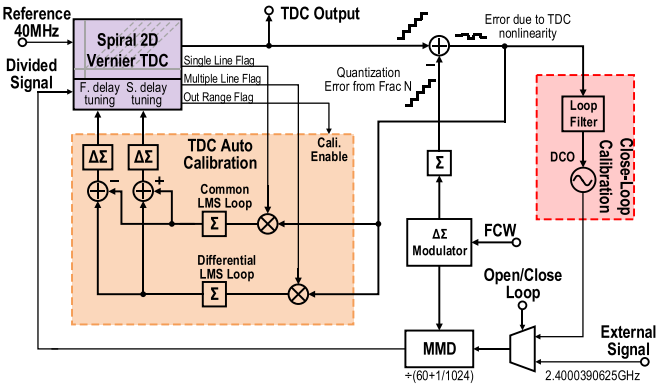

Fig. 13. Automatic 2-D Vernier TDC close-loop and open-loop delay calibrations.

remains the same. This randomization technique does not have a noise shaping effect, nor does it limit the conversion bandwidth. In the process, the spur cause by TDC nonlinearity is randomized, while its resolution is untouched. Fig. 12 gives simulated TDC output spectrum for the cases without, with the 1st-order and with the 2nd-order $\Delta\Sigma$ modulations. A 20-dB spurious-free dynamic range (SFDR) improvement is achieved with the 2nd-order $\Delta\Sigma$ modulation.

It should be pointed out that the reconfigurable structure comprises only one 2-D spiral comparator array in hardware, although four configurations are needed. Therefore, power consumption and area penalty are minimal for the proposed linearization technique. The four comparison configurations are always available in the 2-D spiral comparator array and one of the four valid configurations is selected based on the output sequence of a $\Delta\Sigma$ modulator at the beginning of each comparison cycle. The comparator array outputs are further processed by thermometer to binary encoders to produce the final TDC output.

C. TDC Delay Calibration

Prior to its normal operation, the TDC needs to go through a delay calibration. Calibration is one of the commonly used TDC linearization techniques. A close-loop automatic digital calibration technique based on least-mean-square (LMS) algorithm is developed in [28] and [32]. This paper leverages the technique with additional open-loop calibration capability for TDC stand-alone applications.

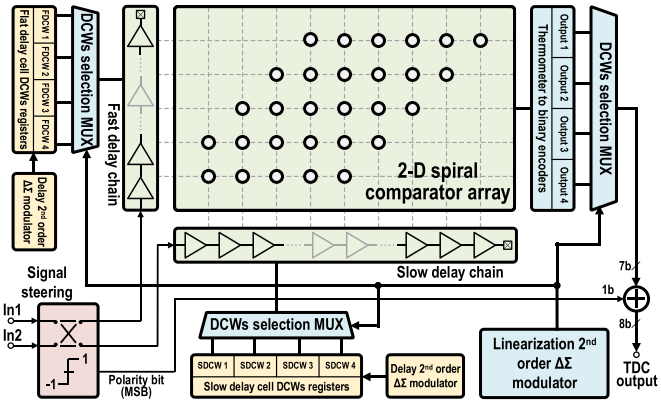

Fig. 14. Block diagram of the proposed reconfigurable 2-D spiral Vernier TDC with 2nd-order $\Delta\Sigma$ linearization.

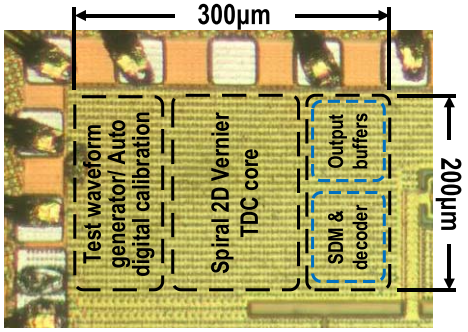

Fig. 15. Die photograph of the TDC prototype chip.

The block diagram of the TDC calibration circuit is shown in Fig. 13. The calibration is accomplished with a 40-MHz reference clock to ensure sufficient time for digital computation. The loop's output frequency is set to a certain fractional number with a minimal fractional part such as $60 + 1/1024$, shown in Fig. 13. With a small fractional number, the quantization error generated by the factional-N accumulator forms a staircase ramp waveform with fine step size that can be used to sweep the TDC input time interval over one DCO cycle. The corresponding TDC output further subtracted from the calculated ideal ramp signal, creating an error signal corresponding to TDC nonlinearity that is used to automatically adjust the TDC delays with optimization goal of minimizing this error. Two LMS loops are designed to collect the differential and common error signals used for fast and slow delay calibrations. Similarly, the open-loop calibration uses an external signal to provide a fractional frequency the same as that used in the close-loop calibration.

However, although the frequency is pulled close to the desired value, the phase error can still be unknown in an open-loop operation. A large phase error could saturate the TDC's output and fail the calibration algorithm. Thus, an out range flag is generated from the TDC to indicate whether the input phase error is out of the TDC detection range or not. This flag is used to validate the TDC input used for automatic calibration. A pair of optimized DCWs for slow delay line and fast delay is obtained during the calibration process and

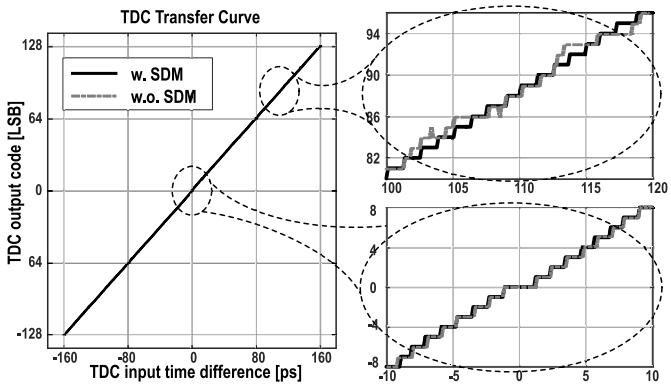

Fig. 16. Measured TDC full-range transfer curves with and without the 2nd-order $\Delta\Sigma$ modulation.

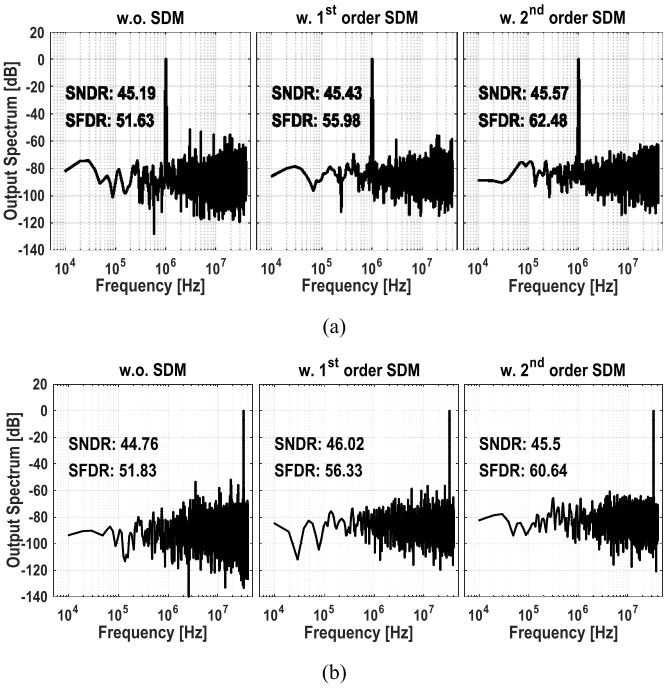

Fig. 17. Measured TDC output power spectrum density with (a) 1.01 MHz and (b) 32.7-MHz input signals under three different measurement configurations: 1) without $\Delta\Sigma$ modulation; 2) with the 1st-order $\Delta\Sigma$ modulation; and 3) with the 2nd-order $\Delta\Sigma$ modulation.

set as pair "0." And the 2nd-order $\Delta\Sigma$ modulator will select four adjacent DCWs to form the pair "-1," "1," and "2" for precise delay interpolation.

D. Proposed TDC System

Fig. 14 presents the block diagram of the proposed TDC system including the proposed spiral comparator arrangement and two $\Delta\Sigma$ modulation-based TDC linearization techniques. In summary, the 2-D spiral comparator array improves both linearity and detection range of the TDC. A $\Delta\Sigma$ modulator is employed in delay interpolation to minimize the quantization errors introduced by digitally tuned delay cells. The folding point errors commonly seen in 2-D comparator arrays are randomized by using a reconfigurable comparator array controlled by the output of another $\Delta\Sigma$ modulator.

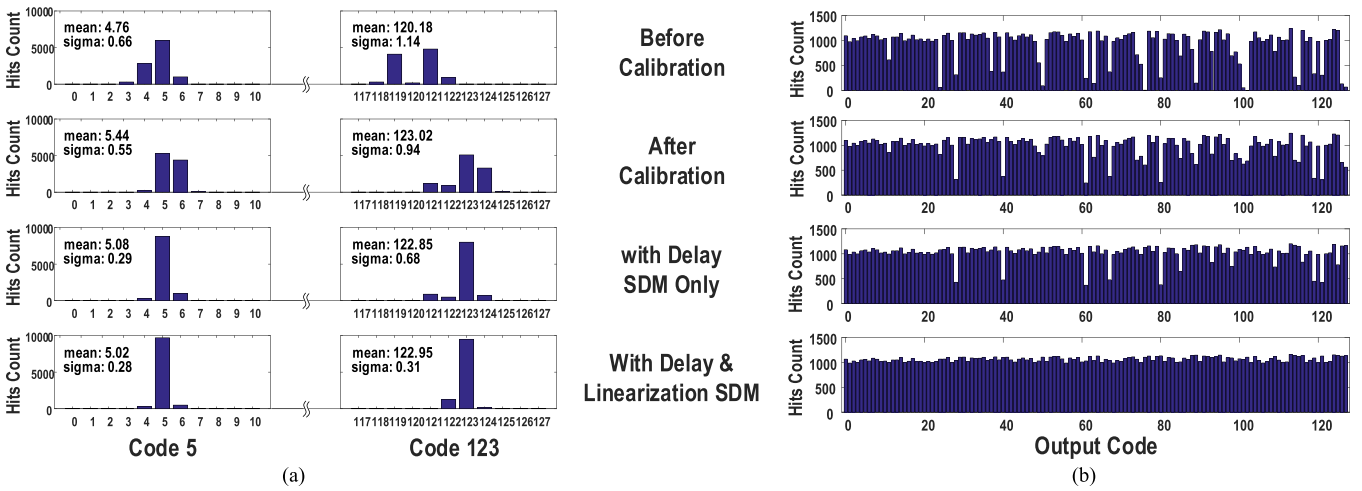

Fig. 18. (a) Single-shot precision measurement results with 10 000 tests measured for four different input time intervals located at code 5, 64, 99, and 123, respectively. (b) Measured histogram plots of TDC output codes with a ramp input signal sweeping the entire detectable range under different settings.

The 2-D spiral Vernier TDC produces seven output bits. A steering module detects lead/lag or polarity information and outputs the most significant bit, forming the 8th bit of the TDC. To ensure there is no dead-zone around the zero-crossing point, the same comparator is used in the steering module with its decision standard derivation around 0.2 ps based on Monte Carlo simulations. This decision error is smaller than the quantization error, i.e., half of LSB(0.625 ps in our design).

V. Measurement Results

The proposed TDC was fabricated in a 45-nm CMOS SOI technology. As shown in the die photograph of Fig. 15, the 2-D Vernier TDC core occupies an area of 0.03 mm^2. Other auxiliary circuits occupy another 0.03-mm^2 space. The measured full-range transfer curves of the TDC with and without the 2nd-order $\Delta\Sigma$ modulator are given in Fig. 16. The TDC covers a conversion range from -160 to 160 ps, namely, 8-bit output with a 1.25-ps resolution. Sinusoidal modulated delay signals are generated with an arbitrary waveform generator and are fed into the TDC to perform a spectrum measurement. Fig. 17 gives the measured TDC output spectrum results with inputs equal to 1.01 and 32.7 MHz under three different configurations: 1) without $\Delta\Sigma$ modulation; 2) with the 1st-order $\Delta\Sigma$ modulation; and 3) with the 2nd-order $\Delta\Sigma$ modulation. A 10-dB SFDR improvement is achieved with the 2nd-order $\Delta\Sigma$ modulation.

Measured histogram plots of the TDC output codes with a ramp input signal sweeping the entire detectable range of the TDC under different settings is presented in Fig. 18(a), illustrating the efficacy of each proposed TDC linearization techniques. Without calibration, the TDC transfer curve is extremely nonlinear with missing codes or code gaps due to the 2-D folding errors, layout mismatches, and unexpected parasitic effects. The 2-D folding error effect has been greatly reduced by automatic delay calibration and delay interpolation using $\Delta\Sigma$ modulators. The folding error residues together with layout mismatches and unexpected parasitic effects are further eliminated by the 2nd-order $\Delta\Sigma$ randomization for the folding

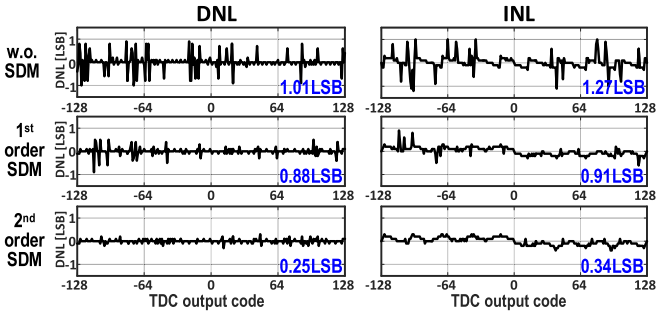

Fig. 19. Measured TDC DNL and INL without $\Delta\Sigma$ modulation, with the 1st-order $\Delta\Sigma$ modulation and with the 2nd-order $\Delta\Sigma$ modulation.

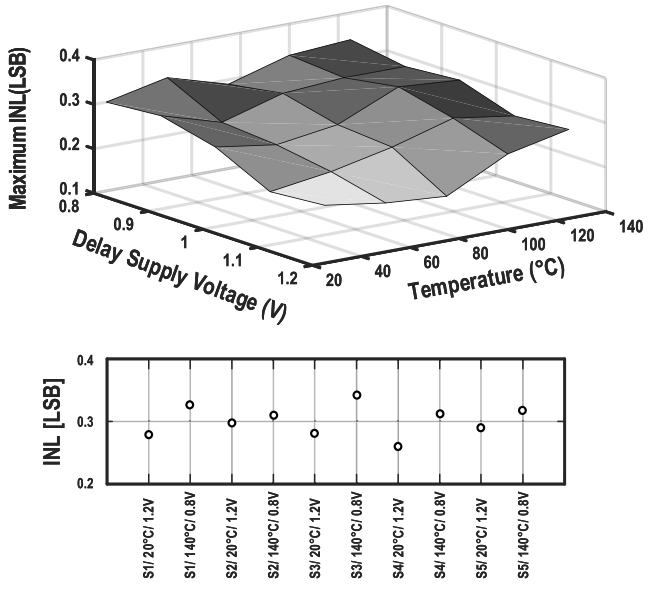

Fig. 20. Measured maximum INL results under voltage/temperature variations for five different TDC chip samples.

locations. The last histogram plot with evenly distributed code hits indicates a highly linear transfer curve. Two different time interval signals are further illustrated with single-shot precision

TABLE I
PERFORMANCE COMPARISON WITH RECENTLY REPORTED TDCS

	L. Vercesi [26] JSSC'10	J. Yu [19] JSSC'10	W. Yu [22] JSSC'15	S. Liu [33] VLSI'16	S. J. Kim [34] ISSCC'15	A. Sai [35] ISSCC'16	**This work**
Topology	2-D Vernier	Vernier ring	1-3 MASH	Parallel sampling	Stochastic	SS-ADC	**2-D Spiral Vernier**
Process	65nm	130nm	65nm	65nm	14nm	65nm	**45nm**
NoB	7	12	11	14	10	6.1	**8**
ENoB (1)	4.90	---	9.42	13.40	8.28	5.76	**7.58**
Resolution	4.8ps	8ps	2.64	6	1.17ps	6ps	**1.25ps**
ER (2)	20.58	---	7.89	8.7	3.85ps	7.60ps	**1.67ps**
Speed [MS/s]	50	15	150	1	100	40	**80**
DNL [LSB]/[ps]	0.9/4.32	---	---	0.1/0.6	0.8/0.94	---	**0.25/0.31**
INL [LSB]/[ps]	3.3/15.8	---	2.0	0.5/3	2.3/2.7	0.27/1.6	**0.34/0.4**
Power [mW]	1.7	7.5	3.52	0.28	0.78	0.36	**0.07-0.69**
Area [mm^2]	0.02	0.26	0.03	0.12	0.036	0.022	**0.04**
FoM (3)	0.266	---	0.012	0.017	0.008	0.131	**0.016**

(1) $ENoB = NoB - log_2(INL+1)$. (2) Effective Resolution (ER) = Resolution $\times 2^{(NOB-ENOB)}$.
(3) FoM = Power / ($2^{NOB} \times F_S$) [pJ / conv-step].

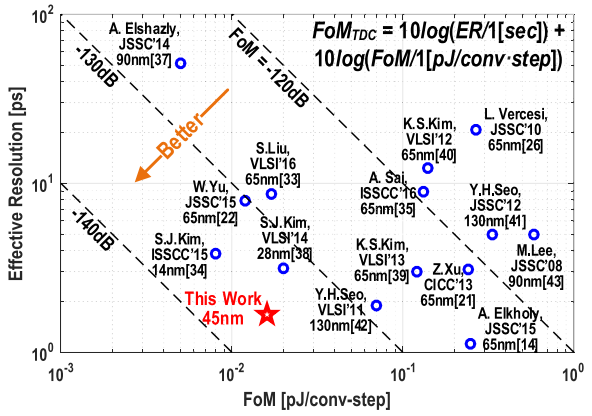

Fig. 21. Performance summary and comparison with prior-art TDC designs.

measurements, as shown in Fig. 18(b), where 10 000 tests are measured for four different input time intervals located at code 5 and 123, respectively.

For comparison, linearity performances are measured with the 2nd-order, 1st-order, and no $\Delta\Sigma$ modulations, as shown in Fig. 19. Periodic errors as large as 1.27 LSB are observed in the measured INL without $\Delta\Sigma$ modulation, showing dominant nonlinearity associated with the folding point errors of 2-D comparator array. With the 2nd-order $\Delta\Sigma$ randomization, the measured INL and DNL have much smaller errors of 0.34 and 0.25 LSB, respectively. Five different TDC chips are measured. The worst measured INL results over a temperature range from 25 °C to 125 °C and a voltage range from 0.8 to 1.2 V are presented in Fig. 20, demonstrating the robustness of the TDC linearity performance against PVT variations with the proposed linearization techniques.

This proposed 2-D spiral Vernier TDC is designed to cover 8 bits with a resolution of 1.25 ps. Taking the nonlinearity performance into consideration, the effective number of bits is 7.58 bits and the effective resolution is 1.67 ps. In the measurement, the TDC consumes 0.3 mW under a conversion rate of 80 MS/s and a 1-V power supply when the TDC input is fed with a staircase sweeping ramp signal similar to a fractional-N mode operation. It consumes 0.7 mW if every cycle of the input phase difference exceeds the TDC's full range, and consumes less than 0.1 mW when dealing with small input time interval, for instance, in an integer-N mode operation in a DPLL. Performance summary and comparison with prior-art TDC designs are listed in Table I. Figure of merit (FoM) is based on a well-accepted data converter FoM evaluation criterion that takes the power consumption, detectable range, and conversion rate into consideration [36]. For TDC designs, effective resolution is an important factor that directly impacts DPLL's performance. Considering both effective resolution and FoM, we summarized the performances of recently reported state-of-the-art TDC designs [37]–[43] and presented the comparison in Fig. 21; demonstrating a very competitive TDC design among the state of the art with excellent linearity performance. The presented TDC design provides precise time measurement and digitization of timing information up to 1.25-ps resolution, which supports a wide variety of applications, including DPLL, direct digital modulator, time-based communication transceivers, [44], [45], and millimeter-wave imaging radars [45], [46].

VI. CONCLUSION

A low power 8-bit 2-D spiral Vernier TDC with 1.25-ps temporal resolution is presented in this paper. A spiral comparator array is proposed to enlarge the TDC detection range and improve the linearity. Two 2nd-order $\Delta\Sigma$ modulators are utilized to lower the quantization errors of the DTC-based unit delay cells and to randomize the periodic folding errors of the 2-D comparator array. With an 80-MHz reference clock, the measured maximum DNL and INL of the proposed TDC are 0.25 and 0.34 LSB, respectively. With the adaptive power control that switches OFF unused delay cells, the TDC power consumption is greatly reduced. Fabricated in 45-nm CMOS technology, the TDC prototype consumes 70–690 μ W under a 1-V power supply at a conversion rate of 80 MHz. It achieves

1.67-ps effective resolution and an FoM_{ADC} of 0.016 pJ/conv step, advancing the state-of-the-art high-performance TDC designs.

ACKNOWLEDGMENT

The authors would like to thank GlobalFoundries, Santa Clara, CA, USA, for IC fabrication support.

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