A Multi-Phase Coupled Oscillator Using Inductive Resonant Coupling and Modified Dual-Tank Techniques

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Abstract—This paper presents a novel coupled oscillator RFIC for multi-phase clock generation. The design achieves low phase noise while maintaining strong coupling among oscillator cores. The proposed transformer-based dual-tank topology forms a loop of coupling path for enhanced multi-phase coupling. To facilitate strong magnetic coupling among oscillator cores, the proposed transformers utilize resonant inductive coupling to enhance the voltage swing at the coupled wing. The phase noise optimization is accomplished by leveraging the adaptive biasing feedback and the enhanced dual-tank technique. The behavioral model based on Alder's equation as well as the analysis of the tank response is given. Full electromagnetic (EM) modeling involving all transformers and the passive interconnecting routes has been performed using the EMX software in order to ensure that simulated performance reflects measurement environment. The prototype RFIC of the proposed circuit with eight phases is implemented in a 65-nm CMOS radio frequency (RF) silicon on insulator technology. The measured phase noise is -124.3 dBc/Hz at 1-MHz offset from 2.41 GHz with 7-mW power consumption per core, and the operating frequency can be digitally tuned from 1.81 to 2.41 GHz. The phase noise can be further improved to -128.2 dBc/Hz at 1-MHz offset from 2.41 GHz by increasing the power consumption to 15 mW per core.

Index Terms— Coupled oscillator, dual-tank technique, impulse sensitivity function (ISF), multi-phase generation, transformer.

I. INTRODUCTION

MULTI-PHASE clock generation has gained popularity due to its widespread applications in numerous critical radio frequency (RF) blocks such as the N-path filter, the sub-harmonic mixer, the interleaved analog-to-digital converter (ADC), and the clock and data recovery (CDR) circuit. Instead of creating four phases using a common quadrature oscillator topology, an oscillator architecture that can generate more than eight phases with good performance is highly desired. Current approaches to multi-phase clock generation such as the ring oscillator, the poly-phase filter,

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and the frequency divider are ruled out as a viable candidate due to their following set of problems: poor phase noise of the ring oscillator, narrow bandwidth of the poly-phase filter, and the need for a high-frequency source for the frequency divider. The coupled-oscillator topology as the best candidate for multi-phase clock generation has been investigated and enhanced over the past decade due to its two intrinsic advantages: 1) the number of phases can be easily expanded by adding an extra oscillator core to the loop [1] and 2) the phase noise, regardless of the degradation caused by the coupling technique, can be improved theoretically by a factor of $10 \log_{10} N$ [2], [3], where N is the number of coupled oscillator cores. That is, as the number of oscillator cores increases, the phase noise can be further reduced.

Most publications have focused on two major types of coupling strategies: 1) active coupling and 2) passive coupling, which includes capacitive and magnetic coupling. The conventional active coupling utilizes additional transistors for coupling; therefore, it suffers from extra noise and increased power consumption introduced by these active devices [4]. The most recent active coupling techniques such as back-gate coupling [5] and bulk injection coupling [6] can partially solve the problems; however, they still suffer from either the weak coupling strength or the poor phase noise. The capacitive coupling, on the other hand, uses additional capacitors for coupling, and can couple the oscillator cores with less noise degradation and less power consumption penalty [7]. However, an ultra-high coupling strength often results in degraded phase noise and decreased oscillation frequency, because additional large capacitors are required. Ultimately, the magnetic coupling is realized using a transformer, which is a part of the oscillator circuit, and thus, does not need an additional die area. However, most of the transformer-based coupling techniques [8], [9], which can achieve good phase noise or strong coupling, are not able to expand to higher number of cores due to the limitations in their topologies and floor plans. In addition, the design of the transformer-based coupling requires a careful electromagnetic (EM) modeling in order to ensure close correlation between simulation and measurement. Moreover, compared to the active and capacitive couplings, another advantage of the transformer-based magnetic coupling is that the coupling path is embedded in the transformer itself; unlike the other two coupling mechanisms, where coupling-related routing is required among oscillator cores. These routings will increase

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Fig. 1. Proposed multi-phase coupled-oscillator topology and its unit oscillator core.

implementation challenges as the number of oscillator cores increases, because a symmetric layout is necessary to ensure an equal coupling strength and identical interconnecting routes among cores.

To properly utilize the advantages of the magnetic coupling technique, and achieve its promising performance, this paper presents a novel magnetic coupling topology with adaptive biasing feedback [10] and resonant inductive-coupling techniques [11], which convert the conventional dual-tank oscillator structure to the one based on the transformer so that both the strong coupling strength and the optimization of phase noise can be achieved simultaneously. Furthermore, the proposed transformer-based oscillator topology facilitates a symmetric floor plan. In addition, using the EM modeling tool, all passive routing is carefully laid out in order to minimize undesired coupling. In Section II, the general idea of the proposed architecture, including the schematic, and the theoretical and behavioral models, will be introduced. In addition, a brief discussion on the coupled-oscillator system will be provided. In Section III, the circuit design details will be introduced; especially, for the transformer and the passive routing. The measured results will be presented in Section IV, and the conclusion will be drawn in Section V.

II. PROPOSED TRANSFORMER-BASED OSCILLATOR ARCHITECTURE

A. Unit Oscillator Core

As shown in Fig. 1, the proposed unit oscillator core adopts the dual-tank and the adaptive biasing feedback techniques, where *j* is the sequence number of the oscillator core. L_1 and L_2 are differential inductors, and, together with C_1 and C_2 , form the dual-tank structure. Unlike the conventional single-NMOS transistor current tail, two separate NMOS transistors (i.e., M₃ and M₄) provide the bias current, and facilitate the implementation of the feedback in the proposed oscillator. C_F and R_b provide the feedback path for adaptive biasing, which passes the ac voltage from the output to the gates of M₃/M₄. C_t represents the 3-bit digitally controlled capacitor array for frequency tuning. The transformer is composed of coil L_1 of the previous adjacent core and coil L_2 of the next core; therefore, the output signal of the previous adjacent core couples to the gates of the cross-coupled transistors of the next oscillator core, and so on.

B. Resonant Inductive Coupling Mechanism

The complete schematic of the proposed eight-phase oscillator is shown in Fig. 2, where the dashed lines represent the coupling paths among transformers. Unlike the other transformer-based structures [12], signal is drawn from the drain of the cross-coupled transistors and coupled to the gate of the same transistors in the adjacent core; forming the closedloop coupling path. This way, the voltage at the gate of the cross-coupled transistor is the superposition of two voltages: 1) the one coming from the output of the same core and 2) that originating from the output of the adjacent core.

Fig. 3 illustrates the signal flow in the simplified circuit, where V_{g+} is the gate voltage, and only one side of the crosscoupled network is shown. $V_{g+,1}$ is that part of the gate voltage that comes from the output of the same core, and its major role is to provide g_m to support the oscillation. $V_{g+,2}$ is the other part of the gate voltage that comes from the output of the adjacent core, and contributes to both coupling and oscillation. Assuming that the output sources $V_{\text{IP},1}$ and $V_{\text{IP},2}$ are independent, and the behavior of the transformer is conventional, the ratio of the voltage of the secondary coil over that of the primary coil is approximately equal to $V_2/V_1 = k\sqrt{L_2/L_1}$, and the two parts of the gate voltage can be separated and expressed as follows:

$$V_{g+,1} = V_{\rm IP,2} \times s^2 L_2 / (2 + s^2 L_2 C_2) \tag{1}$$

$$V_{g+,2} = V_{\text{IP},1} \times k \sqrt{L_2/L_1}$$
 (2)

where k is the coupling factor of the transformer. The proposed structure is different from the conventional dual-tank configuration, where the ratio of L_2/L_1 is small and the ratio of the gate voltage of the cross-coupled transistor over the drain voltage is large. In order to ensure strong coupling, the ratio of L_2/L_1 must be sufficiently large in the proposed architecture, since the coupling strength, *m*, is equal to

$$m = s^{2}k(2 + s^{2}L_{2}C_{2})/\sqrt{L_{2}L_{1}} \approx k\sqrt{L_{2}}/L_{1}.$$
 (3)

However, if the coupling factor k and the ratio L_2/L_1 are not large enough, limited voltage ratio V_2/V_1 can be achieved. For example, in Fig. 4(a) case 1, we are assuming that no additional capacitance is added to the coupled coil, and C_2 is the parasitic capacitance of L_2 . In this case, and as shown in Fig. 4(b), where L'_2 is the equivalent inductance of C_2 and L_2 , for k equal to 0.6, the voltage ratio V_2/V_1 is only 0.79, which is smaller than 1. As a result, it is inadequate to achieve a strong coupling and signal strength. Moreover, we cannot increase the voltage ratio and the coupling factor k arbitrarily, since it will require a larger die size and result in increased parasitic components. To address this issue with minor changes and the least penalty, the resonant inductivecoupling technique is introduced by adding an additional capacitance to the coupled coil. As shown in Fig. 4(c), the selfresonant frequency is pushed down toward the oscillation frequency of the tank by increasing the value of C_2 , and the voltage ratio V_2/V_1 is thus boosted to 1.61, as can be verified



Fig. 2. Schematic of the proposed eight-phase oscillator.



Fig. 3. Simplified equivalent model of coupling paths.

by viewing the ratio of the peak value of the gate voltage over that of the drain at about 2.5 GHz.

To explain this phenomenon, we have drawn the equivalent circuit in Fig. 5, where *M* is the mutual inductance and is equal to $M = k\sqrt{L_1L_2}$. As a result, the voltage ratio V_2/V_1 is equal to

$$V_2/V_1 = \frac{Z_1}{j\omega L_1 + Z_1} \frac{1}{j\omega C_2 Z_2}$$
(4)

where $Z_1 = j\omega M ||Z_2$ and $Z_2 = j\omega L_2 + (1/j\omega C_2)$. Equation (4) is plotted in Fig. 6, where it is clear that the voltage ratio V_2/V_1 can exceed 1 only when C_2 is larger than 1.25 pF.

In the resonant inductive coupling, the gate voltage V_{g+} is dominated by $V_{g+,1}$, i.e., the contribution from the coupled source, as shown in Fig. 7, and V_{g+} is almost in phase with $V_{g+,1}$. Therefore, the coupling strength *m* in (3) can be re-written as follows:

$$m = \frac{Z_1}{j\omega L_1 + Z_1} \frac{1}{j\omega C_2 Z_2} \Big/ \sqrt{L_2 L_1} \approx \frac{Z_1}{j\omega L_1 + Z_1} \frac{1}{j\omega C_2 Z_2}$$
(5)

which demonstrates the relationship between the coupling factor and the coupling strength, as shown in Fig. 8.



Fig. 4. Simulated tank response for two different cases. (a) Simplified circuit. (b) Tank with the conventional transformer coupling (case 1). (c) Tank with resonant transformer coupling (case 2).

As mentioned, implementing the resonant inductivecoupling technique in the proposed oscillator structure does not require an additional component, and is achieved by simply increasing the value of C_2 ; therefore, it facilitates the optimization of the performance, as will be discussed shortly.

C. Transformer-Based Dual-Tank Technique

As discussed in [13] and [14], the conventional dual-tank architecture allows different voltage swings at the gate and the drain of the cross-coupled transistors. As a result, the voltage



Fig. 5. Simplified equivalent model of coupling paths.



Fig. 6. Plot of voltage ratio versus frequency for different values of C_2 .



Fig. 7. Simulated plot of gate and output voltages.

at the drain could be reduced while maintaining the same voltage at the gate in order to minimize the operation time in the triode region and prevent Q degradation of the tank. This concept is illustrated in Fig. 9(a), where the dashed line represents the triode region trigger, and the transistor is in the triode region if the drain voltage is below this line. However, since the objective is to achieve a strong coupling strength in the proposed transformer-based structure, the original functionality is no longer preserved within the single oscillator core. In other words, as we intentionally increase the value of C_2 , the impedance of $L_2/2$ dominates that of C_2 , and the gate voltage $V_{g+,1}$, contributed by its own core, is approximately equal to its output voltage $V_{IP,2}$.

Fortunately, the proposed structure continues to benefit from the advantages of the dual-tank technique; however, through the coupling path. By using the resonant inductive coupling method, we are still able to reduce the voltage swing at the drain while increasing the voltage swing at the gate, and, consequently, reduce the operation time in the triode region. It is worth noting that since the peak of the gate



Fig. 8. Plot of coupling strength versus coupling factor.



Fig. 9. Illustration of voltage swings of (a) conventional dual-tank, (b) transformer-based dual-tank, and (c) transformer-based dual-tank with gate voltage decomposed.

voltage is no longer aligned with that of the drain voltage, as shown in Fig. 9(b), there exist both in-phase and quadrature components at the output. In addition, as the voltage swing of the gate increases relative to that of the drain, the phase noise will potentially degrade, if the signal strength of the quadrature component increases and significantly surpasses that of the output.

D. Phase Noise Reduction Mechanism

In the proposed structure, and as shown in Fig. 1, the phase noise is optimized using two techniques: 1) adaptive biasing



Fig. 10. Simulated phase noise and ac gain versus coupling factor k.

and 2) transformer-based dual-tank techniques. The first technique is implemented by feeding back the signal from the gate of $M_{1/2}$ to the gate of $M_{3/4}$. Since $M_{3/4}$ adjust their currents to follow the output signal, $M_{1/2}$ will be forced to switch faster, and spend less time in the equilibrium region, where noise degradation is the maximum. Therefore, the adaptive biasing feedback increases the bias current when it is needed in order to expedite the transition and suppress the noise. In addition, by using two transistors for biasing, the second harmonic, which is present in the common node of the structure biased with a single transistor, is eliminated, and the flicker noise is significantly suppressed.

The conventional dual-tank structure optimizes the phase noise by increasing the voltage swing at the gate and thus reducing the operation time in the triode region, where the output impedance of the cross-coupled transistors is the smallest, and the Q of the load is degraded. A similar optimization can be performed in the proposed transformerbased architecture, but in a much different manner. One major functional difference between the transformer-based and the conventional dual-tank oscillator is that the former affects both the coupling strength and the voltage swing at the gates of the cross-coupled transistors at the same time. Therefore, the tradeoff between the phase noise and the coupling strength does not follow the same convention as most coupled oscillators, where decreasing the coupling strength always leads to a better phase noise. In order to illustrate this matter clearly, the simulated phase noise versus coupling factor k of the transformer is shown in Fig. 10, where constant current is maintained for different k values. It is worth noting that the simulated coupling strength m in Fig. 10 demonstrates the same trend as the calculated coupling strength m in Fig. 8. As the coupling factor increases from 0.35 to 0.5, the coupling strength increases, as well, and the phase noise improves. That is because when k is relatively small, and the voltage swing of the drain is even larger than that of the gate, the phase noise still benefits from the reduced operation time in the triode region. By further increasing the coupling factor, the phase noise starts to degrade due to the injection of the coupled signal to the zero-crossing point of the oscillation waveform, which is also the case in most prior-art coupled oscillators. This is illustrated in Fig. 9(c), where the signal coupled from another core can be decomposed into two components:



Fig. 11. Simplified equivalent circuit model of the coupling paths.

one contributing to oscillation and the other responsible for coupling. Therefore, as the voltage swing of the output is reduced, the zero-crossing point becomes more sensitive to the quadrature component of the coupled signal.

E. Equivalent System-Level Model

To conduct a system-level analysis of the phase noise and the phase error performance, the equivalent model of the proposed coupled oscillator is shown in Fig. 11, where only one side of the differential structure is illustrated to facilitate the analysis. $I_{\text{tot},j}$ represents the sum of the self-resonant current I_j from the current tank, and the coupled current $I_{c,j}$ from the adjacent tank. Using the generalized Alder's equation [15], [16], the phase noise can be expressed as follows:

$$L(\omega_m) = \frac{KTR}{2V^2} F\left(\frac{\omega_0}{Q\omega_m}\right)^2 \tag{6}$$

where Q is the quality factor of the tank, R is the equivalent parallel resistor with the tank, K is Boltzmann's constant, Tis the absolute temperature, and ω_m is the offset frequency. For a four-core coupled oscillator, the minimum noise factor may be derived as follows:

$$F_{\min} = 1 + \left(\frac{m\sin(\pi/4)}{1 + m\cos(\pi/4)}\right)^{2} + \gamma \left[\frac{1}{1 + m\cos(\pi/4)} \left(1 + m\left(\frac{\cos(\pi/4) + m}{1 + m\cos(\pi/4)}\right)^{2}\right)\right]$$
(7)

where γ is the noise coefficient of the transistor. It is worth noting that the quality factor Q in (6) can be treated as a constant in most conventional oscillator structures, whereas it is a function of the coupling strength m in the proposed structure, because the output impedance is determined by m, and directly loads the tank. Therefore, in order for the equation to represent the proposed architecture better, the relationship between Q and m is estimated by curve fitting the simulated data. In Fig. 12, the simulated Q is captured for different values of coupling strength by sweeping the drain voltage while keeping the gate voltage of the cross-coupled transistors constant. The sixth-order polynomial is used to fit the



Fig. 12. Simulated and curve-fit Q-factor versus coupling strength.

 TABLE I

 COEFFICIENTS FOR SIXTH-ORDER POLYNOMIAL* OF Q-FACTOR



Fig. 13. Plot of phase noise versus coupling strength with constant and curve-fit Q-factor value.

simulated data, and its coefficients are listed in Table I. By applying curve fitting to (6), the phase noise versus coupling strength m is plotted in Fig. 13. In fact, the equation-based data in Fig. 13 show the same trend as the simulated data in Fig. 10, where the minimum phase noise is achieved when coupling strength is approximately 1.5. In addition, Fig. 13 confirms that unlike the conventional structure, where the phase noise degrades as the coupling strength increases, in the proposed topology, good phase noise and strong coupling can be achieved simultaneously.

As far as the phase accuracy is concerned, the expression for phase deviation caused by the tank mismatch can be obtained as follows using Alder's equation:

$$\Delta \varphi = \frac{Q}{2} \frac{(1 + m \cos(\pi/4))^2 + \frac{m}{2Q} (2 \sin(\pi/4) + m)}{m(m + \cos(\pi/4))} \frac{\Delta \omega}{\omega_0} \quad (8)$$

where $\Delta \omega$ is the difference in frequency caused by the mismatch. Similar to the case of phase noise, Q in (8) has been replaced by the fit data, and the phase deviation is plotted in Fig. 14.



Fig. 14. Plot of phase deviation versus coupling strength with constant and curve-fit Q-factor value.



Fig. 15. Plot of phase noise and phase deviation versus additional phase shift on the coupling path in a four-core coupled system.

The proposed oscillator architecture is unlike the conventional structure; in that the phase deviation is small when the coupling strength is small, and as the coupling strength increases, the phase deviation increases first before it decreases. The reason for this behavior is that the Q in the proposed topology has a small starting value, which recovers quickly as the coupling strength increases. When the Qis small, the impedance and the phase of the tank are more flat over frequency; therefore, they are more robust to mismatch. In other words, a coupled signal with certain phase would cause less phase variation in the tank with lower Q. Therefore, there is a tradeoff between phase deviation and phase noise.

In addition, previous publications have stated that the phase shift would help improve both the phase noise and the phase accuracy; especially, for the case of the quadrature oscillator, where there are two oscillator cores in the system [17], [18]. However, this does not apply to our proposed architecture, where there are four cores in the system. By inserting the phase shift in the equation and plotting the phase noise and the phase deviation in Fig. 15, we observe that very limited improvement is achieved in the four-core oscillator as a result of adding an extra phase shift. That is because in the quadrature case, the phase difference between the coupled signal and the local signal is 90°, which is the worst case scenario for both the phase noise and the phase accuracy, and the phase shift benefit will be obtained for the first 45° of shift. However,



Fig. 16. Simulated plot of voltage ratio and FoM versus different values of capacitance in the tank.



Fig. 17. Simulated ISF functions.



Fig. 18. (a) 3-D view of the transformer. (b) 3-D view of the transformers and the passive routing.

in the proposed architecture, the phase difference between the coupled signal and the local signal is 45° , which can be approximately treated as the quadrature case with 45° phase shift on the coupling path. Moreover, the phase shifter is not noise free, and will introduce an extra mismatch to the system; therefore, it is not worth adding an extra phase shift to the proposed system.



Fig. 19. Simulated plots of the transformer performance.



Fig. 20. Simulated phase error versus inductor mismatch.



Fig. 21. Impact of the leakage between adjacent transformers. (a) Output waveforms when coupling factor between adjacent transformers is equal to 0.1. (b) Phase noise versus coupling factor k of adjacent transformers.

III. DESIGN DETAILS

A. Design Methodologies

To properly graft the resonant inductive-coupling technique to the proposed structure, both C_1 and C_2 were swept in order to verify the potential performance, as shown in Fig. 16 and



Fig. 22. Simulated coupling factors between adjacent inductors.



Fig. 23. Simulated output waveforms.

TABLE IIParameters for Fig. 16

C ₁ (F)	$C_2(F)$	Frequency(GHz)
802f	902f	4.835 ^a
1p	834f	2.467
1.2p	789f	2.44
1.6p	509f	2.47
2p	340f	2.439
1.6p 2p	340f	2.47

^a Undesired oscillation mode

Table II. Also, the following equations are used to evaluate the figure of merit (FoM) and FoM_{per phase}:

FoM =
$$10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1\text{mW}}{P}\right] - \mathcal{L}(\Delta f)$$
 (9)

FoM_{Per phase} = 10log
$$\left[\left(\frac{f_0}{\Delta f} \right)^2 \frac{1 \text{mW}}{P} N \right] - L(\Delta f).$$
 (10)

 C_2 plays a major role in determining the enhanced voltage ratio, and C_1 is modified accordingly in order to keep the oscillation frequency constant. In addition, the capacitor values and the corresponding oscillation frequencies are listed in Table II. As C_2 increases, the voltage ratio increases; however, the phase noise decreases. This indicates that the voltage ratio is over saturated, which is similar to the case when the coupling factor k is too large, and the quadrature component is strong. In addition, if we do not increase C_2 carefully, the oscillator might jump to the undesired mode of operation, where the operating frequency is almost doubled. In this mode, the functionality of the dual-tank technique totally collapses, and the voltage ratio is close to 1; therefore, the FoM is largely degraded. On the other hand, if C_2 is too



Fig. 24. Simulated phase error versus frequency.



Fig. 25. EM simulation results of the coupling path. (a) Inductance and Q-factor of the routing between the transformer and the active cell. (b) Phase shift versus frequency of the entire coupling path (including transformer and the routing).

small, it is hard to achieve a strong coupling strength, and the reliability and the startup condition become an issue.

Moreover, the optimization of the phase noise can be verified by examining the impulse sensitivity function (ISF), as shown in Fig. 17, where the magnitude of the ISF of the proposed structure is significantly reduced compared to the conventional structure, and the effective ISF, which is the product of ISF and noise modulation function, is close to zero nearly three quarters of the time in an operation cycle.

B. Transformer and Passive Design

In order to obtain a strong coupling factor k, a transformer with interleaved turns is used, as shown in Fig. 18(a). Also, the coils of the transformer are made by stacking the top two metals in order to minimize the dc resistance and achieve the best possible quality factor. Simulated plots of the transformer performance are shown in Fig. 19, where L_1 and L_2 are 2.5 and 7.4 nH, respectively, at 2.4 GHz.

Since the resonant inductive-coupling technique is adopted in the proposed oscillator architecture, it is interesting to examine how a mismatch introduced to each coil will affect the phase accuracy of the system. As shown in Fig. 20, it is



Fig. 26. Die photograph of the proposed multi-phase coupled-oscillator RFIC.



Fig. 27. Measured phase noise. (a) Total power consumption is 28 mW. (b) Total power consumption is 60 mW.

expected that as the percentage of the mismatch increases, the phase error will also increase. In addition, since the oscillation frequency in the proposed architecture is mainly dominated by L_2 , the phase error is more sensitive to the mismatch in L_2 .

Furthermore, in order to capture the capacitive and magnetic coupling among all critical routings in the layout, the EM model is created using EMX CAD tool from Integrand Software, Inc. As shown in Fig. 18(b), the 37-port EM model includes the transformers, the routing among all oscillator cores, the routing of control signals, the power supply, and ground traces. Therefore, undesired coupling among routings can be avoided during the layout design. It is worth noting that the magnetic leakage among transformers will cause degradation in both the phase accuracy and the phase noise. As shown in Fig. 21(a), where the coupling factor k between adjacent transformers is equal to 0.1, the phase relationship totally collapses. Also, in the phase noise versus coupling factor k of Fig. 21(b), the phase noise increases as the magnetic leakage increases. Due to these observations, the coupling factor k among transformers is designed to be minimum, as shown in Fig. 22, where the coupling factor k between



Fig. 28. Measured phase noise at 1-MHz offset versus the operating frequencies under different dc bias voltages and currents.



Fig. 29. Measured spectral plots of the four outputs.

adjacent inductors is far less than 0.01. In addition, all control signals are routed using the lowest metal layer in order to minimize their interaction with signal paths. It is worth noting that as a result of careful EM modeling, the oscillation frequency is accurately predicted; e.g., the difference between the simulated and the measured frequency is only 80 MHz. Moreover, using the full EM modeling of all passive structures in the layout, the simulated output waveforms that encompass all couplings among proposed oscillator cores are illustrated in Fig. 23, where four phases, out of eight phases, of the fourcore oscillator are shown, and the other four phases are the differential counterparts and not shown. The phase difference between adjacent waveforms is 41°, 45°, and 47°, respectively. In addition, the phase error versus frequency between the first two phases is shown in Fig. 24. Since the mismatches caused by the coupling and routings are fixed, it is expected that the phase error will decrease as the frequency decreases.

In addition to the coupling paths among transformers, there are also a few routings between the transformers and the active cores. These routings are designed to be as short as possible in order to minimize their impact on circuit performance. For example, as shown in Fig. 25(a), only a few hundred pH of inductance is introduced to the load. Furthermore, the simulated phase shift versus frequency for the entire coupling path is shown in Fig. 25(b), where only a few degrees of phase shift is introduced over a wide frequency range, as

TABLE III TABLE OF COMPARISON

	Performance Metrics							
Ref.	Process	Freq. (GHz)	P.N (dBc/Hz) @ 1MHz	Power (mW)	ГоМ	No. of Phases	FoM Per Phase	
This work	65nm CMOS	2.41	-120.1	14	176.3	8	185.3	
			-124.3	28	177.5	8	186.6	
			-128.2	60	178	8	187	
[4]	65nm	4.07	-136	126	188	2	191	
	CMOS							
[19]	65nm	3.8	-123.7	7	185	4	191	
	CMOS							
[5]	0.18µm	1.1	-128	20	180.1	4	186.1	
	CMOS							
[20]	0.13µm	4.9	-112	3.2	180.8	4	186.8	
	CMOS							



Fig. 30. Measured multi-phase output waveforms.

discussed in Fig. 15; as such, the impact of the coupling paths on the performance is negligible.

IV. MEASUREMENT

The prototype eight-phase magnetically coupled oscillator is fabricated in a 65-nm CMOS RF silicon on insulator process. The die photograph is shown in Fig. 26. The core area of the proposed coupled oscillator circuit is 1.4×1.4 mm². In order to make the connections among oscillator cores more symmetric, a circular floor plan is adopted by taking advantage of the transformers. Table III summarizes the performance of this paper and provides comparison with the state-ofthe-art multi-phase oscillator designs. The phase noise is measured using an Agilent E4440 spectrum analyzer with phase noise option. Fig. 27 illustrates the measured phase noise of -124.3 and -128.2 dBc/Hz at 1-MHz offset from 2.41 GHz with power consumption of 28 and 60 mW, respectively. Since a 3-bit capacitor array is implemented for frequency tuning, the operating frequency can be digitally tuned from 1.815 to 2.42 GHz. In addition, measured phase noise versus the operating frequency is shown in Fig. 28 under three different dc operating conditions for each core: 1) V = 0.7 Vand I = 5 mA; 2) V = 1 V and I = 7 mA; and 3) V = 1.5 V and I = 10 mA.

In addition, Fig. 29 shows the spectral plot of the four measured outputs, out of eight outputs, of the four-core oscillator, where the other four outputs are the differential counterparts and not shown. Fig. 30 exhibits four measured phases, which are captured by a Rohde & Schwarz RTO oscilloscope, which supports simultaneous measurement of four channels.

V. CONCLUSION

This paper presented a novel transformer-coupled VCO architecture for multi-phase clock generation. The concept of the prototype circuit is proven by both simulation and measurement. EM modeling was utilized to ensure proper coupling among oscillator cores; thus, improving the correlation between simulation and measurement. The highest measured FoM is 187 dBc/Hz with phase noise of -128.2 dBc/Hz at 1-MHz offset from the 2.4 GHz, and the frequency range can be digitally tuned from 1.815 to 2.41 GHz with eight steps.

REFERENCES

- F. Zhao and F. F. Dai, "A capacitive-coupling technique with phase noise and phase error reduction for multi-phase clock generation," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, USA, Sep. 2014, pp. 1–4.
- [2] H.-C. Chang, X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: Theory and experiment," *IEEE Trans. Microw. Theory Techn.*, vol. 45, no. 5, pp. 604–615, May 1997.
- [3] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.
- [4] S. A.-R. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, "Analysis and design of a multi-core oscillator for ultra-low phase noise," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 4, pp. 529–539, Apr. 2016.
- [5] H.-R. Kim, C.-Y. Cha, S.-M. Oh, M.-S. Yang, and S.-G. Lee, "A very low-power quadrature VCO with back-gate coupling," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 952–955, Jun. 2004.
- [6] M. Jalalifar and G.-S. Byun, "An ultra-low power QVCO using current-coupling and bulk-injection techniques," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 11, pp. 781–783, Nov. 2014.
- [7] F. Zhao and F. F. Dai, "A 0.6-V quadrature VCO with enhanced swing and optimized capacitive coupling for phase noise reduction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1694–1705, Aug. 2012.
- [8] G. Cusmai, M. Repossi, G. Albasini, A. Mazzanti, and F. Svelto, "A magnetically tuned quadrature oscillator," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2870–2877, Dec. 2007.
- [9] L. Wu and H. C. Luong, "A 49-to-62 GHz quadrature VCO with bimodal enhanced-magnetic-tuning technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 3025–3033, Oct. 2014.
- [10] A. Mostajeran, M. S. Bakhtiar, and E. Afshari, "A 2.4 GHz VCO with FOM of 190 dBc/Hz at 10 kHz-to-2 MHz offset frequencies in 0.13 μm CMOS using an ISF manipulation technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
- [11] K. Aditya, M. Youssef, and S. S. Williamson, "Analysis of series-parallel resonant inductive coupling circuit using the two-port network theory," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Yokohama, Japan, Nov. 2015, pp. 005402–005407.
- [12] T. Xi, S. Guo, P. Gui, D. Huang, Y. Fan, and M. Morgan, "Low-phasenoise 54-GHz transformer-coupled quadrature VCO and 76-/90-GHz VCOs in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2091–2103, Jul. 2016.
- [13] Y. Wachi, T. Nagasaku, and H. Kondoh, "A 28 GHz low-phase-noise CMOS VCO using an amplitude-redistribution technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 482–630.

- [14] A. Nikpaik, A. Nabavi, A. H. M. Shirazi, S. Shekhar, and S. Mirabbasi, "A dual-tank LC VCO topology approaching towards the maximum thermodynamically-achievable oscillator FoM," in *Proc. IEEE CICC*, Sep. 2015, pp. 1–4.
- [15] R. Adler, "A study of locking phenomena in oscillators," Proc. IRE, vol. 34, no. 6, pp. 351–357, Jun. 1946.
- [16] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.
- [17] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi, and A. A. Abidi, "The quadrature LC oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.
- [18] F. F. Dai, F. Zhao, and R. Jiang, "Low noise coupling techniques for multi-phase oscillators," in *Proc. IEEE 11th Int. Conf. ASIC (ASICON)*, Nov. 2015, pp. 1–4.
- [19] M. M. Bajestan, V. D. Rezaei, and K. Entesari, "A low phase-noise wide tuning-range quadrature oscillator using a transformer-based dualresonance ring," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1142–1153, Apr. 2015.
- [20] C. T. Fu and C. Howard, "A 0.8-V CMOS quadrature LC VCO using capacitive coupling," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Jeju, South Korea, Nov. 2007, pp. 436–439.
- [21] R. Jiang, H. Noori, and F. F. Dai, "A Multi-Phase coupled oscillator using dual-tank magnetic coupling technique," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Miami, FL, USA, Oct. 2017, pp. 154–157.
- [22] F. Zhao and F. F. Dai, Low-Noise Low-Power Design for Phase-Locked Loops: Multi-Phase High-Performance Oscillators. New York, NY, USA: Springer, Nov. 2014.
- [23] R. Jiang, H. Noori, and F. F. Dai, "A 2.33-GHz, -133-dBc/Hz, and eightphase oscillator with dual tanks and adaptive feedback," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1399–1410, Mar. 2018.



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