A 2.33-GHz, −133-dBc/Hz, and Eight-Phase Oscillator With Dual Tanks and Adaptive Feedback

Rong Jiang, Hossein Noori, *Senior Member, IEEE*, and Fa Foster Dai, *Fellow, IEEE*

Abstract—This paper presents a multiphase clock generation technique, which employs coupled oscillators and the capacitive-coupling mechanism to achieve both low-power and low-noise characteristics. An oscillator core equipped with both dual tanks and the adaptive feedback technique is proposed. To verify the concept, a four-core coupled oscillator is implemented, and an analytical model on its phase noise performance is presented using the generalized Adler's equation. The proposed four-core coupled oscillator is fabricated in a 130-nm CMOS RF SOI process. It achieves measured phase noise of −133 dBc/Hz at 1-MHz offset from 2.33 GHz. The current consumption for each oscillator core is 10 mA from a 1−V supply voltage. The figure of merit (FoM) of the eight-phase oscillator is 184.3 dBc/Hz; resulting in a per-phase FoM of 193.3 dBc/Hz.

Index Terms—Capacitive coupling, multiphase clock generation, oscillators, phase noise.

I. INTRODUCTION

EMERGING technologies such as N-path filters, phased array antennas, interleaved data converters, and subharmonic mixers escalate the need for multiphase clock generation circuits. In addition, as the number of phases of the clock generator increases, certain side benefits are achieved; e.g., less harmonic distortion for the N-path filter. Therefore, an efficient and expandable solution to generate a multiphase clock is of utmost importance. However, most conventional multiphase clock generation mechanisms are not suitable candidates. For example, the delay-cell-based ring oscillator has poor phase noise, and is not qualified for gigahertz and millimeter-wave applications. Furthermore, the ploy-phase-filter-followed structure is narrowband, and cannot meet the requirements of today's software-defined radio. In addition, the frequency-divider-based clock generator requires an oscillator with N times higher operating frequency, and while it could still be a valid candidate for lower gigahertz applications, it will increase the design complexity and power consumption
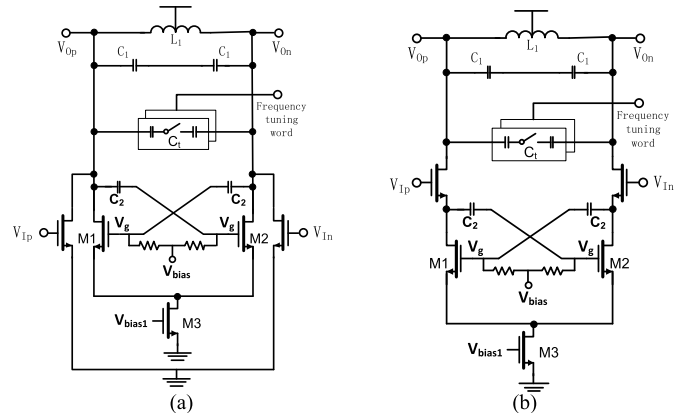
Fig. 1. Conventional transistor-coupled oscillators. (a) Parallel coupling. (b) Series coupling.

as the number of phases and operating frequency increase. With the above in mind, the coupled-oscillator architecture is a potential candidate for multiphase clock generation, since it can achieve high performance, and is easy to expand to a higher number of phases by adding oscillator cells to the coupling path. According to [1], as the number of oscillator cores (N) increases in the coupling system, the overall oscillator phase noise will be improved by a factor of $10 \log_{10} N$. This indicates that additional clock phases and lower phase noise can be achieved simultaneously when using coupled oscillators.

In recent years, several coupling mechanisms have been proposed for coupled oscillators. The most commonly used coupling topology utilizes active devices [2], as shown in Fig. 1. However, the structure with parallel coupling transistors [Fig. 1(a)] suffers from higher power consumption and excess noise due to these additional active devices. Although the structure with a series coupling transistors [Fig. 1(b)] has better phase noise performance, it requires extra voltage headroom, which translates to higher power consumption.

With the above issues in mind, our proposed design uses a capacitive coupling technique [3] for multiphase clock generation, as shown in Fig. 2, which does not suffer from any of the issues mentioned earlier. The proposed multiphase clock generator consists of four oscillators and four coupling paths. Since the oscillators are of differential type, an eight-phase clock can be generated. The coupling among the first three oscillators (i.e., oscillators 1, 2, and 3) is in phase, while that between oscillators 1 and 4 is 180° out of phase
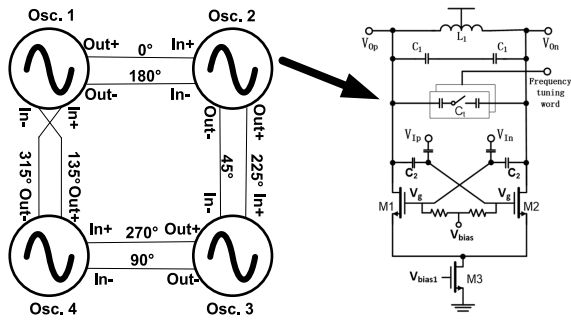
Fig. 2.   Concept of coupled oscillators using capacitive coupling.

in order to create a negative gain stage to meet the phase requirement of the multiphase system.

In addition, to achieve the best performance on the unit cell level, the proposed architecture takes advantage of the recently published techniques to improve the phase noise as much as possible. The following is a brief review of those techniques.

1) Class-F VCO [4] uses a transformer with coupled resonating wings to improve impulse sensitivity function (ISF) by reshaping the output waveform, while Class-C VCO [5] reshapes the current waveform by using a tail capacitor.
2) Alternative ISF manipulation can be implemented by using the adaptive biasing feedback [6], which synchronizes the behavior of the bias transistor with the cross-coupled transistor.
3) The dual-tank technique [7], [8] reduces the operation time of the cross-coupled transistors in the triode region in order to avoid degradation of the Q of the tank.
4) The filtering technique [9], which creates high impedance at the source at ω_0 to form a noise filter.

Nevertheless, some techniques are not suitable for the coupled-oscillator application. For example, capacitive coupling will affect the transformer coupling and output wave reshaping for the Class-F structure. Or, the Class-C architecture requires that the transistor always be far from the deep triode region, which must be fulfilled by another technique such as a low-pass RC filter at the gate to reduce the swing of the drain. Although the filtering and dual-tank techniques both require an additional inductor, the former is less compatible with adaptive biasing feedback. As a result, we arrive at our proposed structure, which adopts only the adaptive biasing feedback and the dual-tank techniques from among all available techniques to form the unit oscillator cell.

However, properly combining unit oscillator cells with capacitive coupling is a great challenge, since it can easily degrade the phase noise instead of improving it. To address this issue, a few modifications were made to each technique as follows.

1) The feedback point is moved from the drains of cross-coupled transistors to their gates.
2) The new capacitive coupling method, unlike the conventional two-capacitor-based structure, utilizes an additional resistor and capacitor in order to be compatible with the dual-tank structure.
3) As a result of incorporating other techniques in the dual-tank oscillator, its voltage and impedance
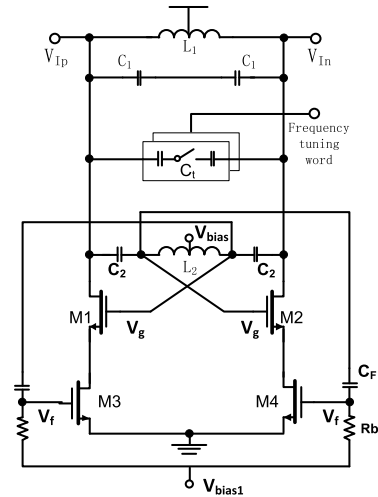

Fig. 3.   Proposed unit oscillator core circuit.

response change. Thus, the new characteristics and the design methodology of the dual-tank oscillator will be discussed.

The proposed oscillator topology features the following to improve the phase noise.

1) Using the capacitive coupling mechanism to shift the injection current to a less sensitive point.
2) Using the intrinsic advantage of the N-core coupled system to reduce the phase noise by a factor of $10 \log_{10} N$ (theoretically).
3) The dual-tank structure minimizes Q degradation caused by the cross-coupled transistors by separating the voltage swing control of their drains and gates and reducing their operation time in the triode region.
4) Using separate transistors for biasing to eliminate the second-order harmonic voltage that is generated if a single-transistor bias is used; therefore, minimizing the noise conversion from the bias transistors to the output.
5) The adaptive biasing feedback path reshapes the tail current and halves the tail transistor's noise.
6) The adaptive biasing feedback path changes the behavior of the cross-coupled transistors, and makes them switch faster in the equilibrium region.

This paper will progressively describe how the proposed unit oscillator core utilizes the capacitive coupling to generate multiple phases while exhibiting excellent phase noise performance. Section II will focus on the unit oscillator structure and provide a brief and intuitive review and explanation of major characteristics of key techniques. In Section III, the proposed structure combined with capacitive coupling will be presented and analyzed. The characteristics of the four coupled oscillator cores are also modeled by using generalized Adler's equation [10]–[12]. The measurement results are presented in Section IV, and conclusions are drawn in Section V.

II. COUPLED-OSCILLATOR STRUCTURE

A. Proposed Unit Oscillator Core

Fig. 3 illustrates the schematic of the unit oscillator core without the coupling path. L_1 and L_2, which are differential

inductors, together with C_1 and C_2 form the dual-tank structure; therefore, the voltage swing of the gate and the drain can be independently adjusted for phase noise optimization. Two nMOS transistors (i.e., M_3 and M_4) provide bias current, and facilitate the feedback implementation. This is in contrast to the conventional single-nMOS transistor current tail. C_F and R_b provide the feedback path, which passes the ac voltage from the gate of M_1/M_2 to the gate of M_3/M_4. Therefore, it further optimizes the phase noise by modifying the current of M_4 and M_3, and improving the ISF of the oscillator. V_{bias1} and V_{bias} provide dc bias for M_3/M_4 and M_1/M_2, respectively. In addition, by adjusting these bias voltages, cross-coupled transistors would spend less time operating at the triode region, which improves their noise performance. C_t is the capacitor bank for frequency tuning.

B. Adaptive Biasing Feedback

The feedback mechanism is implemented by replacing the conventional single-tail transistor with two transistors, and feeding back the signal from the gate of M_1/M_2 to the gate of M_3/M_4. Unlike [6], the feedback is not drawn from the output, where the voltage swing is smaller due to the dual-tank structure. For the sake of clarity, the behavior of the tail and the cross-coupled transistors will be discussed separately.

First, let us discuss the tail transistor. In the conventional single-tail biasing scheme, the second-order harmonic is present at the common-mode node of the cross-coupled transistors; therefore, the 1/f noise of the tail transistor will be up-converted to the close-in frequency band of the output signal. However, in the differential-tail biasing scheme, the common-mode node is eliminated; therefore, the up-converted noise from the tail transistors is at low frequencies only, and the second-order harmonic contributes negligible fluctuation to the output phase. Furthermore, because of the feedback, the behavior of tail transistors M_3/M_4 follows that of their respective branch transistors M_1/M_2; i.e., one of the tail transistors will turn OFF during half of the oscillation cycle. Therefore, the up-conversion of the 1/f noise from tail transistors is largely suppressed. In other words, the noise modulation function (NMF) is almost reduced in half, which leads to a smaller ISF_{eff}.

For the cross-coupled transistors, three types of typical conditions are recognized from their behavior. As shown in Fig. 4, during one cycle of oscillation, transistor M_1 will go through the fully ON to the equilibrium and ultimately to the fully OFF condition. When the transistor is fully OFF, minimum noise and no negative transconductance is generated. On the other hand, when the transistor is fully ON, the degeneration resistor, which is the output impedance of the tail transistor, can suppress the noise of the cross-coupled transistors. As shown in Fig. 5, in the differential-tail biasing case, only one of the tail transistors is ON; as such, the equivalent degeneration resistor exhibited by the output resistance of the tail transistor will be doubled and sufficient to attenuate the equivalent noise presented at the gate of the cross-coupled transistors. During the equilibrium condition, when both M_1 and M_2 are ON, the transistors transfer the maximum amount of noise to the output. Since the feedback will increase
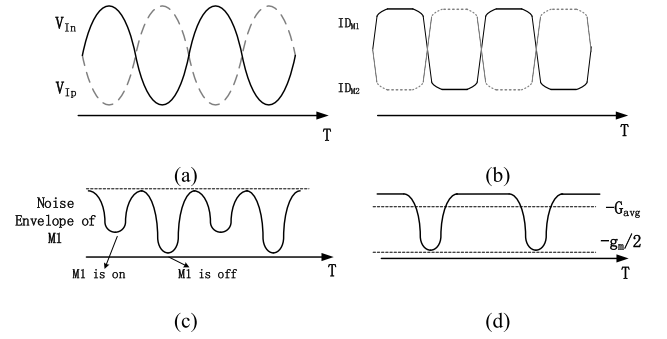

Fig. 4. Behavior of cross-coupled transistors over oscillator output cycles. (a) Drain voltage. (b) Drain current. (c) Noise envelope. (d) $-g_m$ seen from the tank.
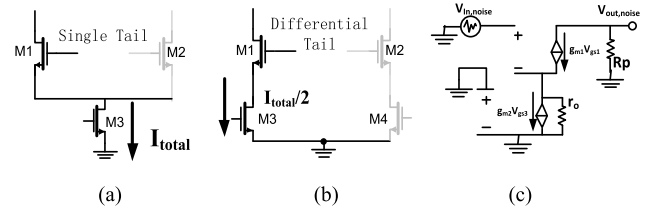

Fig. 5. Illustration of the current flow when M_1 is fully turned ON. (a) Single-tail scheme. (b) Differential-tail biasing scheme. (c) Small-signal model of the differential-tail biasing scheme.

the current during this transition phase, it might appear that it would increase both the thermal and the flicker noise; however, this is not the case. That is because the cross-coupled average transconductance G_{avg}, will be equal to $1/R_P$, and the extra g_m generated by the feedback will force M_1/M_2 to switch faster, and thus spend less time in the equilibrium condition. Therefore, because of the constant G_{avg}, the increase in the peak g_m due to the feedback will actually reduce the noise. In fact, the adaptive biasing feedback increases the bias current when it is needed in order to speed up the transition for suppression of the noise.

C. Dual-Tank Technique

The dual-tank technique is implemented by adding an additional tank (L_2 and C_2) to the conventional single-LC-tank oscillator. Thus, the voltage swing at the gate of the cross-coupled transistors is enhanced. This way, the voltage swing of the drain can be reduced while maintain a large voltage swing at the gate. In the conventional single-tank and cross-coupled oscillator structure, the voltage swing of the output (drain) follows that of the gate with 180° of phase difference. Thus, based on the MOSFET saturation condition ($V_{\text{GS}} - V_{\text{th}} < V_{\text{DS}}$), in the conventional oscillator case, the cross-coupled transistors will operate in the triode region for a long period of time. During the operation in the triode region, the transistors not only contribute a large amount of noise, but also degrade the quality factor of the tank. That is because the transistors act like a tunable resistor with a much lower output resistance which is in parallel with the tank. One way to reduce the noise degradation caused by the small output impedance is to reduce the operation time in the triode region for M_1 and M_2. Owing to the use of the dual-tank structure, the voltage swing at the gate of the
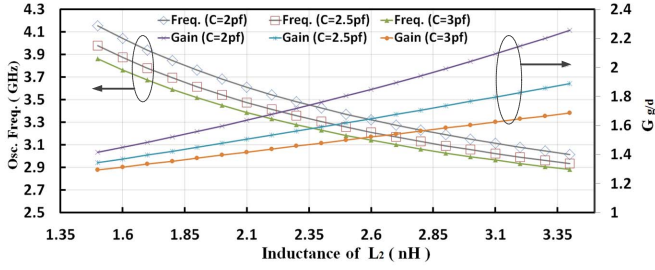
Fig. 6.   Oscillation frequency and $G_{g/d}$ versus L_2 for different C_2 values.

Fig. 7.   Schematics of two candidate implementations of capacitive coupling. (a) Coupling at node $V_{f\pm,j}$. (b) Coupling at node $V_{g\pm,j}$.

cross-coupled transistors is enhanced, and can be larger than that of the drain. This way, the voltage swing of the drain can be reduced while keeping the voltage swing of the gate constant. In other words, the operation time in the triode region is reduced. In addition, according to [7], another way to interpret Leeson's equation regarding the relationship between the output power and phase noise is to treat the phase noise as the result of the output signal-to-noise (SNR) ratio. In this case, without considering the biasing transistor, SNR is equal to the ratio of $\overline{i_d^2} = \mu_n^2 C_{ox}^2 \left(W^2/2L^2\right) \left(V_{GS\_dc} - V_{th}\right)^2 V_{gate}^2$ over $\overline{i_n^2} = 4KT\gamma\, g_{ds} + 4KTG_{tank}$, where i_d and i_n are root-mean square of drain current and total noise current, respectively, and V_{gate} and G_{tank} are the voltage swing of the gate and the parallel tank conductance, respectively. Therefore, if the voltage swing at the gate is kept constant, the phase noise will not be degraded by the reduced drain voltage swing.

The voltage swings of the drain and the gate are a function of the values of the passive components, which are given in [7], and reveal that two oscillation frequencies exist in the dual-tank structure. In order to make the oscillator work at the desired frequency and condition, the ratio of the voltage swing of the gate over that of the drain $G_{g/d}$ as defined in the following equation should be sufficiently large:

$$G_{g/d} = \frac{V_{gate}}{V_{drain}} = \frac{j\omega_0 L_2}{j\omega_0 L_2 + 1/\left(j\omega_0 C_1\right)} = \frac{1}{\left(1 - \frac{\omega_2^2}{\omega_0^2}\right)^2} \quad (1)$$

where $\omega_2 = \sqrt{2}/\sqrt{L_2 C_2}$, and ω_0 is the desired oscillation frequency, which is equals to

$$\omega_0 = \sqrt{v\left(m \pm \sqrt{m^2 - 4n/v}\right)/2} \quad (2)$$

where $m = L_1/C_1 + L_1/C_2 + L_2/C_1$, $n = L_1 L_2$, and $v = C_1 C_2$.

By tuning the values of L_2 and C_2, the desired oscillation frequency and voltage ratio can be obtained. As shown in Fig. 6, if L_2 increases, the oscillation frequency will decrease and $G_{g/d}$ will increase. On the other hand, if C_2 decreases, both the oscillation frequency and $G_{g/d}$ will increase.

III. Proposed Capacitive Coupling

A. Circuit Topology

As mentioned earlier, the capacitive coupling mechanism is adopted in this paper. However, the manner in which the capacitive coupling is used in the proposed unit oscillator
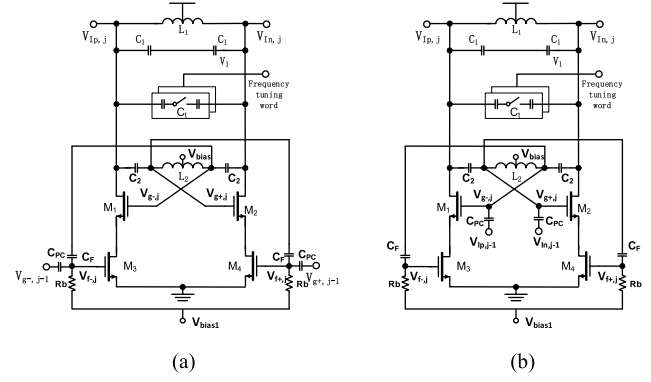
structure should be carefully analyzed in order to maximize the circuit performance. To properly combine the proposed unit oscillator core with the capacitive coupling mechanism, two key points should be kept in mind: first, the capacitive coupling shall have the least interaction with the dual-tank structure, and shall not affect the voltage swings on the gate and the drain of the cross-coupled transistors; second, the signal on the feedback path shall always be in phase with the output, and shall not be interrupted by the coupling path in order to keep the ISF to a minimum.

As shown in Fig. 7, there exist two potential coupling nodes; i.e., $V_{f\pm,j}$ and $V_{g\pm,j}$, where j refers to the index number of the oscillator core. In addition, the coupling at $V_{f\pm,j}$ is through bottom transistors while it is through cross-coupled transistors for $V_{g\pm,j}$.

Fig. 7(a) illustrates the coupling at node $V_{f\pm,j}$. In order to create a coupled signal that is comparable in strength to the signal from the feedback path, the coupled signal is obtained from the gate of the cross-coupled transistors of the adjacent core. However, this kind of coupling will directly interrupt the feedback, and result in phase noise degradation.

Fig. 7(b) shows the coupling at node $V_{g\pm,j}$, where the coupled signal is obtained from the output of the adjacent oscillator core. However, coupling at node $V_{g\pm,j}$ will also interrupt the phase at $V_{g\pm,j}$; therefore, $V_{g\pm,j}$ is no longer in phase with the output voltage; resulting in the degradation of the phase noise. Moreover, the coupling strength is a function of the ratio C_{PC}/C_2, which will affect the $G_{g/d}$ of the dual tank. Therefore, it will create a new trade-off between the coupling strength and the ratio of the gate voltage over the drain voltage.

In order to implement capacitive coupling without interrupting the feedback path, the proposed coupling circuit of Fig. 7(b) is further modified as shown in Fig. 8, where the two capacitors C_{CC} and C_{PC} form the coupling path, and R_S passes the dc voltage from V_{bias} to M_1/M_2. Furthermore, C_{CC} enables M_1/M_2 to form cross-coupled transistors, which present the $-G_m$ impedance to the tank, and maintain the oscillation. In addition, C_{PC} is the path for the coupling of the voltage signal from an adjacent oscillator. The coupled signal is then converted to current by the cross-coupled transistors, and injected in the tank. The coupling strength factor M is
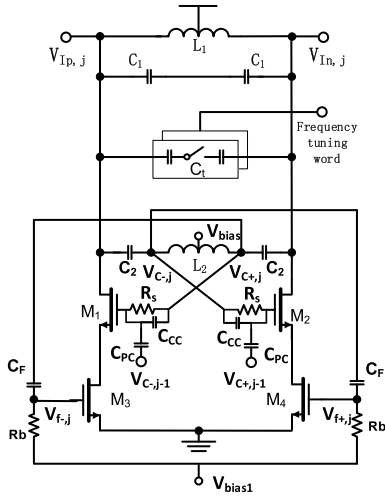
Fig. 8.   Proposed unit oscillator core architecture with coupling paths.

defined as $M = C_{PC}/C_{CC}$, which also represents the ratio of the injected signal to the self-resonance signal.

The proposed coupling structure fulfills our objective in two ways. First, C_{CC} prevents direct coupling to the two sides of inductor L_2; thus, $V_{C\pm,j}$ remains in phase with the output. Second, the voltage swing of various nodes in the dual tank is affected by the total capacitance $C_{tot} = C_{CC} \parallel C_{PC}$; therefore, the coupling strength and $G_{g/d}$ are not interacting with each other if C_{tot} is a constant. By combining a few of the proposed unit oscillator cells and using the coupling mechanism, we arrive at the complete eight-phase oscillator circuit, as shown in Fig. 9.

Often times, the coupling strength creates a trade-off between the phase noise and the phase accuracy [2]. In the proposed structure, this kind of tradeoff exists, as well. By increasing the coupling strength factor, M, the phase accuracy will improve; however, the peak of V_{gate} is shifted toward the zero-crossing point of the output signal, where it has the highest noise sensitivity; thus, the phase noise will be degraded. In order to identify the best trade-off between the phase noise and the phase accuracy, these parameters were plotted versus the coupling strength, as shown in Fig. 10. In order to generate phase error in the simulation, one percent capacitance mismatch was added to the LC tank. As M increases from 0.4 to 1.6, the variation of phase error becomes quite stable for M greater than 1, and the phase noise continues to increase almost linearly.

B. Analysis of Passive Coupling Paths

The capacitive coupling paths of the proposed multiphase oscillator are shown in Fig. 11, where only half of the differential structure is illustrated to simplify the analysis. Fig. 11(a) exhibits coupling paths of the oscillator in Fig. 7(b), while Fig. 11(b) illustrates those of the oscillator in Fig. 8. Both types of coupling implementations discussed in Section III-A are shown side-by-side in Fig. 11 in order to facilitate comparison and provide further details.

As shown in Fig. 11(a), the gate voltage of the cross-coupled transistors $V_{gate+,j}$, consists of two components: $V_{out+,j}$,

which comes from its own tank through C_2, and $V_{out+,j+1}$, which is coupled from the adjacent core through C_{PC}. Therefore, the gate voltage is equal to

$$V_{gate+,j} = (1/(1+M)) G_{g/d'} V_{out+,j+1} + (M/(1+M)) G_{g/d'} V_{out+,j} \quad (3)$$

where $M = C_{PC}/C_2$ is the coupling strength factor, and $G_{g/d'}$ is the redefined ratio of the gate voltage over the drain voltage, and is equal to

$$G_{g/d'} = \frac{(\frac{L_2}{2})/(1 - \omega_0^2 L_2 C_{PC})}{(\frac{L_2}{2})/(1 - \omega_0^2 L_2 C_{PC}) - 2/(C_2 \omega_0^2)}. \quad (4)$$

Since the feedback signal is also directly obtained from $V_{gate+,j}$, the voltage on the feedback path is obviously not in phase with $V_{out+,j}$. Therefore, the phase of the current injected to the bottom transistor will move to a point which is more sensitive to noise. In addition, based on (3) and (4), C_2 and C_{PC}, which are a function of the dual-tank system, determine the coupling strength M; thus, increasing the design complexity. This leads us to use the proposed structure in Fig. 11(b).

As shown in Fig. 11(b), the gate voltage is separated from the feedback, and is still equal to (3); however, the coupling strength factor M is modified to C_{PC}/C_{CC}. The feedback signal is now obtained from $V_{C,j}$, which is in phase with the output voltage $V_{out,j}$. Therefore, $G_{g/d'}$ in (3) is redefined as follows:

$$G_{g/d'} = \frac{\left(\frac{L_2}{2}\right)/(1 - \omega_0^2 L_2 C_{tot})}{\left(\frac{L_2}{2}\right)/(1 - \omega_0^2 L_2 C_{tot}) - 2/(C_2 \omega_0^2)} \quad (5)$$

where C_{tot} is equal to $C_{PC} \parallel C_{CC}$. Therefore, C_2 and C_{tot} are only a function of the dual tanks. In other words, if C_{tot} is a constant, M and $G_{g/d'}$ are not related, as show in Fig. 12, where, as M increases, the voltage ratio $G_{g/d'}$ of the proposed capacitive coupling structure is kept mostly constant, while that of the conventional capacitively coupled structure is decreasing.

In order to visualize the relationship among $G_{g/d'}$, oscillation frequency and C_{tot} the simulated oscillation frequency and $G_{g/d'}$ are plotted as a function of C_{tot} in Fig. 13, where it is clear that both $G_{g/d'}$ and the oscillation frequency of the tank decrease as C_{tot} increases.

C. Phase Relationship

As mentioned in [12], the generalized Adler's equation is a strong tool for analyzing the coupling effects among LC oscillators. To begin the analysis, the equivalent model of the multiphase oscillator is illustrated in Fig. 14, where $i_{TOT,j}$ is the sum of self-resonance current I_j and the coupled current $I_{c,j}$, and their ratio $I_{c,j}/I_j$ is equal to the coupling strength factor M. θ_j is the phase of a given tank, and is expressed as $\theta_j = \omega_{osc} t + \Psi_j$. Therefore, the differential equations for phases and amplitudes based on the generalized
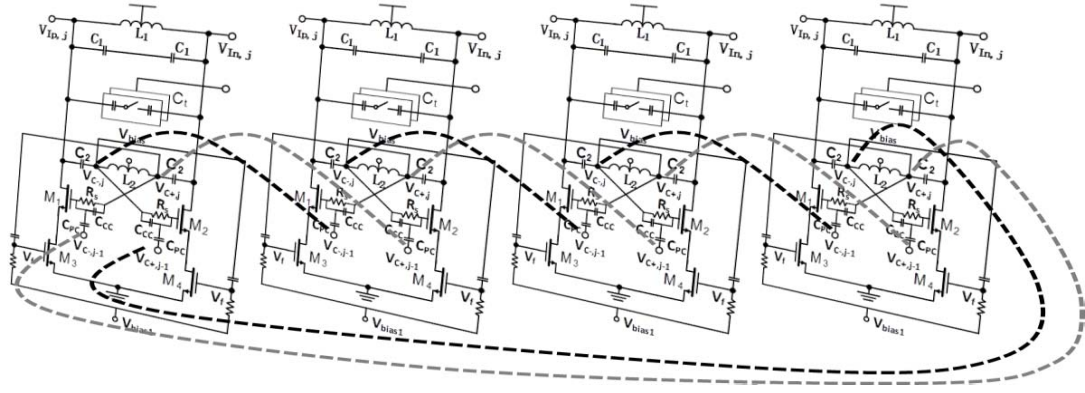
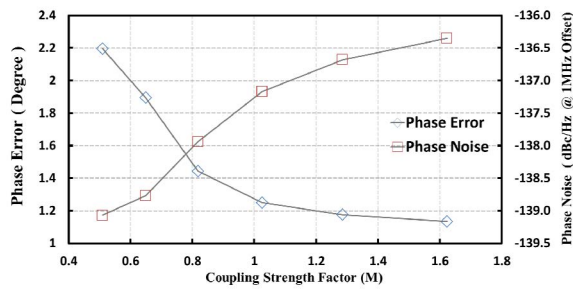Fig. 9. Schematic of the complete capacitively coupled multiphase oscillator.

Fig. 10. Simulated phase error and phase noise versus coupling strength factor.
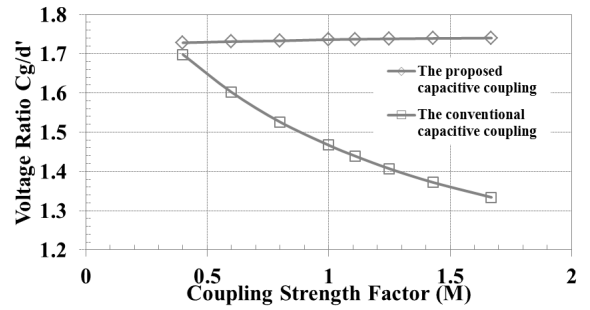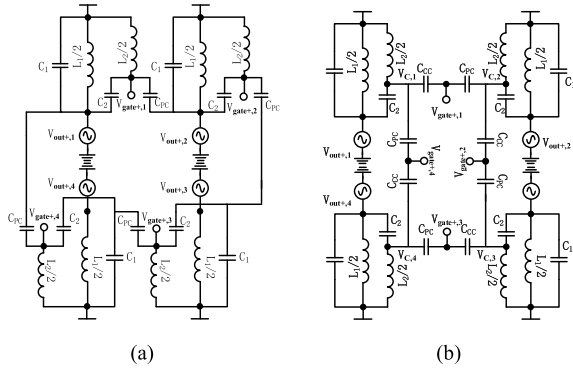

Fig. 12. Voltage ratio $G_{g/d'}$ versus M with both the proposed and the conventional capacitive coupling structures.

Fig. 11. (a) Equivalent circuit of coupling paths in Fig. 7(b). (b) Equivalent circuit of coupling paths in Fig. 8.

Fig. 13. Simulated oscillation frequency and $G_{g/d'}$ versus C_{tot}.
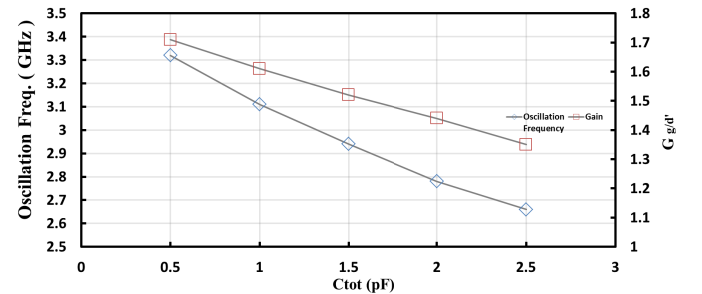
Adler's equation are as follows:

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q} \frac{I_{c,4} \sin(\theta_4 - \theta_1)}{I_1 - I_{c,4} \cos(\theta_4 - \theta_1)} \quad (6)$$

$$\frac{d\theta_2}{dt} = \omega_0 + \frac{\omega_0}{2Q} \frac{I_{c,1} \sin(\theta_1 - \theta_2)}{I_2 + I_{c,1} \cos(\theta_1 - \theta_2)} \quad (7)$$

$$\frac{d\theta_3}{dt} = \omega_0 + \frac{\omega_0}{2Q} \frac{I_{c,2} \sin(\theta_2 - \theta_3)}{I_3 + I_{c,2} \cos(\theta_2 - \theta_3)} \quad (8)$$

$$\frac{d\theta_4}{dt} = \omega_0 + \frac{\omega_0}{2Q} \frac{I_{c,3} \sin(\theta_3 - \theta_4)}{I_4 + I_{c,3} \cos(\theta_3 - \theta_4)} \quad (9)$$

$$RC\frac{dA_1}{dt} + A_1 = \frac{4R}{\pi}(I_1 - I_{c,4} \cos(\theta_4 - \theta_1)) \quad (10)$$

$$RC\frac{dA_2}{dt} + A_2 = \frac{4R}{\pi}(I_2 + I_{c,1} \cos(\theta_1 - \theta_2)) \quad (11)$$

$$RC\frac{dA_3}{dt} + A_3 = \frac{4R}{\pi}(I_3 + I_{c,2} \cos(\theta_2 - \theta_3)) \quad (12)$$

$$RC\frac{dA_4}{dt} + A_4 = \frac{4R}{\pi}(I_4 + I_{c,3} \cos(\theta_3 - \theta_4)) \quad (13)$$

where A_j is the voltage amplitude of a given tank. In the ideal case, since there is no mismatch among oscillators, the tank currents are identical in each core and so are the injected currents. Assuming Ψ_1 is a reference phase, which is zero°, two sets of solutions with a stable condition can be obtained: 1) $\Psi_1 = 0$, $\Psi_2 = \pi/4$, $\Psi_3 = \pi/2$, and $\Psi_4 = 3\pi/4$ and 2) $\Psi_1 = 0$, $\Psi_2 = -\pi/4$, $\Psi = -\pi/2$, and $\Psi_4 = -3\pi/4$. By inserting phases in (6)–(13), the oscillator frequencies and
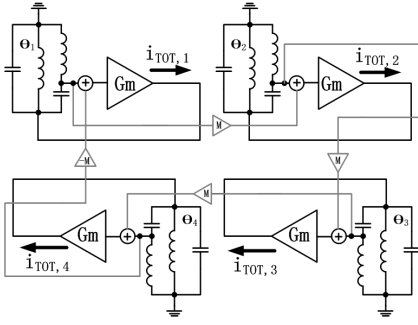
Fig. 14.   Equivalent model of the proposed multiphase oscillator.

Fig. 15.   Plot of phase deviation versus coupling strength factor.

amplitudes for both modes are obtained as follows:

$$\omega_{m1} = \omega_0 + \frac{\omega_0}{2Q} \frac{M\sqrt{2}/2}{1 + M\sqrt{2}/2} \tag{14}$$

$$\omega_{m2} = \omega_0 - \frac{\omega_0}{2Q} \frac{M\sqrt{2}/2}{1 + M\sqrt{2}/2} \tag{15}$$

$$A_{m1} = A_{m2} = \frac{4R}{\pi} I(1 - M\sqrt{2}/2) \tag{16}$$

where ω_{m1} and ω_{m2} are the oscillation frequencies when $\Psi_2 = -\pi/4$ and $\Psi_2 = \pi/4$, respectively. Equation (16) reveals that both modes have the same amplitude; however, the oscillation frequency of one mode is higher than the resonance frequency of the *LC* tank, while that of the other mode is lower. Simulation shows that the proposed oscillator architecture tends to oscillate at the higher frequency. In contrast to the quadrature-coupled oscillator, as the number of cores increases to four in the proposed oscillator architecture, the oscillation frequencies of the cores approach ω_0, and the amplitude of the voltage swing increases. That is because the phase difference between the injected current and the self-resonance current is small, and requires the tank to rotate a smaller angle in order to convert the current to voltage.

The phase error can be analyzed by introducing mismatch to the tank. Let us assume that the mismatch occurs in the first tank, and the phase difference among oscillator cores is $\pi/4$. By substituting ω_0 with $\omega_0 - \Delta\omega$ in (6), and setting $\theta_1 = \omega_{\text{osc}}t$, $\theta_2 = \omega_{\text{osc}}t - \pi/4 + \Delta\varphi_2$, $\theta_3 = \omega_{\text{osc}}t - \pi/2 + \Delta\varphi_3$, and $\theta_4 = \omega_{\text{osc}}t - 3\pi/4 + \Delta\varphi_4$ in (6)–(13), it can be concluded that $\Delta\varphi_2 = \Delta\varphi = \Delta\varphi_3/2 = \Delta\varphi_4/3$. Therefore, the phase deviation due to the tank mismatch can be written as follows:

$$\Delta\varphi = \frac{Q}{2} \frac{(1 + M\cos(\pi/4))^2 + \frac{M}{2Q}(2\sin(\pi/4) + M)}{M(M + \cos(\pi/4))} \frac{\Delta\omega}{\omega_0} \tag{17}$$

where $\Delta\varphi$ is also the phase deviation between adjacent cores.

In Fig. 15, $\Delta\varphi$ versus M with one percent mismatch in the tank capacitor is plotted, where the phase deviation exhibits the same trend as in Fig. 10.

D. Phase Noise

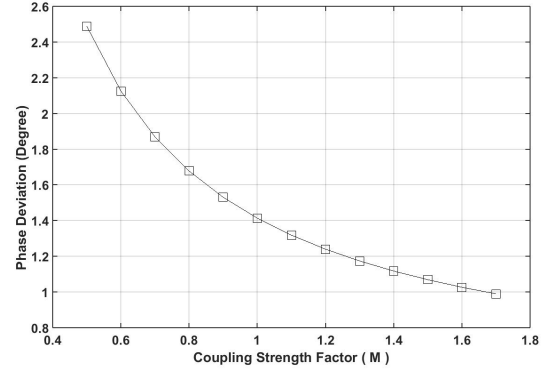The phase noise of the proposed multiphase oscillator can be analyzed by employing the generalized Adler's equation.

In order to obtain a complete expression for the phase noise, the contribution from both the thermal noise and the transistors' 1/f noise is taken into account. First, let us introduce the white noise to the tank by injecting noise current i_n, whose noise power spectral density is $4KT/R$ and whose phase is $\theta_n = \omega_{\text{osc}}t + \omega_m t$. Consequently, the phases of the oscillators become $\theta_1 = \omega_{\text{osc}}t + \hat{\theta}_1$, $\theta_2 = \omega_{\text{osc}}t - \pi/4 + \hat{\theta}_2$, $\theta_3 = \omega_{\text{osc}}t - \pi/2 + \hat{\theta}_3$, and $\theta_4 = \omega_{\text{osc}}t - 3\pi/4 + \hat{\theta}_4$, where $\hat{\theta}_1$, $\hat{\theta}_2$, $\hat{\theta}_3$, and $\hat{\theta}_4$ are the phase fluctuation due to the injected noise. To analyze this noise, (6) is modified as follows:

$$\frac{d\theta_1}{dt} = \omega_0 - \frac{\omega_0}{2Q} \frac{I_{c,4}\sin(\theta_4 - \theta_1) + \frac{\pi}{4}i_n\sin(\theta_n - \theta_1)}{I_1 - I_{c,4}\cos(\theta_4 - \theta_1) + \frac{\pi}{4}i_n\cos(\theta_n - \theta_1)}. \tag{18}$$

By inserting the phases in (6)–(9), and with further simplification, we obtain

$$\frac{d\hat{\theta}_1}{dt} = \frac{\omega_0}{2Q} \frac{M(\cos(\pi/4) + M)}{(1 + M\cos(\pi/4))^2}(\hat{\theta}_2 - \hat{\theta}_1)$$
$$- \frac{\omega_0}{2Q} \frac{\pi}{4} \frac{i_n/I}{1 + M\cos(\pi/4)}\sin\omega_m t$$
$$- \frac{\omega_0}{2Q} \frac{\pi}{4} \frac{i_n/I(M\sin(\pi/4))}{(1 + M\cos(\pi/4))^2}\cos\omega_m t \tag{19}$$

$$\frac{d\hat{\theta}_2}{dt} = \frac{\omega_0}{2Q} \frac{M(\cos(\pi/4) + M)}{(1 + M\cos(\pi/4))^2}(\hat{\theta}_3 - \hat{\theta}_2) \tag{20}$$

$$\frac{d\hat{\theta}_3}{dt} = \frac{\omega_0}{2Q} \frac{M(\cos(\pi/4) + M)}{(1 + M\cos(\pi/4))^2}(\hat{\theta}_4 - \hat{\theta}_3) \tag{21}$$

$$\frac{d\hat{\theta}_4}{dt} = \frac{\omega_0}{2Q} \frac{M(\cos(\pi/4) + M)}{(1 + M\cos(\pi/4))^2}(\hat{\theta}_1 - \hat{\theta}_4). \tag{22}$$

If only the close-in phase noise is considered when $\omega_m \ll M(\cos(\pi/4) + M)/(1 + M\cos(\pi/4))^2$, the phase variation is equal to

$$\hat{\theta}_1 \approx \hat{\theta}_2 \approx \hat{\theta}_3 \approx \hat{\theta}_4 \approx -\frac{\omega_0}{8Q} \frac{\pi}{4} \frac{i_n/I}{1 + M\cos(\pi/4)} \frac{1}{\omega_m}$$
$$\times \left(\cos\omega_m t - \frac{M\sin(\pi/4)}{1 + M\cos(\pi/4)}\sin\omega_m t\right)$$
$$\approx -\frac{\omega_0}{8Q} \frac{\pi}{4} \frac{Ri_n}{V} \frac{1}{\omega_m}\left(\cos\omega_m t - \frac{M\sin(\pi/4)}{1 + M\cos(\pi/4)}\sin\omega_m t\right). \tag{23}$$

Fig. 16. Plot of the phase noise versus M.
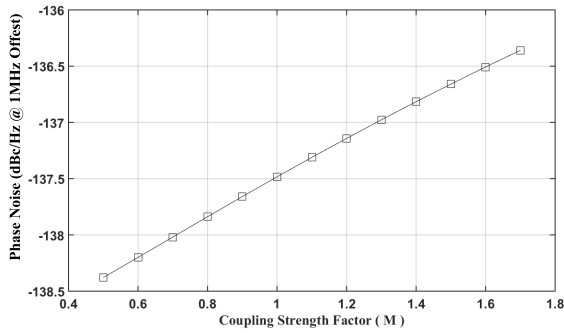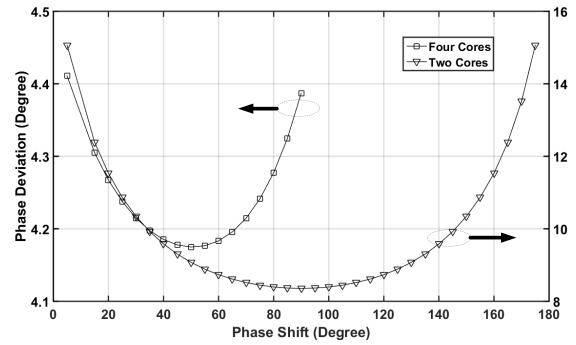

Fig. 17. Plot of phase deviation versus phase shift for both the four-core and the two-core oscillators.

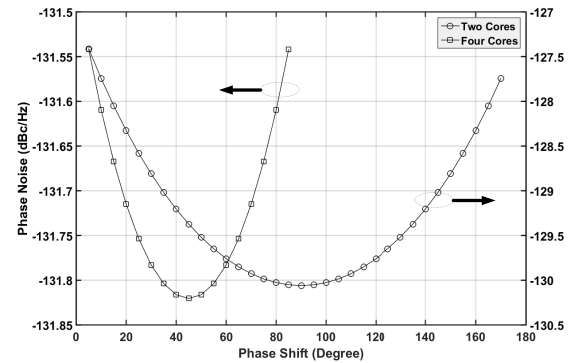Fig. 18. Plot of phase noise versus phase shift for both the four-core and the two-core oscillators.

Therefore, the phase noise contributed by the white noise is equal to

$$
\mathcal{L}(\omega_m) = \frac{1}{T} \int_0^T \hat{\theta}^2(t)\, dt = -\frac{1}{4V_0^2} \frac{kT}{C} \frac{\omega_0}{Q} \frac{1}{\omega_m^2}
$$
$$
\times \left(1 + \left(\frac{M\sin(\pi/4)}{1 + M\cos(\pi/4)}\right)^2\right) \frac{1}{(1 + M\cos(\pi/4))^2}. \tag{24}
$$

By repeating the above analysis for both the regenerative and the coupled noise from the cross-coupled transistors, the ratio of the spectral densities is obtained as follows:

$$
\frac{\mathcal{L}_{\mathrm{SW},C}}{\mathcal{L}_{\mathrm{SW},C}} = M\left(\frac{\cos(\pi/4) + M}{1 + M\cos(\pi/4)}\right)^2. \tag{25}
$$

By combining (22) and (23), the overall phase noise is equal to

$$
\mathcal{L}(\omega_m) = \frac{kTR}{2V^2} F \left(\frac{\omega_0}{Q\omega_m}\right)^2 \tag{26}
$$

where the minimum noise factor is

$$
F_{\min} = 1 + \left(\frac{M\sin(\pi/4)}{1 + M\cos(\pi/4)}\right)^2
$$
$$
+ \gamma \left[\frac{1}{1 + M\cos(\pi/4)}\left(1 + M\left(\frac{\cos(\pi/4) + M}{1 + M\cos(\pi/4)}\right)^2\right)\right]. \tag{27}
$$

The graph of the phase noise versus M in Fig. 16 also illustrates the same trend as the simulation results in Fig. 10.

E. Analysis of Phase Shift

We know that by adding a certain phase shift to the coupling path, both the phase noise and the phase accuracy can be further optimized. Since most publications have focused on two-core (quadrature) oscillators [12], [13], it is worth providing a brief analysis on the four-core structure, and comparing it with the quadrature oscillator. By repeating the above phase noise and phase accuracy analyses with inserted phase shift, (17) and (27) are rewritten as (28) and (29), shown at the bottom of the next page.

From Figs. 17 and 18, the following two major differences are observed between the proposed four-core and the quadrature oscillators: 1) the optimization of the phase noise and the phase accuracy of the four-core oscillator is not as effective

as that of the quadrature oscillator and 2) the most optimum point is shifted from 90° to approximately 45°. As a matter of fact, these results are expected, because as the number of cores increases, the phase of the coupled signal becomes closer to the phase of the output signal. Therefore, it intrinsically moves the peak value of the coupled signal to the point which is less sensitive to noise. On the other hand, if the phase shift moves from 45° to 90° in a quadrature oscillator, there will be little improvement in performance. Since the additional phase shift would increase phase noise, we are not introducing any phase shift to the coupling paths, nor do we recommend this for the four-core oscillator design.

F. Design Methodology

Since the proposed structure is modified by adding extra components and even changing the behavior of the dual tank in order to make it compatible with each technique employed, it is worth discussing the justification behind the choice of some key components from the design perspective.

As mentioned earlier, R_S is added to the critical signal path to provide the dc voltage to the gate of the cross-coupled transistors; therefore, its value will directly affect the noise performance. As shown in Fig. 19, if R_S is so small and comparable to the impedance of capacitor C_1 (1 pF) at 2.4 GHz (i.e., 66 Ω), it will degrade the phase noise. Once R_S increases to 2.8 kΩ, the phase noise becomes flat and starts degrading slightly due to the increased thermal noise from R_S.

For the design of the dual-tank oscillator, we have analyzed three cases with different L_1 and L_2 combinations. As shown
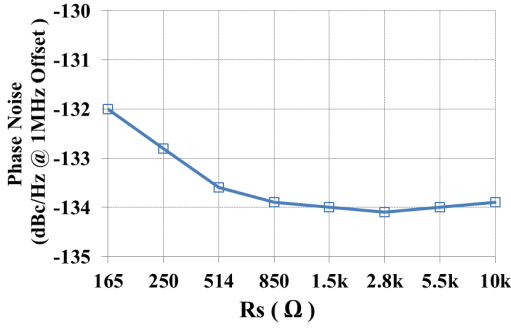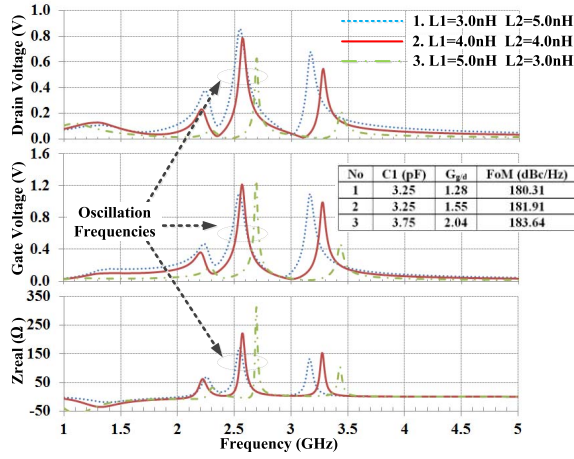
Fig. 19. Simulated phase noise versus R_S.

Fig. 21. Simulated ISF and ISF$_{\text{eff}}$ of both conventional and proposed structures.

Fig. 20. Voltage and impedance response of the proposed dual-tank structure.

Fig. 22. Equivalent circuit for negative transconductance of the proposed oscillator architecture.

in Fig. 20, the voltage and impedance responses are plotted by injecting current to tank, where Z_{real} is the real part of the impedance seen from the output node. In the first case, where L_1 is smaller than L_2, the voltage ratio $G_{g/d}$ is smaller than the other two cases; therefore, the figure of merit (FoM) can still be improved. In the third case, where L_1 is larger than L_2, although the simulation shows a better FoM than the second case, the voltage ratio $G_{g/d}$ is exaggerated and there are a few potential issues. For example, the tank capacitor C_1 needs to be much larger in order to keep the same operating frequency, which will potentially affect the frequency tuning range. In addition, since the output impedance is higher, the current must be reduced in order to maintain the voltage swings of both the gate and the drain. This will force the bottom device to be smaller; thus, potentially affecting the startup condition. This will be discussed in the following section. It is also worth noting that other oscillation modes will be suppressed as L_1 increases and L_2 decreases.
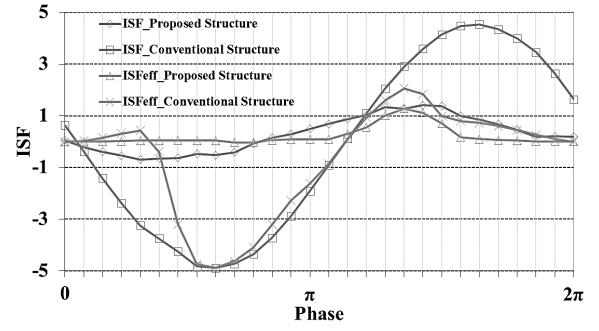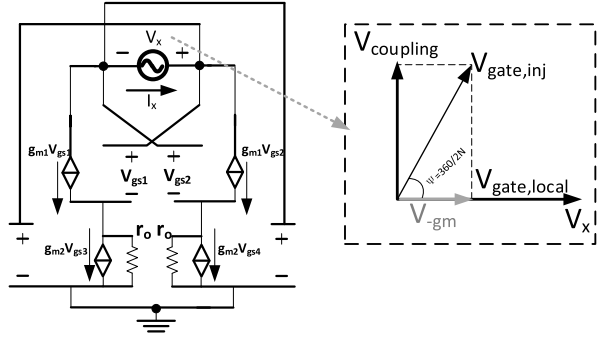
The overall function and performance of the proposed oscillator can be verified by looking at the ISF function. As shown in Fig. 21, compared to the conventional structure (Fig. 2), the ISF of the proposed structure is largely reduced, and the effective ISF, which is the product of ISF and NMF, is close to zero more than three quarters of the time in an operation cycle.

G. Startup Condition

As a result of the feedback path, the startup condition is relaxed in the proposed oscillator structure. In order to illustrate this effect, the equivalent circuit of the active part is shown in Fig. 22. Since the gate length of the bias transistors is larger than that of the cross-coupled transistors, only their output resistance r_o is included in the small-signal model for simplicity. For a single-core oscillator, the negative impedance seen by the tank is equal to

$$R_{\text{startup}} = \frac{2}{g_{m1}} \frac{1 + g_{m1}r_o}{1 + g_{m2}r_o} \tag{30}$$

which must be smaller or equal to the tank loss R_p. Unlike the conventional oscillator, where the negative impedance is fixed

$$\Delta\varphi = \frac{Q}{2} \frac{(1 + M\cos(\pi/4 - \varphi))^2 + \frac{M}{2Q}(2\sin(\pi/4 - \varphi) + m)}{M(M + \cos(\pi/4 - \varphi))} \frac{\Delta\omega}{\omega_0} \tag{28}$$

$$F_{\min} = 1 + \left(\frac{M\sin(\pi/4 - \varphi)}{1 + M\cos(\pi/4)}\right)^2 + \gamma\left[\frac{1}{1 + M\cos(\pi/4)}\left(1 + M\left(\frac{\cos(\pi/4 - \varphi) + M}{1 + M\cos(\pi/4)}\right)^2\right)\right] \tag{29}$$

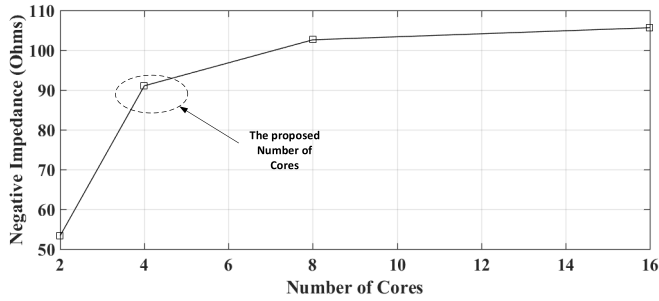Fig. 23. R_{startup} versus the number of oscillator cores at 2.33 GHz.
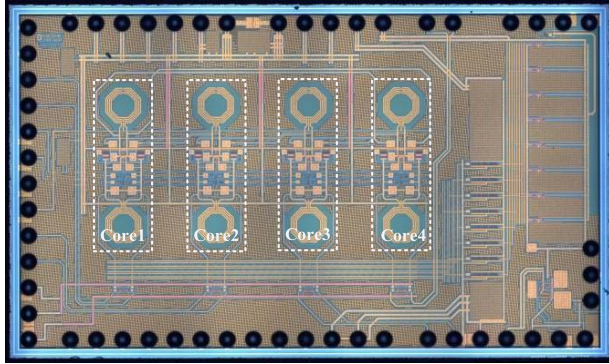

Fig. 24. Die photograph of the proposed four-core oscillator.

and equal to $-2/g_{m1}$, in the proposed oscillator architecture, it is easier to achieve any negative resistance due to the factor $(1 + g_{m1}r_o)/(1 + g_{m2}r_o)$. In summary, if g_{m2} is larger than g_{m1}, which is the case in the proposed design, the startup condition will be relaxed. For the general case of multicore coupling, the signal from both the local core and the coupling core contributes to the startup. Suppose V_{gate} is the gate voltage in a single-core case. As a result, in the multicore case, the part of the gate voltage originating from the local core will be $V_{\text{gate,local}} = V_{\text{gate}}(M/(1+M))$, and that coming from the coupling core will be $V_{\text{gate,}inj} = V_{\text{gate}}(1/(1+M))$. As shown in Fig. 23, only the part of $V_{\text{gate,}inj}$ that is $V_{-\text{gm}}$ and in phase with $V_{\text{gate,local}}$ contributes to the negative impedance, and the rest contributes to the coupling. Thus, assuming all oscillator cores are operating at a stable condition V_x is equal to $V_{\text{gate}}\left(\frac{M}{1+M} + \frac{1}{1+M}\cos(\pi/N)\right)$ and (30) can be rewritten as follows:

$$R_{\text{startup}} = \frac{2}{g_{m1}}\frac{1+g_{m1}r_o}{1+g_{m2}r_o}\left(\frac{M}{1+M} + \frac{1}{1+M}\cos(\pi/N)\right). \quad (31)$$

As shown in Fig. 23, as the number of oscillator cores increases, the coupling system starts up more easily, because the coupled signal increases the portion of voltage that is in phase with the injected output.

IV. MEASUREMENT

The proposed four-core capacitively coupled oscillator is implemented in a 130-nm CMOS RF SOI process, and the die photograph is shown in Fig. 24. The oscillator occupies 1.8×0.95 mm^2 of chip area (0.3×0.95 mm^2 each core).
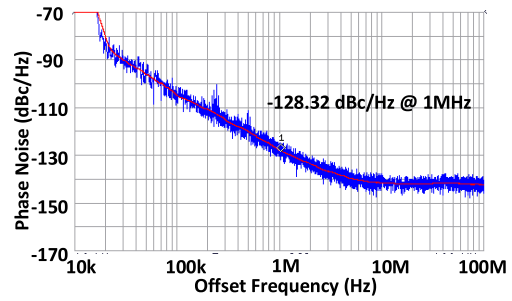

Fig. 25. Measured phase noise at 2.33 GHz (6 mA of current for each core).
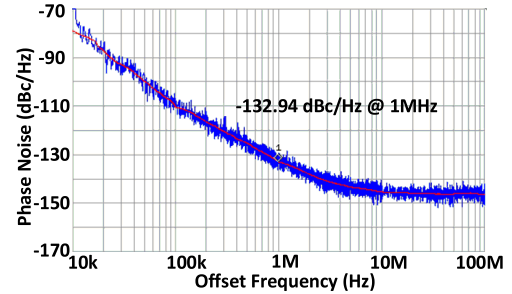
Fig. 26. Measured phase noise at 2.33 GHz (10 mA of current for each core).
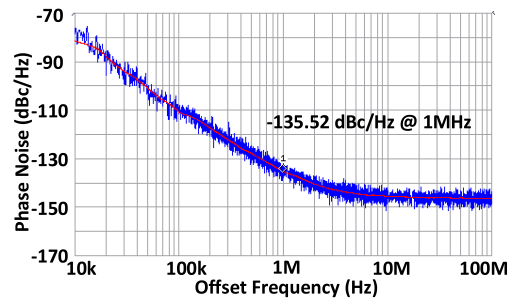
Fig. 27. Measured phase noise at 2.33 GHz (17 mA of current for each core).

Fig. 28. Measured phase noise versus frequency for three dc operating points.

Also, the solder bump is used for flip-chip-type mounting on the PCB.

The phase noise is measured using an Agilent E4440 spectrum analyzer with phase noise option and without averaging. Figs. 25–27 illustrate the measured phase noise at 2.33 GHz under different dc operating conditions. When the currents

Fig. 29.   Measured output waveforms of the proposed four-core oscillator.

TABLE I
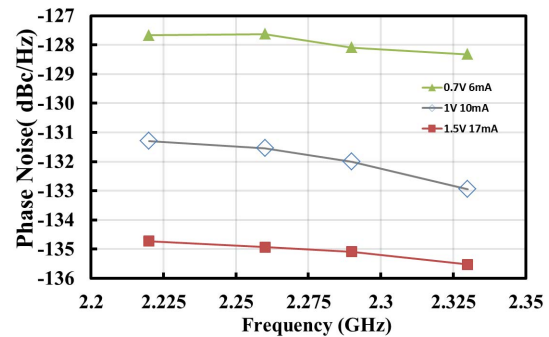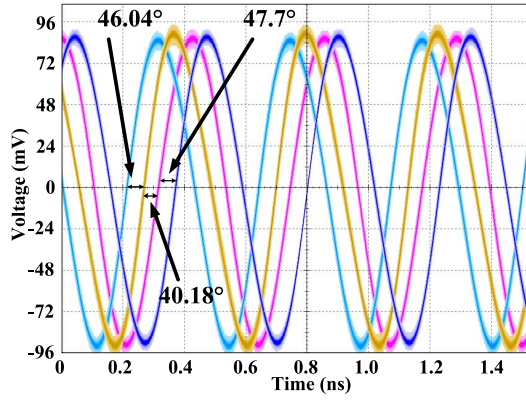PERFORMANCE SUMMARY AND COMPARISON

Ref.	Process	Freq. (GHz)	P.N. (dBc/Hz) @1 MHz	Power (mW)	FoM[a]	No. of Phases	Active Area (mm²)	FoM Per Phase[b]
This work	**130nm CMOS**	**2.33**	**-128.32**	**16.8**	**183.3**	**8**	**1.8 x 0.95**	**192.3**
			-133	**40**	**184.3**	**8**		**193.3**
			-135.52	**102**	**183**	**8**		**192**
[14]	65nm CMOS	14	-110	15	181.2	8	0.7 x 0.7	190.2
[15]	65nm CMOS	4.07	-136	126	188	4	0.98 x 0.38	194
[16]	65nm CMOS	3.8	-123.7	7	185	4	1.0 x 0.35	191

[a] $\text{FoM} = 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1\text{mW}}{P}\right] - \mathcal{L}(\Delta f)$.   [b] $\text{FoM}_{\text{per phase}} = 10\log\left[N\left(\frac{f_0}{\Delta f}\right)^2 \frac{1\text{mW}}{P}\right] - \mathcal{L}(\Delta f)$,
where N is the number of the phase.

for each core are 6 mA (0.7 V), 10 mA (1 V), and 17 mA (1.5 V), the values of phase noise are −128.32, −132.94, and 135.52 dBc/Hz, respectively at 1-MHz offset. Since two frequency-tuning bits are implemented in the design, the operating frequency can be set to 2.22, 2.26, 2.29, and 2.33 GHz. In addition, Fig. 28 illustrates the phase noise versus operating frequency for three different dc operating points.

The output waveforms of the proposed four-core oscillator are measured by a Rohde and Schwarz RTO Digital Oscilloscope, which supports simultaneous measurement of four channels. Fig. 29 exhibits four measured phases, out of eight phases, of the four-core oscillator, where the other four phases are the differential counterparts and are not shown. The phase difference between adjacent outputs, from left to right, are 46.04°, 40.18°, and 47.7°, respectively.

Table I summarizes the performance of the proposed four-core oscillator and compares it with recent multiphase clock generation publications.

V. CONCLUSION

This paper presented a novel oscillator architecture with both the dual-tank and the feedback techniques. Four oscillator cores are capacitively coupled for multiphase clock generation. The proposed coupling technique is analyzed with a theoretical model based on Adler's equations. The proposed phase noise reduction method is verified by measurement, where the ultralow phase noise of −135.52 dBc/Hz at 1-MHz offset from 2.33 GHz is achieved.

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Rong Jiang received the B.S. degree in communication engineering from the Chongqing University of Posts and Telecommunications, Chongqing, China, in 2012, and the M.S. degree in electrical engineering from Auburn University, Auburn, AL, USA, in 2013, where he is pursuing the Ph.D. degree in electrical engineering.

In 2016, he joined the Peregrine Semiconductor Corporation, San Diego, CA, USA. His current research interests include integrated RF front end and VCOs.

Hossein Noori (GSM'09–SM'10) received the B.S. degree in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1995, and the M.S. degree in electrical engineering from Auburn University, Auburn, AL, USA, in 2011, where he is currently pursuing the Ph.D. degree in electrical engineering.

From 1995 to 1997, he was a Telecommunications Researcher with the Office of Research and Standards of the Command of Telecommunications of the Law Enforcement Force of Iran. From 1997 to 2000, he was a Telecommunications Consultant with Tarhe Ertebatat Consultants, Tehran. From 2000 to 2004, he was a Lead RF Systems Engineer with Kaval Wireless Technologies, Toronto, ON, Canada, where he designed several high-profile in-building RF coverage enhancement systems such as that for the Toronto International Airport. From 2004 to 2009, he was a Technical Consulting Manager with inCode Wireless, San Diego, CA, USA. From 2011 to 2013, he was a Technical Consultant with AT and T Mobility, Atlanta, GA, USA. Since 2013, he has been a Staff RFIC Design Engineer with the Peregrine Semiconductor Corporation, San Diego. He has authored or co-authored eight peer-reviewed articles and has one issued patent and two pending patents. His current research interests include programmable and multiband integrated RF front end for mobile handsets as well N-path filters.

Mr. Noori is a Professional Engineer (P.Eng.) and has been a member of the Ontario Society of Professional Engineers in Canada since 2002 and a member of IEEE-HKN, Tau Beta Pi, and a Life Member of Phi Kappa Phi collegiate honor societies.

Fa Foster Dai (M'92–SM'00–F'09) received the Ph.D. degree in electrical engineering from The Pennsylvania State University, State College, PA, USA, in 1998.

From 1997 to 2000, he was a Technical Staff Member of very large scale integration with Hughes Network Systems, Germantown, MD, USA. From 2000 to 2001, he was a Technical Manager/Principal Engineer of RFIC with YAFO Networks, Hanover, MD, USA. From 2001 to 2002, he was a Senior RFIC Engineer with Cognio Inc., Gaithersburg, MD, USA. In 2002, he joined Auburn University, Auburn, AL, USA, where he is currently a Reynolds Family Endowed Professor of electrical and computer engineering. He has authored or co-authored six books and book chapters including *Integrated Circuit Design for High-Speed Frequency Synthesis* (Artech House 2006) and *Low-Noise Low-Power Design for Phase-Locked Loops-Multi-Phase High-Performance Oscillators* (Springer, 2014). His current research interests include analog and mixed-signal circuit designs, RFIC and MMIC designs, and high-performance frequency synthesis.

Dr. Dai was a Guest Editor of the IEEE JOURNAL ON SOLID-STATE CIRCUITS from 2012 to 2013 and the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS in 2001, 2009, and 2010. He served on the Technical Program Committees (TPC) of the IEEE Symposium on VLSI Circuits from 2005 to 2008. He currently serves on the TPCs of the IEEE Custom Integrated Circuits Conference and the IEEE Radio Frequency Integrated Circuits Symposium. He serves on the Executive Committee of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). He was the TPC Chair of 2016 BCTM and the General Chair of 2017 BCTM.