A 2.4-GHz 16-Phase Sub-Sampling Fractional-N PLL With Robust Soft Loop Switching

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***Abstract*— A 16-modulo fractional-N sub-sampling phase-locked loop (SSPLL) with a quadrature voltage-controlled oscillator (VCO) interpolating 16 output phases is presented in this paper. Automatic soft switching between the sub-sampling phase control loop and the frequency control loop is proposed to improve loop robustness against perturbations and interferences, achieving more stable loop dynamics for a larger range of phase errors compared with prior art SSPLL designs. A capacitive phase interpolation network is implemented for 16-phase clock generation starting from quadrature phases. The 16 phases are further utilized to achieve fractional-N operation with a sub-sampling phase detector. This passive phase interpolation at the VCO frequency introduces no extra noise or power and avoids in-band phase noise degradation for fractional-N mode. Implemented in a 130-nm CMOS technology, the SSPLL chip achieves a measured in-band phase noise of −120 dBc/Hz and a measured integrated jitter of 158 fs at 2.4 GHz, while consuming 21 mW with 16 output phases. The measured reference spur and fractional spur levels are −72 and −52 dBc, respectively.**

***Index Terms*— Fractional-N, jitter, multi-phase voltage-controlled oscillator (VCO), phase detector, phase-locked loop (PLL), stability, sub-sampling.**

I. Introduction

PHASE-LOCKED loops (PLLs) are commonly applied for clock and carrier signal generation. Due to circuit non-idealities, the zero-crossing timing of the output clock from a PLL shows random jitter and periodic disturbances, or phase noise and spurious tones in the frequency spectrum. These non-idealities impact systems in various ways such as unwanted spectral emissions and reduced interference robustness due to reciprocal mixing with phase noise and spurs [1]. Techniques and architectures to generate clean clocks are hence of great importance to electronics system. In digital PLL, this can be improved with a high-resolution time-to-digital converter or digital calibrations [2], [3], whereas the in-band phase noise in an analog PLL is limited by the tri-state phase-frequency detector (PFD).

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Recently, a sub-sampling phase detector (SSPD) has proposed as an alternative to the PFD to achieve greatly improved in-band phase noise [4]–[6]. As an SSPD only detects phase, other means are needed for frequency detection and switching between the two detector outputs to define which one controls the voltage-controlled oscillator (VCO). To this end, the SSPLL in [4] uses a tri-state PFD with intentional large dead zone to switch between the frequency-locked loop (FLL) and the sub-sampling (phase) loop (SSL). Due to the narrow capture range of the SSL, the SSL may lose lock in the presence of large perturbations. Moreover, potentially a prolonged relocking time is required as the phase errors need to be accumulated for a quite long time before the dead zone is passed that triggers the FLL to be switched on. This problem was partially solved in [7] by removing the dead zone from the FLL. However, the revised FLL is constantly injecting its charge pump (CP) current as well as its noise into the loop filter. Depending on the amount of current injected from the FLL, the in-band phase noise of the PLL may be degraded. This paper tries to stick to the original idea of the SSPLL in [4] by removing the FLL CP noise when the loop is in lock. We propose an *automatic soft-switching* scheme that eliminates FLL noise in lock, but still ensures agile and robust locking [8]. When the phase error is approaching zero, the proposed scheme *gradually increases the SSL gain and decreases the FLL gain*, while maintaining *a constant total loop gain* during loop transition. As a result, the loop dynamics such as loop bandwidth and gain/phase margin will not vary much throughout the switching process. When the loop is locked, the gain of the FLL is effectively turned off while the SSL is fully turned on, eliminating the FLL noise contribution to in-band phase noise.

Another feature of this paper is the use of an SSL in the context of concurrent multi-phase clock generation. Such clocks are increasingly needed in various circuit building blocks, including the N-path filter, multi-path passive mixer, time-interleaved analog-to-digital converter/digital-to-analog converter, and phased array beam former. Multi-phase clocks can be generated with ring oscillators [9], [10], but the phase noise is inferior compared to *LC*-based VCO. Another widely applied technique is to use an N times higher frequency than the needed frequency followed by frequency division by N [11], [12]. This only works well up to a certain (technology-dependent) frequency. This paper proposes an alternative passive structure for multi-phase clock generation directly at the operational frequency, without involving any higher frequency oscillators and dividers.

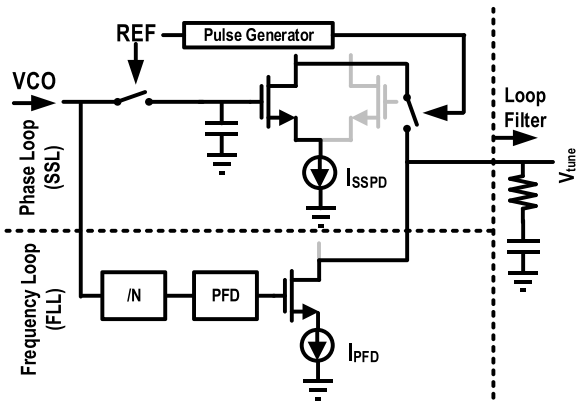

Fig. 1. Simplified block diagram of the dual-loop architecture.

This paper is an extended version of our conference paper [8]. The analysis of the loop switching scheme and the multi-phase interpolator has been extended. Extra simulation and measurement results are given. This paper is organized as follows. Sections II and III discuss our proposed loop gain switching scheme and fractional SSPLL architecture; Section IV presents detailed circuit implementations of various building blocks in the system; measurement results are presented in Section V.

II. Robust Locking With Sub-Sampling Technique

An SSPD can achieve a gain much higher than a traditional tri-state PFD [4], and hence lower in-band noise, as there is more suppression of the noise from the CP, which is the major in-band noise contributor in a classical PLL. On the other hand, since it directly samples the VCO waveform without frequency downscaling, the SSPD maintains its high gain only within a small region around zero crossing of the VCO waveform. If for some reason a relatively large phase error exists after the loop is locked, the in-band noise floor might be degraded due to reduced SSPD gain. Furthermore, the sampled voltage of an SSPD operating on a sinusoidal VCO signal only works well within $\pm\pi/2$ phase shift compared to the zero crossing. Beyond that the SSPLL may lock to another VCO zero crossing with long relocking time or might even never regain lock on its own.

A. Soft Loop Gain Switching Scheme

To improve the robustness of locking with an SSPD, a simplified SSPLL block diagram of our proposed dual-loop gain switching scheme is shown in Fig. 1. The conversion gain of the feedback path from VCO output phase ($\Delta\varphi$) to CP output current (ΔI) in the SSL can be derived as [4]

$$G_{\mathrm{SSL}} = \frac{\Delta I}{\Delta\varphi} = A_{\mathrm{VCO}} \cdot \frac{\sin(\Delta\varphi)}{\Delta\varphi} \cdot \frac{\tau}{T_{\mathrm{ref}}} \cdot g_m = A_{\mathrm{VCO}} \cdot \mathrm{sinc}(\Delta\varphi) \cdot \frac{\tau}{T_{\mathrm{ref}}} \cdot \sqrt{2\mu C_{\mathrm{ox}} \frac{W}{L} \cdot I_{\mathrm{SSPD}}} \quad (1)$$

where A_{VCO} denotes the magnitude of the VCO waveform, $\Delta\varphi$ is the loop phase error, τ represents the output current pulsewidth, and T_{ref} represents the reference period, respectively. Similarly, the conversion gain of the feedback path from VCO output phase to CP output current in the FLL can be found as

$$G_{\mathrm{FLL}} = \frac{\Delta I}{\Delta\varphi} = \frac{1}{N} \cdot \frac{I_{\mathrm{PFD}}}{2\pi} \quad (2)$$

where N and I_{PFD} represent the division ratio and the CP current, respectively. Thus, the total loop gain of the dual-loop PLL shown in Fig. 1 is given by $G_{\mathrm{total}} = G_{\mathrm{SSL}} + G_{\mathrm{FLL}}$.

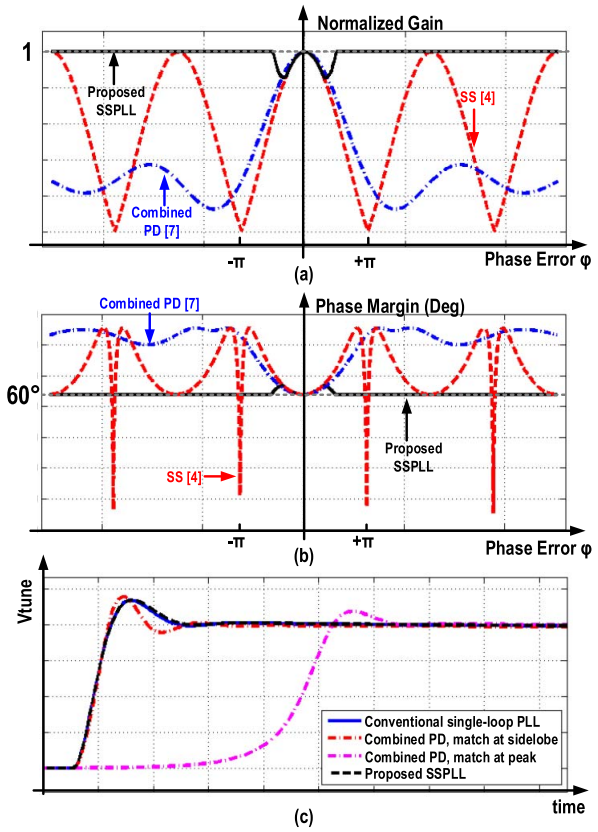

Fig. 2. Illustrations of (a) total loop gain normalized by its maximum value and its variation versus static phase error. An SSPD with dead zone [4] shows a repeated profile due to harmonic locking; the combined SSPFD [7] shows a sinc profile, and our proposed scheme features a rather constant gain. (b) Phase margin variation versus static phase error. (c) Transient loop locking behavior.

Multiple approaches exist to combine the SSL and the FLL. Fig. 2(a) presents the total loop gain normalized by its maximum value versus static phase errors for some prior art designs and our proposed soft-switching scheme. The SSPD assisted with dead zone PFD [4] shows a periodic behavior because it can lock to any zero crossing of the VCO waveform. Since the phase error is still within the dead zone, the FLL is not activated in this case [4]. Each null corresponds to a large drop in-phase margin as shown in Fig. 2(b), which causes potential stability issues. Since G_{SSL} follows a sinc function with respect to the phase error and G_{FLL} shows a constant gain, directly summing these two terms as suggested in [7] leads to a gain profile of a sinc function with a dc offset shown in Fig. 2(a). Although this combined SSPFD approach [7] can avoid harmonic locking, the loop experiences large gain variation as the phase error changes from $\pm\pi$ to 0.

Consequently, loop bandwidth and phase margin also vary dramatically, causing stability concern. The problem can be further exacerbated in this architecture since the gain of the FLL needs to be very small in order to reduce the extra noise from the FLL. With the minimum FLL gain, the loop barely maintains a positive total gain for arbitrary phase error, making the total loop gain close to 0 when the phase error approaches $\pm\pi$.

The core idea of our proposed gain switching scheme is to tune the current I_{SSPD} and I_{PFD} dynamically with respect to the phase error such that, instead of a direct superposition, soft switching from one loop to the other is achieved. As a result, the total loop gain variation is reduced. Initially, only the FLL is activated by tuning I_{PFD} to its maximum. As the loop drives toward locking, the SSL will be activated while the FLL will be turned off once the phase error is sufficiently small such that the SSPD can safely lock on its own. After phase locking is achieved, only the SSL remains active. Note that turning off FLL with I_{PFD} only shuts down the CP in the FLL, whereas both the PFD and the divider still need to remain active to detect phase error. Our proposed loop gain switching scheme shows only slight gain and phase margin variations during loop switching as shown in Fig. 2, leading to much improved stability. In addition, the CP in the FLL is totally off at lock in, resulting in low in-band phase noise performance in the proposed SSPLL.

During the lock process, the phase error largely varies. A constant loop gain during the lock process avoids variations in loop dynamics. As a result, the system is robustly stable and relocking time and overshoot are predictable. As shown in Fig. 2(c), large variations in open-loop gain for the combined PD scheme [7] cause difficulties during the locking process in which the SLL and FLL loop gains are always added. If the loop gains are matched to the desired gain (which leads to the desired locking time and overshoot) at its peak, the locking time will be prolonged [see Fig. 2(c)] since the gain for larger phase error is too small. On the other hand, if the total loop gain is matched at its (sinc) sidelobe level, larger overshoots result since the peak gain at zero phase error is too large. In comparison, the proposed soft loop switching scheme gives a consistent locking behavior over the entire locking process due to the constant loop gain.

To ensure equal gain of two loops in our proposed structure, the PFD needs to match the peak gain of the SSPD which is usually much larger. Thus, a large CP current I_{PFD} is required to achieve this gain matching. Fortunately, the CP in the FLL is turned off after phase lock, avoiding its power consumption and the large noise associated with a large current. During the loop switching, it becomes more difficult to maintain a constant gain since G_{SSL} follows square root relationship with respect to current (1) while G_{FLL} follows a linear relationship with its current (2). As a compromise between complexity and effectiveness, we propose to reduce gain variation during the switching by making the total current a constant:

$$I_{\mathrm{total}} = I_{\mathrm{SSPD}} + k \cdot I_{\mathrm{PFD}} \tag{3}$$

where k represents current ratio between CPs in SSPD and PFD since the current in PFD needs to be larger than that in SSPD for gain matching ($k \approx (1/3)$ in our case). As we will show below, this can be conveniently achieved with a differential pair where its tail current source sets the total current.

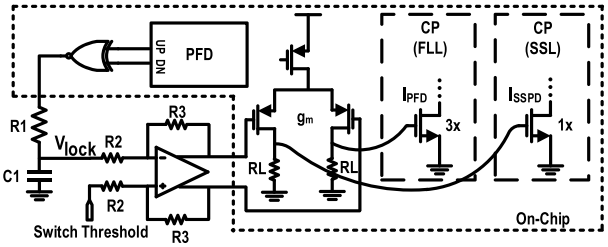

Fig. 3. Simplified schematic of the proposed loop switching controller.

B. Loop Switching Controller

As shown in Fig. 3, our proposed loop gain switching controller can be broken down into three parts. First, an XNOR gate is tied to the PFD output in the FLL. Along with a low-pass *RC* filter, an averaged loop phase error ε can be measured [13]. The output signal V_{lock} is inversely proportional to the phase error, meaning smaller ε leads to a higher V_{lock}. In the second part, an amplifier, or a soft comparator, consisting of an operational amplifier is utilized to compare V_{lock} with a programmable switching threshold. This threshold shall be set sufficiently high in order to ensure that the switching from the FLL to the SSL occurs only after the phase error is within the locking range of the SSPD, i.e., one VCO period. In addition, a high threshold also helps with fast switching from the SSPD to the PFD once the loop somehow loses phase lock due to perturbation. The third part consists of a PMOS differential pair which directly drives current sources in CPs of the FLL and the SSL. The differential pair ensures a constant sum of a scaled PFD current and the SSPD current for a constant loop gain. The reason for using resistors instead of current mirror is to ensure the deactivated loop being entirely off. During loop switching, we assume the differential pair in linear mode, thus defining a small signal switching gain of the loop switching controller

$$G_{\mathrm{sw}} = \frac{\Delta V}{\Delta \varphi} = \left(\frac{V_{\mathrm{DD}}}{2\pi}\frac{1}{1+sR_1C_1}\right)\cdot\left(1+\frac{R_3}{R_2}\right)\cdot(g_m R_L) \tag{4}$$

where V_{DD} and g_m denote the power supply voltage and transconductance of the differential pair. Three brackets represent contribution from each part in switching controller.

The simulated loop gain normalized by its maximum value versus phase error (V_{lock}) over different process corners and temperatures is shown in Fig. 4. A tolerable worst peak-to-peak gain variation of 18% is observed. To compensate for different process corners, the bandwidths (i.e., open-loop gain) of the two loops are calibrated to be equal before normal operation. As a result, the loop only needs to tolerate the variations from temperature and voltage. The phase margin of the loop is designed with sufficient margin such that the loop will always be stable across process, voltage, and temperature (PVT) variations. Relocking time with switching threshold

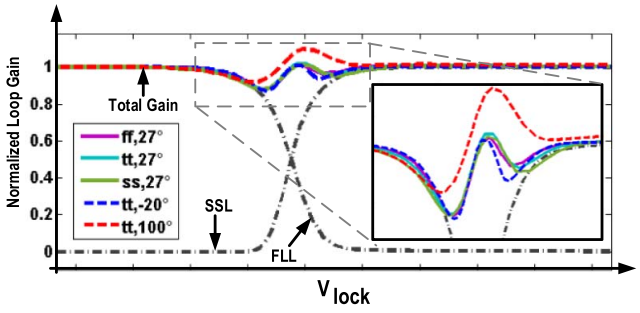

Fig. 4. Simulated loop gain variation for the proposed soft loop switching scheme over process corners and temperatures. ff, tt, and ss denote fast, typical, and slow corners, respectively, and all temperatures are in Celsius.

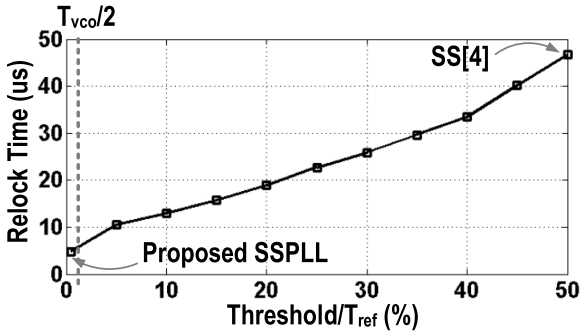

Fig. 5. Simulated relocking time versus the percentage of switching threshold over reference period; division ratio $N = 48$.

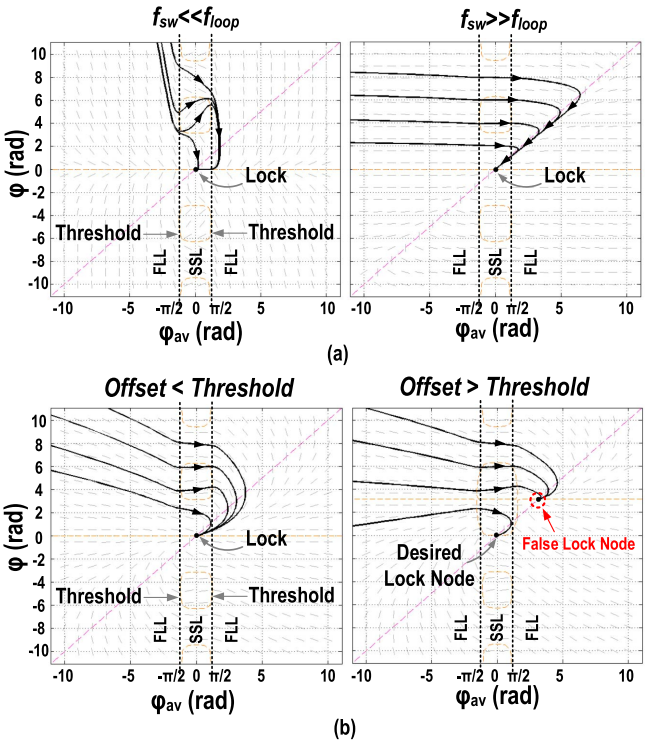

Fig. 6. Simulated phase portrait of the proposed soft-switching SSPLL with (a) different soft-switching control bandwidth f_{sw} and constant loop bandwidth. (b) Different phase offsets between the SSL and the FLL. Center of the plots indicates the lock state.

normalized by reference period has been simulated, as shown in Fig. 5. A voltage perturbation corresponding to a frequency step of 3 MHz is injected to the VCO tuning input after the loop is locked. This causes the SSL to lose lock while the FLL will be activated depending on the switching threshold. The relocking time increases with the larger switching threshold since the phase error needs to be accumulated for a longer time in order to trigger the FLL.

C. Locking Analysis for the Switched PLL

The proposed dual-loop PLL architecture with soft-switching scheme can be analyzed as a hybrid switched system exploiting existing control theory. The foregoing analysis on the loop gain and the phase margin variation is based on the assumption that the phase error has settled to a constant value, i.e., a quasi-static phase error. However, the implemented switching scheme is not only controlled by the instantaneous phase error, but also rather by its averaged value produced by R_1 and C_1 in Fig. 3. To estimate the low-pass filter effect, we used a simplified model with a type-I PLL for both the SSL and the FLL. The differential equation of the switched PLL can be described as

$$\begin{aligned} d\varphi_{\text{av}}/dt &= (\varphi - \varphi_{\text{av}})/(R_1 \cdot C_1) \\ d\varphi/dt &= -K_{\text{SSL}}\sin(\varphi) \cdot (1 - \tanh(g \cdot (|\varphi_{\text{av}}| - \varphi_{\text{th}}))) \\ &\quad -K_{\text{FLL}}\varphi(1+\tanh(g \cdot (|\varphi_{\text{av}}| - \varphi_{\text{th}} - \varphi_{\text{offset}}))) \end{aligned} \quad (5)$$

where K_{SSL} and K_{FLL} represent the SSL and FLL loop gain; φ and φ_{av} represent the instantaneous and averaged (filtered with R_1 and C_1) phase errors, and g represents a scaling parameter which is proportional to the switching gain G_{sw} as in (4). For simplicity, the loop soft-switching behavior shown in Fig. 4 is modeled with a hyperbolic tangent function. Parameters φ_{th} and φ_{offset} represent the switching threshold in radian and the phase offset between the two loops. φ_{th} can be converted to the corresponding voltage with $V_{\text{th}} = \varphi_{\text{th}}(V_{\text{DD}}/2\pi N)$, where V_{DD} is the supply voltage and N is the division ratio. The simulated phase portrait of the switched PLL with different switching control-loop bandwidth f_{sw} (defined as the bandwidth of the low-pass filter formed by R_1 and C_1) and a constant loop bandwidth f_{loop} is shown in Fig. 6(a). Using a high f_{sw}, φ_{av} is quickly converging to the actual phase error. In case of a low f_{sw}, the PLL does not switch to the FLL fast enough at large phase errors, driving itself away from locking in some regions. However, eventually the loop is still able to achieve locking.

Since the feedback path of the FLL includes an additional multi-modulus divider compared to the SSL, the propagation delay in the feedback path can differ by hundreds of picoseconds between the two loops. Unbalanced layout and PVT variation can further exacerbate the delay mismatch. Such mismatch not only causes a larger loop gain variation, but also might lead to multiple locking points. As shown in Fig. 6(b), as long as the offset remains below the switching threshold, only one stable point exists on the phase portrait. For a phase offset larger than the threshold, the nullclines of φ_{av} where its derivative is zero intersects with that of φ, causing an additional stable node, i.e., false locking where only the

FLL is in lock while the SSL is not. To compensate for the propagation delay mismatch, we have implemented a calibration utilizing the tunable delay d_T on the reference path which will be covered in Section V.

III. Multi-Phase Generation for Fractional-N Mode

A. Fractional-N Mode With SSPD

In integer-N mode, the VCO zero crossing will always be aligned with the reference edge after phase locking since the VCO frequency is an integer multiple of the reference frequency. Extending the SSPLL to fractional-N mode requires the divider to switch between multiple integer division ratios in every reference cycle [14], causing instantaneous phase error while achieving a correct equivalent fractional division ratio on time average. Consequently, the VCO or the feedback edge will move periodically around the reference edge, creating instantaneous phase errors even after phase locking. In case of a basic fractional operation where the divider switches between N and $N+1$, the maximum phase error, or the phase gap, can reach one VCO cycle. Considering the narrow locking range and even narrower high-gain range of the SSPD, the feedback signal, and the reference signal needs to be properly realigned before feeding into the SSPD for fractional-N operation.

Prior art designs have proposed to utilize a tunable delay or digital-to-time converter (DTC) on the reference path [15]–[17] to build a fractional-N SSPLL. By appropriately delaying the reference clock in every cycle, the phase gap between the reference edge and the feedback edge can be closed. However, this DTC is required to cover one or multiple VCO cycles with a fine resolution to provide the required fractionality. Furthermore, the DTC needs to be highly linear; otherwise large fractional spurs will arise. Delays from inverters will also contribute extra noise proportional to the amount of delay inserted as argued in [18] and [19]. Introducing large amount of delay on the reference might severely degrade PLL's in-band noise floor since its jitter will be multiplied by N^2 when transferred to the PLL output. Other approaches have proposed using active phase interpolator [19], [20] to decrease the amount of delay required on the reference path. However, the phase interpolator still contributes additional noise and consumes a large portion of the total power from the entire PLL [19]. In addition, only one VCO phase can be generated at a time in this structure whereas some applications require multi-phase clock outputs as discussed previously.

In our proposed PLL, edge alignment is achieved through utilizing multiple interpolated VCO phases uniformly spanning from 0° to 360°. By selecting the VCO output phase, in each reference cycle, which provides a zero crossing that is closest to the reference edge, the phase gap can be decreased to π/M where M denotes the number of available VCO phases. Furthermore, by using a fractionality of n/M where n denotes an arbitrary integer between 1 and $M-1$, it is possible to close the phase gap for every reference edge, as the phase error increment without selecting another VCO output is equal to the phase error difference between two VCO outputs. Ideally, the SSPD would see zero phase error thus exhibiting a clean

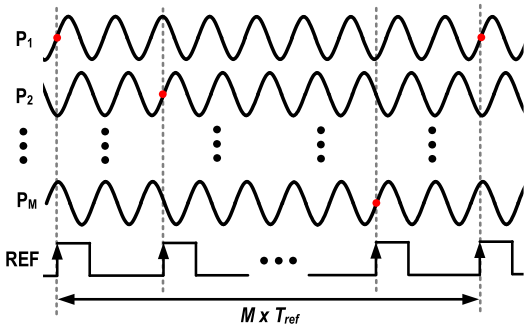

Fig. 7. Realignment of VCO zero crossing and reference edge utilizing a multi-phase VCO.

output spectrum without any fractional spurs. Consider a simple example as shown in Fig. 7, a fractional PLL is achieved with M VCO phases P_1–P_M. By jumping one VCO cycle each time, the sampling reference edge is always aligned with one of the zero crossings of VCO waveform. To generalize this idea, the fractional frequency can be programmed as

$$f_{\text{frac}} = \left(N + \frac{n}{M}\right) \cdot f_{\text{ref}} \tag{6}$$

where N, n, and M represent the integer division ratio, the VCO phase jump in each cycle, and the total number of available VCO phases, respectively. n can be an arbitrary integer number from 1 to $M-1$. Compared with prior art using extra delay on the reference path or an active interpolator, our proposed architecture involves no active components, thus minimizing the extra power or noise for fractional-N operation and multi-phase clock generation. Note that even though the interpolation network does not consume power, the phase selecting multiplexer consumes about 1 mA.

B. Capacitive Interpolation for Multi-Phase Clock Generation

In our proposed design, the generation of multiple clock phases is achieved through capacitive interpolation with a quadrature LC oscillator. A similar VCO architecture with fewer interpolated phases has been proposed in [21]. Consider a simple case of two capacitors connected in series between the in-phase (I) and the quadrature (Q) component of a quadrature VCO (QVCO) output. By tuning the ratio of two capacitors, arbitrary phase between 0° and 90° can be interpolated. In this PLL, the QVCO output is further extended into interpolating 16 phases as shown in Fig. 8. Four capacitors are connected in series between 0° and 90° from the QVCO to generate three additional sub-phases of 22.5°, 45°, and 67.5°, respectively. Let us define a capacitor ratio $\alpha = C_2/C_1$. The phase at each node can be determined using superposition calculating the contribution from the I and Q component, respectively.

First, let us ignore the loading effects. Later, we will include parasitic loading effects and also consider the effect on oscillation frequency and Q of the tank in the VCO. From $I+$ to $Q+$, the phase at the first node can be found to be $\tan\theta = \alpha/(\alpha+2)$. Using θ of 22.5°, α can be calculated to be $2^{1/2}$ which is approximated with 1.4 in the

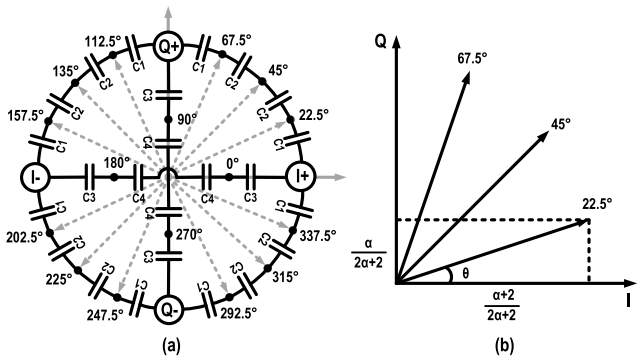

Fig. 8. (a) Capacitive phase interpolation network. (b) Interpolating arbitrary phases from a pair of quadrature signals with capacitance ratio $\alpha = C_2/C_1$.

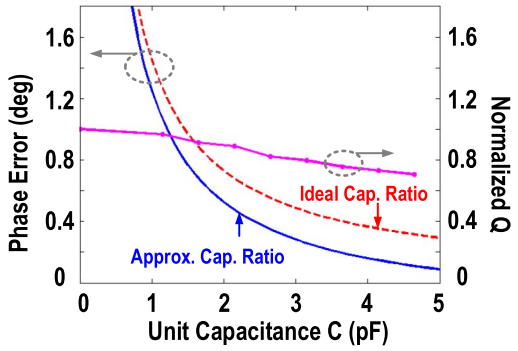

Fig. 9. Effect of interpolating capacitance value on phase error reduction with parasitic loading and VCO tank quality factor degradation.

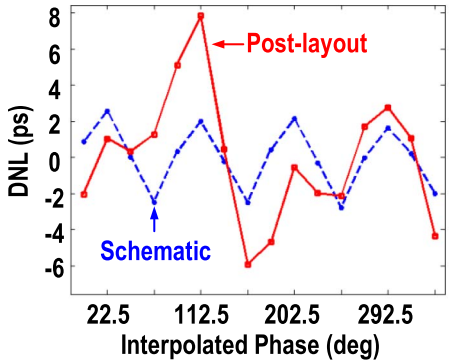

Fig. 10. Simulated phase error DNL of interpolated output phases before and after parasitic extraction.

actual implementation. Even though the phase can be tuned to arbitrary value, magnitude of the interpolated phases can have slight variation. With an α of $2^{1/2}$, magnitude at 22.5°, 45°, and 67.5° can be calculated to be approximately 0.765, 0.707, and 0.765 assuming a unity magnitude at $I+$ and $Q+$. Even though subsequent buffers will reshape interpolated sinusoidal waveform into square wave with similar magnitude, this nonuniform magnitude still causes a certain amount of phase error in interpolated VCO phases. To match the magnitude with interpolated phases, the magnitude of the original four VCO phases is scaled down as well with capacitors C_3 and C_4 as shown in Fig. 8. With a capacitance ratio C_4/C_3 of $(2^{1/2}-1)$, the output magnitude of four quadrature phases is scaled to 0.707. Again, this capacitance ratio is approximated with 0.4 in the actual design. In summary, assuming $C_3 = C_4 = C$ as the unit capacitance, all capacitor values can be found as: $C_1 = 1.4\ C, C_2 = C_3 = C$, $C_4 = 0.4C$.

Having determined the capacitance ratio, we can now discuss how to choose the absolute value for these capacitors. Parasitic capacitance tends to create additional phase error in the interpolated phases. Larger interpolation capacitors alleviate the parasitic impact while reducing the achievable oscillation frequency. A load of 30 fF representing the input capacitance of the next stage is attached to each output of the interpolation network. The simulated phase error at the node 22.5° is shown in Fig. 9. Phase error larger than 2° can be observed for small unit capacitance C. Approximating the ideal capacitance ratio $2^{1/2}$ with 1.4 caused a phase difference of about 0.2°. For very large C, the phase error is approaching zero with ideal capacitance ratio. However, larger unit capacitance C occupies more area which also leads to more parasitics. Furthermore, it also adds extra capacitive loading on the VCO, decreasing its oscillation frequency and tuning range. The simulated VCO tank quality factor, as shown in Fig. 9, decreases with larger C, requiring more VCO power to maintain the same oscillation frequency and phase noise. In our design, a unit capacitance of about 1.2 pF is chosen as a compromise in this tradeoff.

The simulated phase error is shown in Fig. 10. From schematic-level simulation, due to the nonuniform interpolated magnitudes as mentioned earlier, periodic phase maxima and minima can be observed on the differential nonlinearity (DNL). In post-layout simulation with all the parasitic, the phase error between interpolated phases increased due to imbalanced layout and wiring which is difficult to avoid entirely. Large fractional spurs will arise if these phase errors are left unresolved. We utilized the tunable delay d_t on the reference clock path to compensate for these small variations. Based on the sampled voltage in SSPD, different delays are assigned on the reference path for each phase which is achieved with an on-chip digital logic. Details of this calibration will be covered in Section V. However, this can only reduce the spurs in fractional-N mode. For multi-phase clock application where each phase is required to be evenly spaced, a controllable delay running at VCO frequency is needed at each interpolated nodes.

IV. System and Building Blocks

A block diagram of the proposed fractional sub-sampling PLL is shown in Fig. 11. The main phase lock SSL consists of an SSPD for low in-band phase noise operation. As explained in Section II, the FLL uses divider/PFD for its larger capture range to ensure a robust locking, while the loop switching controller automatically tunes gains of two loops based on the current phase error. Due to the frequency divider, the delay of the feedback path in the FLL is slightly larger than that of the SSL. An unsynchronized feedback signal causes ambiguity in terms of locking between the two loops and makes it more

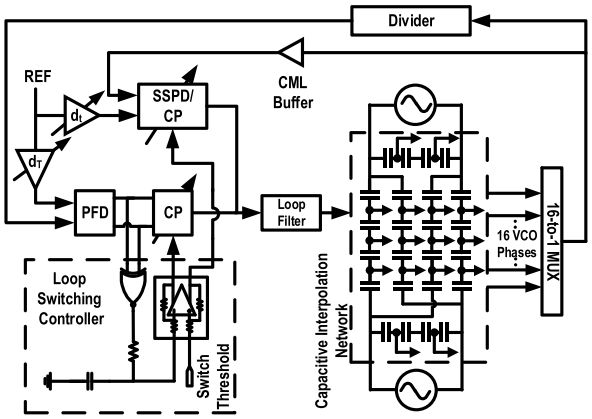

Fig. 11. Block diagram of the proposed multi-phase fractional-N SSPLL.

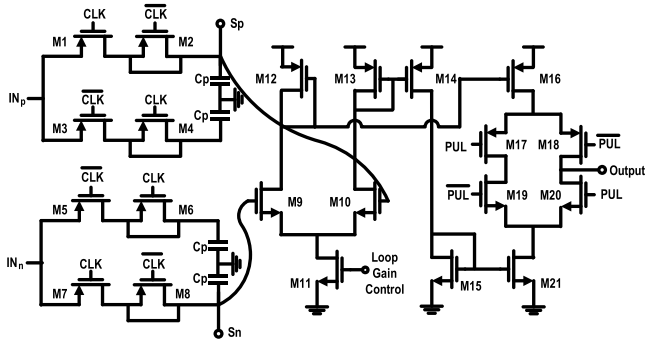

Fig. 12. Simplified schematic of the SSPD and CP.

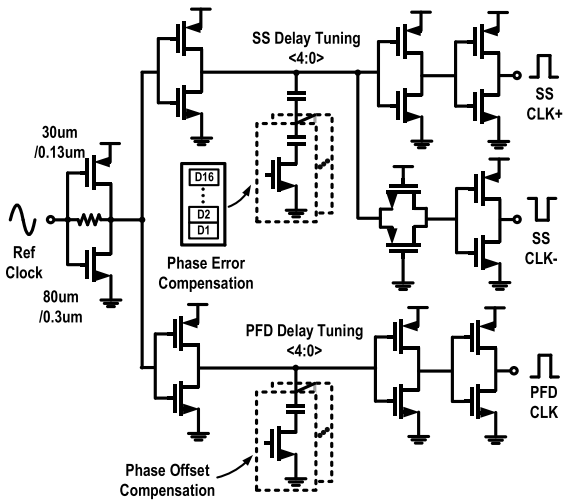

Fig. 13. Schematic of the reference buffer with tunable delays.

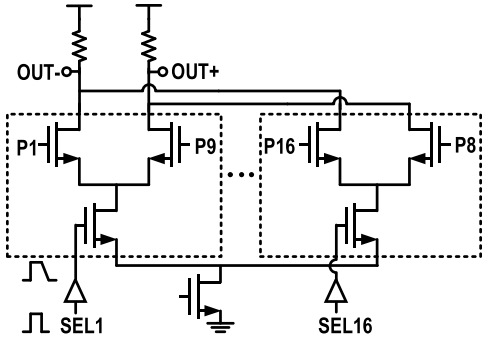

Fig. 14. Schematic of the CML multiplexer.

difficult for the loop switching controller to decide when to transit between detectors. Thus, a coarse controllable delay d_T was inserted on the reference path of the PFD to calibrate for the delay difference. Another fine controllable delay d_t is inserted in the reference clock path for the SSPD to calibrate for phase errors in interpolated VCO phases.

A. Sub-Sampling Phase Detector

As shown in Fig. 11, the multiplexer after the VCO is connected to the SSPD through a buffer. Similar to a sample and hold circuit, the SSPD consists of switches (M_1, M_7) and sampling capacitors ($C_p \sim 0.12$ pF) as shown in Fig. 12. Two shorted transistors M_2 and M_8 are connected to source and sink extra charges from the switching transistors. Their sizes are tuned to approximately half of M_1 and M_7. Two dummy paths consisting of M_3–M_6 with extra sampling capacitors are implemented to remain a constant loading on previous stages during sampling which helps reducing the reference spur [22]. The gain of the SSL is controlled through tuning the tail current in M_{11} for loop switching. In addition, the sampled voltage at S_p and S_n are also connected to pins through several stages of buffers to probe the phase error of the selected VCO phase.

B. Tunable Reference Buffer

A low-noise off-chip crystal oscillator generates a 50-MHz sinusoidal waveform with a peak magnitude of 0.6 V as the reference clock. The first stage self-biased inverter is most critical in terms of additional noise in the whole clock chain. Thus, the NMOS transistor is given a large width for higher g_m and less flicker noise, whereas the PMOS can maintain a normal size to save power as shown in Fig. 13. This also enables faster rising edge at SSCLK+ and falling edge at SSCLK− which are used as the sampling edges in the SSPD. The fine tunable delay for VCO phase error calibration on the SSPD clock path is implemented with a 5-bit binary weighted capacitor array. A series capacitor is connected between the capacitor array and the inverter output to improve the resolution. Simulation shows that a tuning range of 30 ps with a resolution around 1 ps is achieved. Likewise, the second delay on the PFD clock path for synchronizing feedback signal in two loops is also implemented with capacitor array. It is designed to cover a larger range (400 ps) with coarse resolution (20 ps). Note here the jitter requirement is relaxed since it is only used in the FLL.

C. CML Multiplexer

A current-mode-logic (CML)-based multiplexer has been implemented for phase selection as shown in Fig. 14. P_1–P_{16} denotes the 16 interpolated phases while SEL_1–SEL_{16} represents the one bit high phase selection word. Only one differential pair will be ON and conducting current (∼1 mA) at a time while the other 15 pairs will be shut down to

minimize the total loading on the interpolation network and to save power. To minimize the unbalanced loading between ON and OFF state which causes extra phase error and higher spur level in fractional-N mode, the CML-based structure has been adopted where each P_1–P_{16} nodes is loaded by two MOSFET gates, the loading variation mainly comes from different gate parasitic capacitances with different biasing currents during ON or OFF states. When the bias current is on, the gate capacitance is about 27 fF in simulation, while it is 4 fF for the OFF state. Considering an interpolation capacitance of 1.2 pF, a load capacitance variation from 4 to 27 fF creates a phase error of about 0.5°, corresponding to 0.57 ps at 2.4 GHz. This residual error can be further corrected for with the tunable delay d_t which will be discussed in detail later. In addition, even though the selected VCO phase is toggled at the reference clock rate, it will not significantly increase the reference spur since the minor loading variation due to phase switching is ignorable compared to the total loading from the interpolation network onto the VCO tank. It should be noted that if all VCO phases are used as a multi-phase clock, each phase in the interpolation network will need to be buffered, alleviating the issue of unbalanced loading.

An asymmetric buffer is inserted on the selection words to sharpen its rising edge while flatten the falling edge. This ensures a small amount of overlap between two adjacent selection bits to reduce glitches at multiplexer output during phase switching. Since all the VCO phases are available in parallel at different ports of the interpolation network, the multiplexer only needs to activate a branch to select the desired VCO phase at the reference rate. In addition, considering that the selected phase is sampled by the SSPD at the rising edge of the reference clock, while its falling edge is used for phase selection, race conditions are avoided. Large dc biasing resistors are attached to the interpolation nodes (P_1–P_{16}) for proper operation of the differential pairs. Since the resulting parallel resistance seen by the tank is fairly large (∼10 kΩ), this will not impose significant degradation on the VCO noise performance. In order to ensure a consistent propagation delay added onto each phase, a symmetric layout of the multiplexer was designed with care. Again, the residual phase error of the interpolated VCO phases can be calibrated with the tunable delay d_t on the reference path.

D. Quadrature VCO

The capacitive coupled QVCO is illustrated in Fig. 15, in which the oscillation signal of each oscillator core is coupled to the gates of the NMOS transistors in the next stage through the phase-coupling capacitor $C_{\rm qc}$. The cross-coupling capacitor $C_{\rm cc}$ path forms the $-g_m$ needed for oscillation. The combination of coupling factor, defined as $m = C_{\rm qc}/C_{\rm cc}$, source degeneration C_S and g_m can be used to tune the coupling path phase delay for minimum phase noise and phase error without multi-modal oscillation. We choose $m = 0.6$ and phase delay of 60° to achieve the optimized phase noise and phase error [23]. The I/Q outputs from the QVCO are connected to the interpolation network for multi-phase signal generation, as shown in Fig. 11.

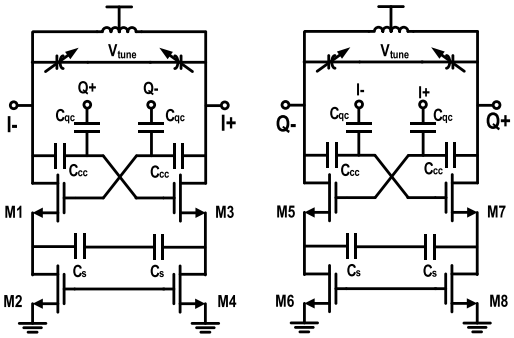

Fig. 15. Schematic of the quadrature capacitive coupled VCO.

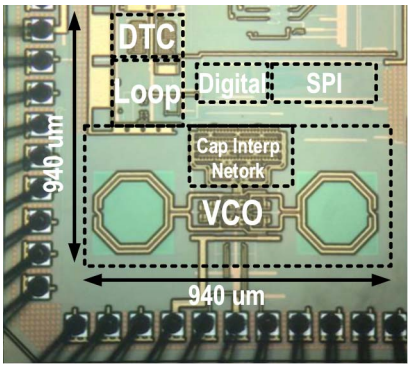

Fig. 16. Die photograph of the fractional-N SSPLL.

Capacitance value C_S in the QVCO can be used to alter the phase shift of the quadrature-coupled signals and thus can be used for phase noise optimization [23], [24]. It can be shown that both the C_S and the oscillating transistor's transconductance g_m can alter the phase shifting relationship. While g_m needs to be kept as a constant to overcome the tank loss for stable oscillation, C_S provides a tunable parameter for phase shift adjustment. As shown in [23] and [24], phase noise can be minimized by shifting the peak value of noise source current away from the zero-crossing point of the VCO output signal. Thus, C_S is adjusted to achieve the optimized phase noise at the center of oscillation frequency band.

V. Measurement Results

The proposed SSPLL is implemented in a 130-nm CMOS technology with the die photograph shown in Fig. 16. The total active area is approximately 0.43 mm^2. The system consumes 21 mW with a 1.3-V power supply. The system power breakdown is shown in Table I. Most of the power is consumed by the QVCO which delivers a phase noise of −121 and −140 dBc/Hz at 1 and 10 MHz, respectively, achieving a VCO FoM of −178 dB. The QVCO is able to tune from 2.39 to 2.46 GHz. We have not detected an effect on the VCO phase noise in measurements by turning on or off the multiplexer, thus the loading on the interpolation network has no significant degradation on the VCO performance.

The measured phase noise of the reference clock, the SSPLL, and the VCO is shown in Fig. 17. In integer-N mode, a low in-band noise floor of −120 dBc/Hz has been

TABLE I
POWER BREAKDOWN OF THE PROPOSED SSPLL

Module	Power (mW)
SSPD/CP	2
CML Buffer, Multiplexer	2
QVCO, Phase Interpolator	11
Divider, PFD	5
Ref. Buf., Tunable Delay, Digital Logics	1
Total	21

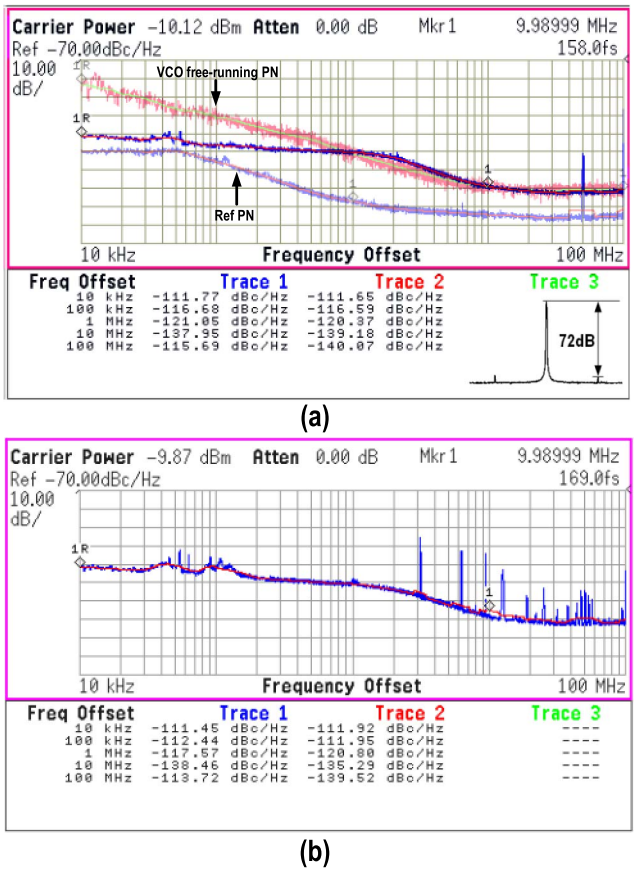

Fig. 17. (a) Measured phase noise and reference spur at 2.4 GHz in integer-N mode. (b) Measured phase noise in fractional-N mode at 2.397 GHz.

measured as expected due to using SSPD. The loop bandwidth is set to around 1.5 MHz where the in-band noise floor intersects the VCO free-running phase noise for minimal PLL total noise. An integrated jitter of 158 fs (10 kHz–10 MHz) has been measured at 2.4 GHz. With careful circuit and layout design, a very low reference spur of −72 dB has been measured. In the fractional-N mode, limited by the number of VCO phases, the finest available fractionality is 1/16 leading to a fractional offset frequency of 3.125 MHz. With an integer division ratio of 48, the synthesized frequency equals 2.397 GHz. The measured phase noise at this frequency is shown in Fig. 17, maintaining an in-band noise floor around −120 dBc/Hz with an integrated jitter of 169 fs (10 kHz–10 MHz). The measured in-band phase noise variation as the PLL switches from the FLL to the SSL is presented in Fig. 18. In the measurement, the differential input

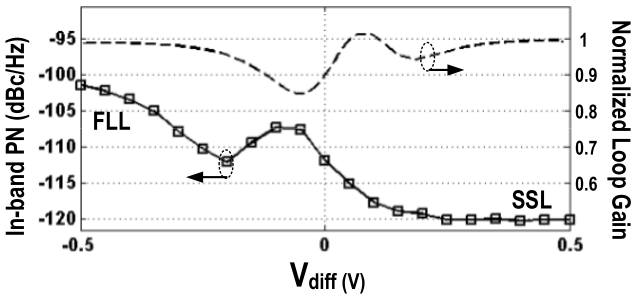

Fig. 18. Measured in-band phase noise variation in integer mode with the simulated normalized loop gain versus differential input voltage that tunes the currents to switch the loop from FLL to SSL.

voltage V_{diff} to the differential pair in the switching controller (see Fig. 3) was swept from −0.5 to 0.5 V, corresponding to a transition from the FLL to the SSL. The measured in-band phase noise improves from −102 dBc/Hz (FLL ON and SSL OFF) to −120 dBc/Hz (FLL OFF and SSL ON). Phase noise varies when the PLL transits between these two cases. Phase noise peaks around the middle point, where the simulated total loop gain drops.

Due to the phase error of interpolated VCO phases, the closest fractional spur with a fractionality of 1/16 originally was −37 dBc as shown in Fig. 19. The phase error among interpolated VCO phases can be detected with the sampled voltage S_p and S_n at the SSPD output that are wired to the pin and observed using an external oscilloscope which is elaborated in Fig. 20(b). To calibrate for the phase error, the sampling reference edge can be delayed or advanced with the fine tunable delay cell d_t in the reference path. The control bits are stored in an on-chip memory (D_1–D_{16}) and sequentially shifted onto d_t by an integrated digital logic. After calibration, the variation of the sampled voltage (S_p, S_n) for different VCO phases will be greatly reduced with lower fractional spur level. As a result, the closest fractional spur has reduced by 15 dB to −52 dBc. The loop bandwidth in this case was set to 1 MHz, so that the fractional spur has experienced slight suppression from the loop filter before and after the phase error calibration. For an automatic integrated calibration, a basic comparator will be able to provide the required information using a basic least-mean square algorithm for calibration.

The robustness of the proposed soft loop gain switching scheme has been tested as well. In the test setup, a periodic step voltage of approximately 150 mV was injected in a way similar to [7]. Through a large capacitor connected in series, the VCO supply voltage will experience spikes periodically resembling the perturbation from the digital circuits. Such interference will force the SSL out of lock and thus the relocking behavior of the PLL can be repeated and observed. The exact amount of disturbance required to drive a PLL away from lock depends on many circuit and design parameters which is difficult to model accurately. However, as a rule of thumb, as soon as the induced phase error exceeds the capture range of the SSPD (i.e., from $-\pi$ to π or half VCO period), the SSL will lose lock.

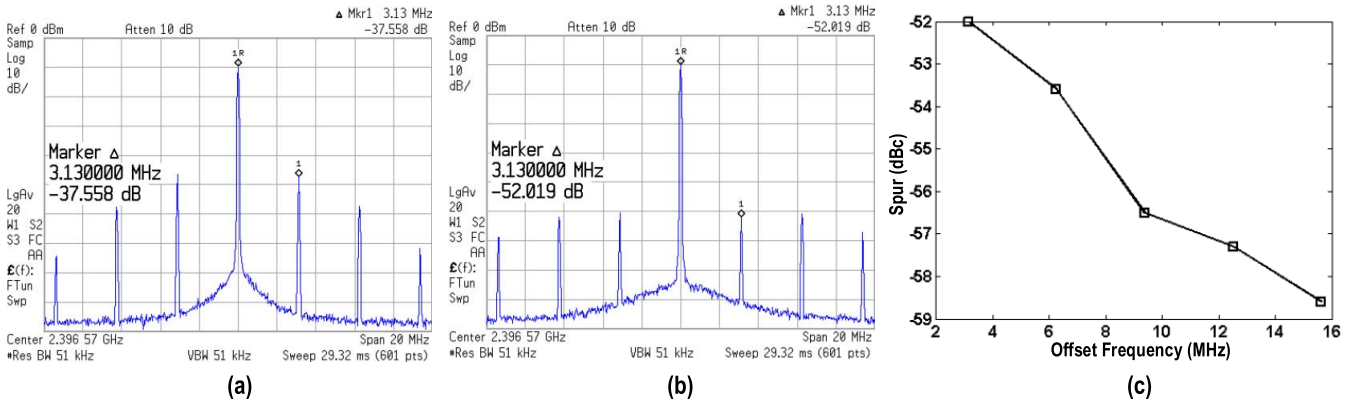

Fig. 19. Fractional spur (a) before phase error calibration, (b) after calibration, and (c) across fractional offset frequency.

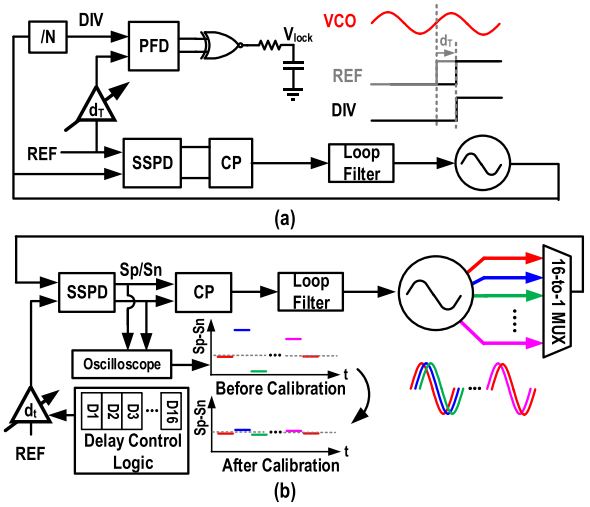

Fig. 20. Testing setup for (a) dual-loop feedback delay mismatch calibration in integer mode. (b) VCO interpolation phase error calibration in the fractional-N mode.

Two experiments were conducted with our proposed PLL. First, the switching threshold is set to $V_{\rm DD}/2$, indicating the loop starts switching as soon as phase error reaches $T_{\rm ref}/2$. Under such configuration, the proposed PLL is very similar to [4] where PFD has a dead zone of $T_{\rm ref}/2$. As shown in Fig. 21(a), after the perturbation has been injected, the lock detection instantly drops, indicating the PLL is out of lock. However, the FLL still remains inactive because the phase error at this time is not large enough to reach the switching threshold of $T_{\rm ref}/2$. Thus, the PLL needs to wait for an accumulation of phase error to activate the frequency loop and regain locking. Note that soft switching is still applied here which is different from the hard switching used in [4]. However, the issue of delayed relocking is clearly demonstrated.

In the second setup, a high switching threshold close to $V_{\rm DD}$ is applied with an estimated FLL dead zone of $\pm\pi/2$ or ± 104 ps at 2.4 GHz. This ensures that the SSL is enabled only when the phase error is within its detection range. As shown in Fig. 21(b), once the lock detection voltage drops below the switching threshold, the loop instantly switches to the FLL. The relocking time has been reduced by more than half compared to that in the first setup. After the loop is relocked, it is switched back to the SSL. Since the FLL is completely disconnected from the loop filter after phase lock, the interference and noise from the FLL can be avoided. The relocking time of this design is longer compared to [7] due to average phase error estimation (the low-pass pole from R_1 and C_1 in Fig. 3) and the off-chip op-amp used to control the loop switching behavior. Thus to provide locking robustness against high-frequency disturbance, the frequency response of the loop switching controller needs to be increased. As for the noise on the supply voltage, if the supply noise is sufficiently large to cause the phase error to trigger the loop switching, the proposed soft-switching scheme has advantage over prior art designs in relocking time.

In order to compensate for the delay mismatch between two loops, a coarse tunable delay d_T on the reference clock for the PFD is used as shown in Fig. 20(a). In this calibration, the PLL first locks to an integer frequency with the FLL and then switches to phase locking with the SSL. Note that the loop can still maintain locking after switching from the FLL to the SSL as long as the delay mismatch between two loops is smaller than one VCO period. Next, d_T is tuned based on $V_{\rm lock}$ from the FLL where larger $V_{\rm lock}$ indicates smaller phase error in the FLL. Once d_T is tuned to compensate for the extra propagation delay in the feedback path from the divider, the SSL will be locked to the reference edge while the FLL will be locked to the delayed reference edge, respectively. The phase offset calibration will be limited by the resolution of the tunable delay d_T (20 ps) which is much smaller compared to one VCO cycle ($\sim$400 ps). The measured relocking transient without loop delay calibration is shown in Fig. 22 from which we can see that the loop switches between the FLL and the SSL for multiple times, prolonging the relocking time compared to that with loop delay calibration.

A performance summary and comparison to other state-of-the-art SSPLL designs is given in Table II. The fractionality (1/16 in this paper) is limited by the number of available VCO output phases. If finer step size is needed, the interpolated VCO phases can provide the coarse tuning for fractional-N operations. Additional phase tuning can be achieved by tuning

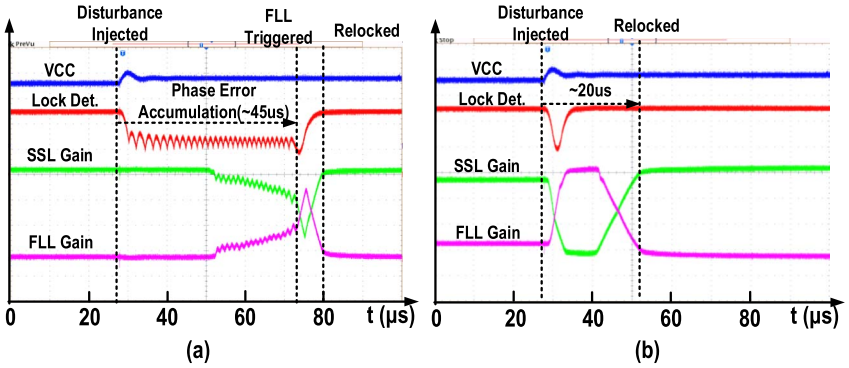

Fig. 21. Measured relocking transient behavior after a supply perturbation for (a) low switching threshold, similar to an SSPLL using FLL with large dead zone. (b) High switching threshold, demonstrating fast relock for the proposed SSPLL.

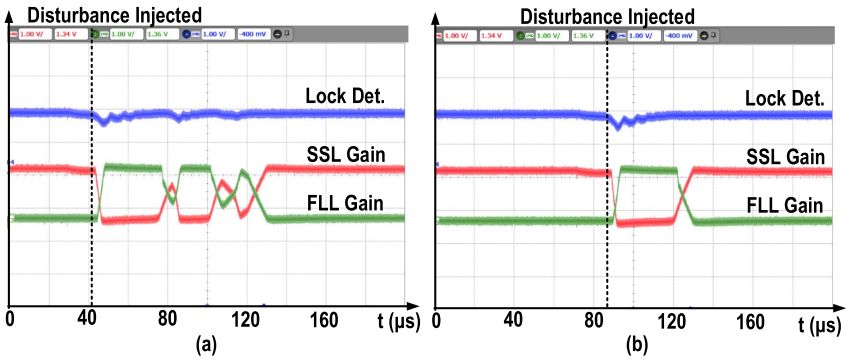

Fig. 22. Measured relocking transient behavior with (a) large phase offset between two loops and (b) minimal phase offset after loop delay mismatch calibration.

TABLE II
MEASURED SSPLL PERFORMANCES AND COMPARISONS

	Gao [22] JSSC-10 Integer-N	Hsu [7] TCAS-15 Integer-N	Chang [15] JSSC-14 Frac-N	Gao [16] ISSCC-16 Frac-N	Narayanan [19] JSSC-16 Frac-N	**This work Frac-N**
Technology (nm)	180	65	180	28	65	**130**
Ref. (MHz)	55.25	50	48	40	40	**50**
Output Freq. (GHz)	2.21	1.9-2.3	2.12~2.4	2.7-4.3	4.34-4.94	**2.39-2.46**
In-band PN (dBc/Hz)	-121	-122	-112	-	-120	**-120**
Int. RMS Jitter (fs)	300 (10kHz-100MHz)	484 (10kHz-40MHz)	266 (10kHz-30MHz)	159* (10kHz-40MHz)	133* (10kHz-10MHz)	**169* (10kHz-10MHz)**
Ref. Spur (dBc)	-80	-41	-55	-78	-70	**-72**
Frac. Spur (dBc)	-	-	-70 (3 MHz)	-54 (100 kHz)	-59 (30 kHz)	**-52 (3.125 MHz)**
Power (mW)	3.8	8.8	17.3	8.2	6.2	**21**
No. of Out. Phases	2	2	2	2	32	**16**
FoM (dB)	-244	-236	-239	-247	-250	**-242**

$FoM = 10log\left((\frac{\sigma_t}{1s})^2 \cdot \frac{Power}{1mW}\right)$, * measured in fractional mode

the delay stages on the reference path. The use of interpolated VCO phases greatly reduces the maximum delay needed on the reference path. As a result, low power and less degradation of the in-band phase noise can be achieved. The power consumption in this design is slightly larger compared to other SSPLL designs, mainly due to the use of larger feature size CMOS. Even though we only achieved a decent FoM of −242 dB, we can generate 16 VCO phases simultaneously.

VI. CONCLUSION

A fractional-N sub-sampling PLL with fast robust locking has been presented in this paper using a dual-loop structure with automatic soft loop switching. The potentially long relocking time of an SSPLL loop has been reduced without compromising the in-band phase noise. Compared with prior art SSPLLs, the proposed loop switching scheme greatly reduces the variation in loop gain and phase margins for a large range of phase error. Utilizing a QVCO with a capacitive interpolation network, the proposed SSPLL can simultaneously generate 16 VCO phases for multi-phase clock applications. Using a passive interpolation network, the proposed SSPLL can be extended from integer-N mode to fractional-N mode with little overhead in noise or power. This SSPLL design has achieved a reference spur and fractional spur of −72 and −52 dBc, respectively. The integrated jitter in integer-N and

fractional-N modes are 158 and 169 fs at 2.4 GHz, respectively, while consuming 21 mW including the power consumed by FLL.

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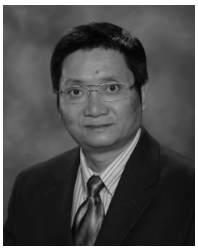

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