

A Full-Duplex Transceiver Front-End RFIC with Code-Domain Spread Spectrum Modulation For Tx Self-Interference Cancellation and In-Band Jammer Rejection

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Abstract — This paper presents a code-domain spread spectrum modulation scheme for full-duplex transceiver (TRx) front-end (FE) with the dual purposes of in-band jammer rejection and transmitter (Tx) self-interference (SI) suppression. The radio frequency (RF) code modulation scheme is applied to the inputs of the PA and the LNA. As a result, the only signal that can be decoded and restored at the receiver (Rx) is the one that was coded with the same code sequence at the Tx, while the in-band jammers, as well as the Tx SI, will be suppressed. A fully integrated on-chip duplexer with a load impedance tuner further isolates the Tx and Rx, cancels the Tx SI leakage and improved error vector magnitude (EVM) in full-duplex mode. The transceiver front-end was fabricated in a 45nm CMOS SOI process with total chip area of 2x2mm² and an active area of 1.4mm². The front-end RFIC achieves 18.8dB in-band jammer suppression and up to 51dB Tx SI suppression cross 1MHz bandwidth. Measured EVM of the receiving signal is improved from 20% to 2.5% with the code modulation on and it is further reduced to less than 1% when the on-chip duplexer is fine-tuned to achieve maximum Tx SI cancellation. The Tx maximum output power is 15dBm. The Rx consumes 50mW with LNA NF of 3.5dB to 4.2dB in the frequency range of 1.1GHz to 2.5GHz.

Keywords—*Spread spectrum code modulation; self-interference cancellation (SIC), full-duplex (FD); Radio Frequency Integrated Circuit (RFIC); duplexer; power amplifier (PA); low noise amplifier (LNA); error vector magnitude (EVM).*

I. INTRODUCTION

Integrating emerging multi-band wireless standards with small form factor into mobile devices is highly desirable, yet challenging. Conventional RF front-end requires dedicated surface acoustic wave (SAW) filters for each band to avoid interferences. The full-duplex operation is even more challenging due to simultaneous transmission and receiving (STAR) at the same frequency band. To provide required channel filtering without using SAW filters, researches on N-path filtering in the frequency domain and beam-forming in spatial domain has attracted attention recently. Moreover, self-interference cancellation (SIC) for potential STAR operation has become popular lately [1-4]. Ref. [1] demonstrated a code domain Rx using code-modulated LO signals for Tx self-interference rejection. However, the duplexer and the Tx with code modulator were not integrated. As a result, it cannot capture the actual Tx self-interference scenario in practice. In this design, we propose a fully integrated transceiver architecture for simultaneous SIC and in-band jammer rejection using a code-domain spread spectrum modulation (CSSM)

scheme. A pseudorandom code is applied on the transmitting signal on the Tx path, and by a coherent code-demodulation, only the desired signal encoded at the Tx can be decoded and restored at the Rx with the same code. Meanwhile, all other unwanted interferences such as SI leakage from the Tx to the Rx in the receiving chip and any in-band jammers from the antenna port are suppressed by spreading their energy over the code modulation bandwidth. This paper is structured as follows: Section II discusses the concept of code-domain spread spectrum modulation technique for in-band jammer and self-interference suppression; Section III presents the proposed full-duplex FE architecture with the detailed design approaches for key building blocks; Section IV provides chip measurement results followed by the conclusions given in Section V.

II. RF CODE-DOMAIN SPREAD SPECTRUM MODULATION

The code-domain spread spectrum technique modulates a narrow band signal with a bandwidth of BW_{sig} using a pseudorandom code sequence with a higher chip rate of R_{chip} with the spreading factor (SF) defined as R_{chip}/BW_{sig} . The signal is spread over a bandwidth which is SF times wider and the signal power density is thus reduced by $10\log_{10}(SF)$ dB. This approach has been widely used in baseband with digital processing. With the advance of semiconductor technology, we can now fully implement the CSSM scheme in RF domain to achieve unprecedented performance on both in-band jammer rejection and Tx SI suppression.

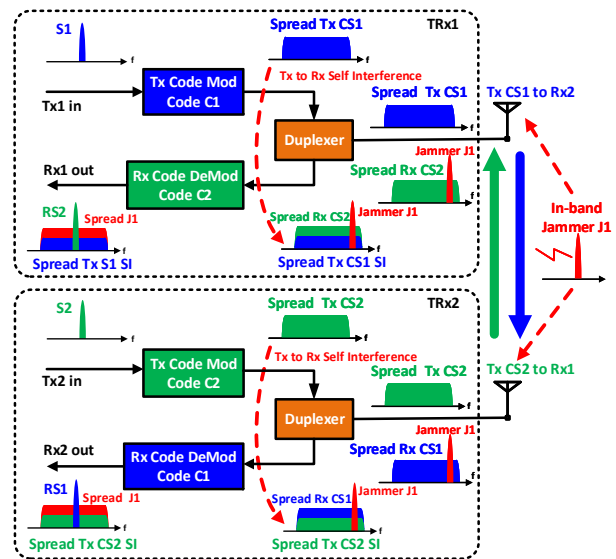


Fig. 1. Proposed RF CSSM system block diagram.

Fig. 1 illustrates simplified system block diagram with two transceiver RF front-ends communicating with each other in STAR mode. The synchronized orthogonal code sequences, C1 and C2, are applied to both Tx modulator and Rx demodulator highlighted with blue and green colors in Fig.1, respectively.

The system functions as follows: The narrowband signals, S1 and S2, are first code-modulated at the Tx and are spread to wideband signals as CS1 and CS2, respectively. Due to the Tx to Rx leakage through the duplexer and other parasitic paths, the code spread signals CS1/CS2 will be leaked to the Rx on the same chip with certain attenuation. Assuming an in-band jammer J1 is also applied at both inputs of the FEs, only the coded input signals CS1/CS2 can be demodulated and recovered to original narrowband signals RS2/RS1 by the Rx demodulators, while the jammer and Tx SI signals cannot be decoded or restored, keeping their spread spectra with the in-band power suppressed by $10\log_{10}(\text{SF})$ dB.

III. PROPOSED FULL-DUPLEX FRONT-END ARCHITECTURE

Fig. 2 shows the architecture of the proposed full-duplex transceiver front-end with code-domain spread spectrum modulation. The on-chip building blocks consist of a PA, an LNA, a load impedance tuner, and an on-chip differential duplexer.

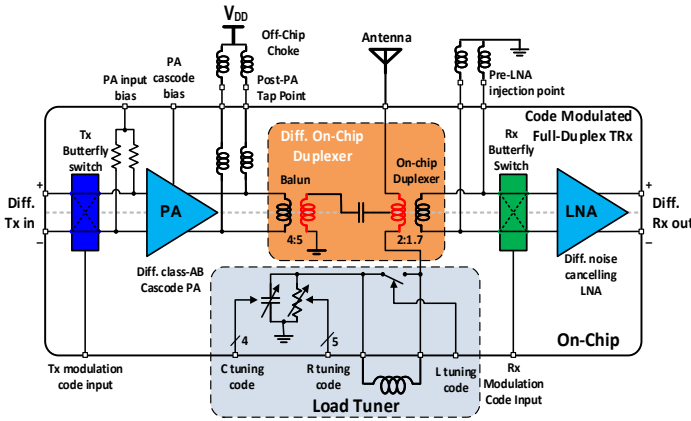


Fig. 2. Proposed CSSM full-duplex transceiver front-end architecture.

The Tx front-end contains a differential cascode PA with a butterfly switch used for code modulation. The schematic diagram of the PA is shown in Fig. 3(a). The PA core has 32 cells. The input stage transistors have a W/L ratio of $45\mu\text{m}/40\text{nm}$. The cascode transistors are thick oxide transistors to handle high output swing. With a designed 16Ω load impedance, the simulated PA core can deliver up to 30dBm saturated power (P_{SAT}) with 25dB small signal gain. The PA power supply is provided externally through on-chip and off-chip chokes. The transmission gate butterfly switches serve as a code modulator to modulate the PA input signals with inverse phases. With careful consideration among the trade-offs of PA efficiency, load impedance variation, and stability, the butterfly switches are placed at the PA input to achieve high Tx SI suppression at the cost of increased PA BW requirement. The switch sizes are determined based on the trade-off between DC current handling capability and maximizing code modulation chip rate.

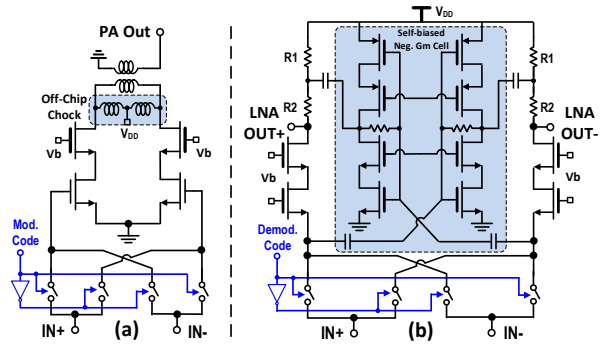


Fig. 3. Schematic diagrams of (a) differential cascode PA with code modulator, and (b) differential noise canceling LNA with code demodulator.

The schematic diagram of the differential noise canceling LNA with a code demodulation butterfly switch is shown in Fig. 3(b). To tolerate large in-band jammer and to protect the Rx front-end, i.e., the LNA, the switches for the code demodulator are placed in front of the LNA to spread the jammer spectrum before it reaches the LNA. To minimize the noise contribution, the switch on-resistance of the transmission gates is designed to be as small as possible (e.g., 5Ω) with large transistor sizes. Since the chip rate of the de-spreading codes is a few hundreds of mega chips per second (Mcps), these large switch transistors have an ignorable impact on the frequency response of the Rx. The self-biased inverter based negative gm cells cancel the noise of the CG stages, leading to improved LNA noise figure.

As shown in the Fig. 4(a), the on-chip differential duplexer consists of a balun and a transformer between the PA output and the LNA input. The balun at the PA output converts the PA differential output to a single-ended signal while transferring the PA output impedance from 16Ω to 25Ω . The transformer at the LNA input is an on-chip duplexer which provides high isolation from the single-ended PA output to the differential LNA input with a matched load [5]. It also provides desired impedance matching at the terminals of 25Ω single ended PA output port, 75Ω differential LNA input nodes, and 50Ω impedance at the antenna side. Both transformers are optimized with around 1dB loss for each path in the simulation. Compared to the differential duplexer used in [6], the proposed topology removes one hybrid transformer and results in reduced chip area and insertion loss.

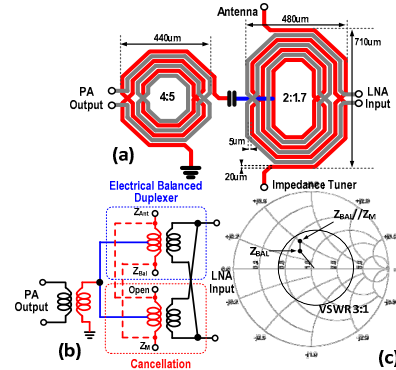


Fig. 4. On-chip duplexer configuration with equivalent circuits and load impedance tuning.

In addition to the advantages mentioned above, the proposed duplexer not only provides impedance transformation among balun, antenna, and LNA ports on the duplexer paths, but also forms an injection path for the feedforward vector signal cancellation, as shown in the equivalent circuit Fig. 4(b). The common mode signals from Tx to Rx are rejected on the duplexer path. The impedance tuner sets an impedance of Z_{BAL}/Z_M , where $Z_{BAL} = Z_{ANT}$. As a result, the remaining non-common mode Tx SI leakage signals can be removed by Z_M with the opposite phase from the cancellation injection path.

The impedance tuner consists of a 1-bit off-chip tunable series inductor, a 4-bit binary tunable shunt capacitor, and a 5-bit tunable shunt resistor. 6 stacked switches are implemented in the shunt C/R tuner to handle up to 27dBm PA output with high VSWR load conditions. During switch-off state, the switch body is biased with an external negative voltage to enhance its linearity. The proposed tuner impedance covers VSWR<3:1 range as shown in Fig. 4(c) of the Smith Chart with reasonable resolution.

IV. MEASUREMENT SETUP AND RESULTS

The proposed transceiver front-end RFIC was fabricated in a 45nm CMOS SOI technology with a total area of 2x2mm² and a core area of 1.4mm² as shown in Fig. 5. The measurement results in Fig. 6 show the Tx SI cancellation performance with various tuner code settings for the duplexer crosses the frequency range of 1.25GHz~1.7GHz. The R tuning as shown in Fig. 2 mainly determines the notch response of the Tx SI cancellation. Once R code is chosen, C tuning code sets the notch frequencies and provides around 25dB extra cancellation with 40MHz bandwidth cross the frequency tuning range of 1.4GHz~1.63GHz.

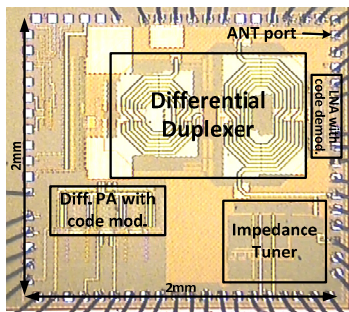


Fig. 5. Die photo of the proposed full-duplex transceiver front-end.

Fig. 7 shows the measured Tx SI spectra at the LNA input with 1MHz Tx BW at 1.452GHz. When the tuner is set to high impedance and the code modulation is off, the Tx SI presented at the LNA input is -36dBm/100kHz. With a 10Mcps code modulation, the Tx SI is suppressed by around 10dB. Together with the optimally tuned on-chip duplexer, extra 41dB suppression can be achieved to reach a total of 51dB suppression against the Tx SI.

Fig. 8 gives the measured EVM for a 1MHz QPSK signal transmitting from Tx2 to Rx1 with various settings. For this test, the Tx1 SI power is swept while the received power from Tx2 is fixed. The relative Tx1 SI power in the plot is calculated at LNA input of Rx1, divided by the receiving signal power at the same point, under the condition that code modulation is off

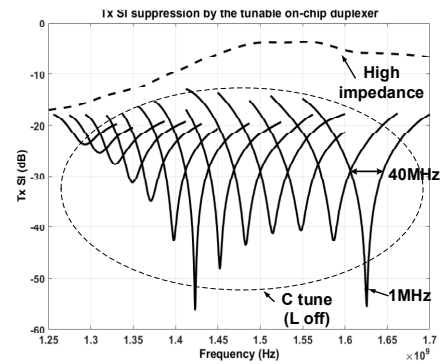


Fig. 6. Measured on-chip duplexer notch response with different impedance tuner code.

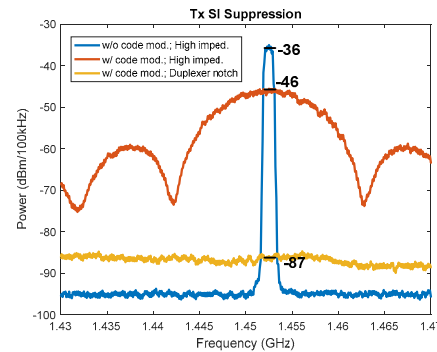


Fig. 7. Measured spectrum comparison for Tx SI suppression.

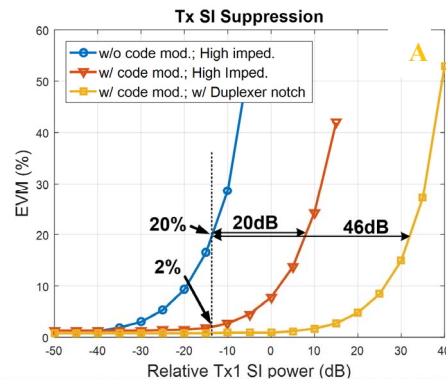


Fig. 8. Measured EVM of QPSK transmission versus Tx SI power. Received signal power is -30dBm at antenna port and test point A corresponds to Tx power of +2dBm at antenna port.

and the duplexer is not optimally tuned. Taking 20% EVM as a reference point, Tx SI signal can be suppressed by 20dB with 100Mcps code modulation, which is in good agreement with the theoretical factor of $10\log_{10}(SF)$ dB. Total 46dB Tx SI suppression can be achieved with a properly-tuned duplexer and 100Mcps code modulation. At the same Tx1 power, measured EVM is reduced to 2% with 100Mcps code modulation, and is further improved to less than 1% with an optimally tuned duplexer.

Fig. 9 presents a comparison of the measured constellations for 64-QAM modulated data transmission with 1MHz signal BW without and with 100Mcps code modulation and the optimally tuned duplexer for Tx SI suppression. The EVM is measured at both LNA input and output to eliminate LNA's

linearity limit. The EVM at LNA output is improved from 8.8% to 2.1% with CSSM and optimal duplexer tuning. Note that the test equipment may lose lock, therefore its reading may not be accurate, when EVM is larger than 8%.

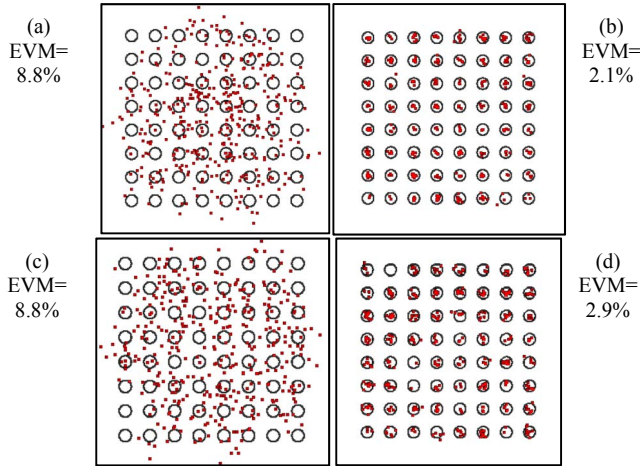


Fig. 9. Measured EVM at LNA output and input for 64-QAM transmissions. (a) and (b) EVM at LNA output with Tx and Rx power of -15dBm at antenna; (c) and (d) EVM at LNA input with Tx power of 0dBm and Rx power of -5dBm at antenna; (a) and (c) CSSM off and duplexer not optimally tuned; (b) and (d) CSSM on and duplexer optimally tuned.

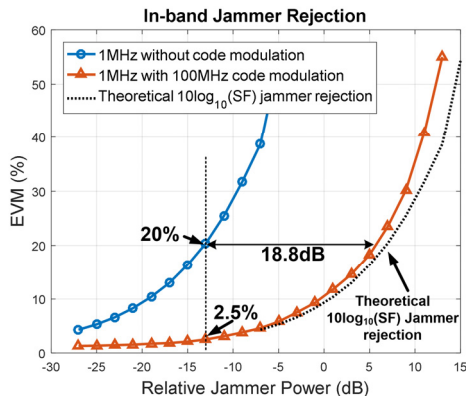


Fig. 10. Measured EVM for in-band jammer rejection.

Fig. 10 demonstrates the in-band jammer rejection by showing EVM of a 1MHz signal transmission with various in-band jammer power level and a fixed Tx2 power. The labeled relative jammer power is referenced to the receiving signal power at the Rx1 LNA input for the case without code modulation. Both Tx2 and Rx1 are code modulated with the same C1 code at 100Mcps chip rate. Taking the 20% EVM as the reference point, 18.8dB higher in-band jammer power can be tolerated for the 1MHz signal transmission when a 100Mcps code modulation is applied.

Table I summarizes the transceiver FE performances in comparison with the recently published state-of-the-art full-duplex TRx. This proposed fully integrated TRx FE presents a design with both Tx SI suppression and in-band jammer rejection capability. It achieves as high as 51dB SIC, 18.8dB in-band jammer rejection, large Tx port power handling (+15dBm), and low LNA noise figure (3.5~4.2dB) with low power consumption.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART FULL-DUPLEX TRX DESIGNS.

	JSSC 2015[2]	ISSCC 2016 [3]	ISSCC 2017 [4]	This work
Architecture	Mixer-first TRX with Active Baseband Duplexing	RX with integrated magnetic-free N-path-filter-based circulator and BB SIC	Magnetic-free n-path-filter-based circulator-receiver with on-chip balance network	TRx with tunable differential duplexer and code modulation
RX Freq. Range	0.1-1.5GHz	0.6-0.8GHz	0.61-0.975GHz	1.1-2.5GHz
RX Gain	53dB	42dB	28dB	15dB
RX Noise Figure *	5-8dB	8.4dB	6.3dB	3.5-4.2dB **
RX Power	43-56mW(incl. TX)	100mW	72mW	50mW
Integrated Antenna Interface	Yes (baseband duplexing LNA)	Yes (magnetic-free non-reciprocal circulator)	Yes (magnetic-free non-reciprocal circulator)	Yes (tunable differential duplexer)
Integrated SI Suppression Domains	Analog BB	RF+Analog BB	RF	RF
SI suppression by code modulation	N/A	N/A	N/A	20dB SIC across 1MHz BW
Amount of Integrated SI suppression	33dB across 300kHz	42dB SIC across 12MHz BW	40dB SIC across 20MHz BW	51dB SIC across 1MHz BW
Overall TX Port Power Handling	-17.3dBm	-7dBm	+8dBm	+15dBm
In-band Jammer Rejection	N/A	N/A	N/A	18.8dB across 1MHz BW
Code Modulation Rate	N/A	N/A	N/A	100MHz
Technology	65nm CMOS	65nm CMOS	65nm CMOS	45nm CMOS
Active Area	1.5mm ²	1.4mm ²	0.94mm ²	1.4mm ²

* NF measured in half-duplexing mode. ** NF measured from LNA input.

V. CONCLUSIONS

This paper proposed an RF code-domain spread spectrum modulation scheme used in full-duplex transceiver front-end for in-band jammer rejection and transmitter self-interference suppression. This design achieves superior performance of in-band jammer rejection and Tx self-interference suppression of 18.8dB and 51dB across the 1MHz bandwidth, respectively. The received signal EVM is improved from 20% to 2.5% with code modulation and is further improved to less than 1% with the optimally tuned on-chip duplexer. Tx outputs and handles +15dBm power. Rx consumes 50mW with LNA NF of 3.5dB to 4.2dB from Rx range of 1.1GHz to 2.5GHz, respectively. To our best knowledge, this is the first reported fully integrated TRx FE with RF code domain signal processing to provide simultaneous in-band jammer rejection and Tx self-interference suppression for full-duplex STAR operation.

VI. ACKNOWLEDGEMENT

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REFERENCES

- [1] A. Agrawal and A. Natarajan, "A 0.3 GHz to 1.4 GHz N-path mixer-based code-domain RX with TX self-interference rejection," *RFIC Symposium*, pp. 272-275, Honolulu, 2017.
- [2] D. Yang, *et al.*, "A Wideband Highly Integrated and Widely Tunable Transceiver for In-Band Full-Duplex Communication," *IEEE J. Solid-State Circuits*, vol. 50, no. 5, pp. 1189- 1202, May. 2015.
- [3] J. Zhou, *et al.*, "Receiver with Integrated Magnetic-Free N-Path-Filter-Based Non-Reciprocal Circulator and Baseband Self-Interference Cancellation for Full- Duplex Wireless," *ISSCC Digest*, pp. 178-180, Feb. 2016.
- [4] N. Reiskarimian, *et al.*, "Highly-Linear Integrated Magnetic-Free Circulator- Receiver for Full-Duplex Wireless," *ISSCC Digest*, pp. 316-317, Feb. 2017.
- [5] M. Mikhemar, H. Darabi and A.A. Abidi, "A Multiband RF Antenna Duplexer on CMOS: Design and Performance," *IEEE J. Solid-State Circuits*, vol.48, no.9, pp. 2067-2077, Sept. 2013.
- [6] S. H. Abdelhalem, *et al.*, "A Tunable Differential Duplexer in 90nm CMOS", *RFIC Symposium*, pp. 101-104, Montreal, 2012.