A Multi-Phase Coupled Oscillator Using Dual-Tank Magnetic Coupling Technique

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***Abstract*—This paper presents a novel coupled-oscillator RFIC for multi-phase clock generation. The design achieves low phase noise while maintaining strong coupling among oscillator cores. The proposed transformer-based dual-tank topology forms a loop of coupling path for enhanced multi-phase coupling. The phase noise optimization is accomplished by leveraging the dual-tank and the adaptive-biasing feedback techniques, while the transformers facilitate strong magnetic coupling among oscillator cores. Full electro-magnetic (EM) modeling of all transformers and the passive interconnecting routes has been performed using EMX in order to ensure that simulated performance reflects measurement environment. The prototype of the proposed circuit with 8 phases is implemented in a 65nm CMOS RF SOI technology. The measured phase noise is -124.3 dBc/Hz @ 1MHz offset from 2.41 GHz with 7mw power consumption for each core, and the operating frequency can be digitally tuned from 1.81 GHz to 2.41 GHz.**

Keywords—multi-phase, coupled oscillators, transformer, dual-tank

I. INTRODUCTION

Low-noise multi-phase clock generation is gaining popularity due to its wide applications in numerous critical radio frequency (RF) blocks such as the N-path filter, the sub-harmonic mixer, the analog-to-digital converter (ADC), and the clock data recovery (CDR). Current approaches to multi-phase clock generation such as the ring oscillator, the poly-phase filter, and the frequency divider are ruled out as a viable candidate due to their own set of problems such as poor phase noise, narrow bandwidth, or the need for a high frequency source. The coupled-oscillator topology as the best candidate for multi-phase clock generation has been discussed and improved over the past decade due to its two intrinsic advantages [1]: 1) the number of phases can be easily expanded by adding an extra oscillator core to the loop; 2) the phase noise, regardless of the degradation caused by the coupling technique, can be improved theoretically by a factor of $10\log_{10} N$, where N is the number of coupled oscillator cores.

Recent publications have focused on three major types of coupling strategies: active coupling, capacitive coupling, and magnetic coupling. The active coupling utilizes additional transistors for coupling; as a result, it suffers from extra noise and increased power consumption introduced by these active devices [2]. The capacitive coupling, on the other hand, uses additional capacitors for coupling, and can couple

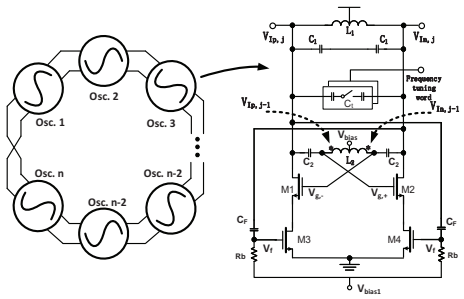


Fig. 1. The proposed multi-phase coupled-oscillator topology and its unit oscillator core.

the oscillator cores with less noise and power penalty [3]. However, an ultra-strong coupling strength often comes with degraded phase noise. Ultimately, magnetic coupling is realized using a transformer, which is part of the oscillator circuit and thus does not need additional die area. However, transformer design requires a careful EM modeling to ensure close correlation between simulation and measurement. Another advantage of the transformer-based magnetic coupling is that the coupling path is embedded in the transformer itself, unlike the other two coupling mechanisms, where coupling-related routing is required among oscillator cores. These routings will increase implementation challenges as the number of oscillator cores increases, as a symmetric layout is necessary in order to ensure an equal coupling strength among cores.

This paper presents a novel magnetic coupling topology, which transforms the conventional dual-tank oscillator structure to one based on the transformer. With the adaptive biasing feedback, low phase noise and strong coupling strength can be achieved simultaneously. Furthermore, the proposed transformer-based oscillator topology facilitates a symmetric floorplan. Additionally, using the EM modeling tool, all passive routing is carefully modified in order to minimize unnecessary coupling.

II. THE PROPOSED TRANSFORMER-BASED OSCILLATOR ARCHITECTURE

A. Unit Oscillator Core

As shown in Fig. 1, the proposed unit oscillator core adopts the dual-tank and the adaptive biasing feedback techniques,

where *j* is the sequence number of the oscillator core. L_1 and L_2 are differential inductors, and, together with C_1 and C_2, form the dual-tank structure. Unlike the conventional single-NMOS transistor current tail, two separate NMOS transistors (i.e., M_3 and M_4) provide the bias current, and facilitate the implementation of the feedback in the proposed oscillator. C_F and R_b provide the feedback path for adaptive biasing, which passes the AC voltage from the output to the gate of M_3/M_4. C_t represents the 3-bit digitally-controlled capacitor array for frequency tuning. The transformer is composed of coils L_1 and L_2, where coil L_1 is from the previous adjacent core and coil L_2 is from the current core; therefore, the output of the previous core can couple its signal to the gates of the cross-coupled transistors of the next oscillator core.

B. Coupling Mechanism

The complete schematic diagram of the proposed 8-phase oscillator is shown in Fig. 2, where the dashed lines represent the coupling paths among the transformers. Unlike current transformer-based structures [4], signal is drawn from the drain of the cross-coupled transistors and coupled to the gate of the same transistors in the next core; forming the coupling path. This way, the voltage at the gate of the cross-coupled transistor is the superposition of two voltages: 1) the one coming from the output of the same core; and, 2) that from the output of the adjacent core.

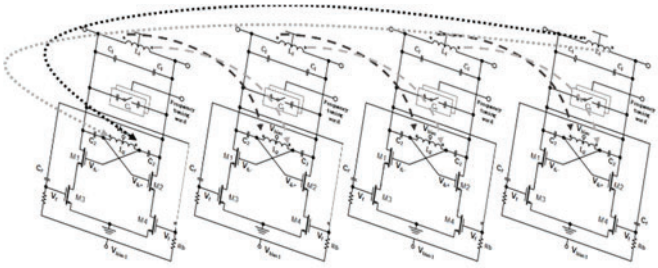


Fig. 2. The schematic diagram of the proposed 8-phase oscillator.

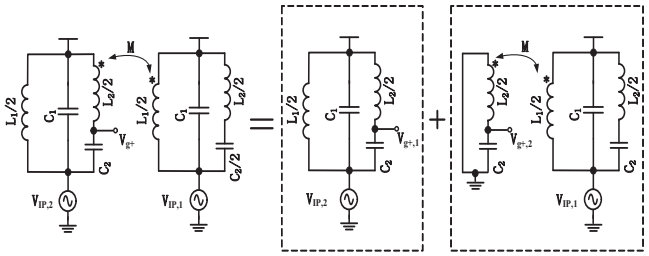


Fig. 3. The simplified equivalent model of coupling paths.

Fig. 3 illustrates the signal flow in the simplified circuit, where V_{g+} is the gate voltage and only one side of the cross-coupled network is shown. $V_{g+,1}$ is that part of the gate voltage that comes from the output of the same core, and its major role is to provide the oscillation signal. $V_{g+,2}$ is the other part of the gate voltage that comes from the output of the adjacent core, and contributes to both coupling and oscillation. Assuming that the output sources $V_{IP,1}$ and $V_{IP,2}$ are independent, the two parts of the gate voltage can be separated and expressed as follows:

$$V_{g+,1} = V_{IP,2} * s^2 L_2/(2 + s^2 L_2 C_2) \quad (1)$$

$$V_{g+,2} = V_{IP,1} * k\sqrt{L_2/L_1} \quad (2)$$

where *k* is the coupling factor of the transformer. The proposed structure is unlike the conventional dual-tank configuration, where the ratio of L_2/L_1 is small and the ratio of the gate voltage of the cross-coupled transistor over that of its drain is large. In order to ensure strong coupling, the ratio of L_2/L_1 must be sufficiently large in the proposed architecture. As a result, the impedance of $L_2/2$ dominates that of C_2. Therefore, $V_{g+,1} \approx V_{IP,2}$, and V_{g+} is dominated by $V_{g+,2}$. In addition, the transient waveforms are plotted in Fig. 4, and the coupling strength, *m*, is equal to

$$m = s^2 k(2 + s^2 L_2 C_2)/\sqrt{L_2 L_1} \approx k\sqrt{L_2/L_1}\,. \quad (3)$$

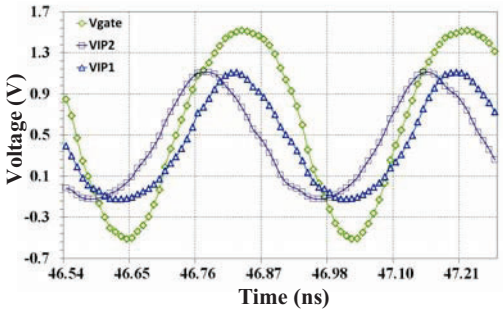


Fig. 4. Simulated plots of the transient waveforms of V_{IP1}, V_{IP2}, and Vg+.

C. Phase Noise Optimizaion

In the proposed structure, phase noise is optimized using two techniques: 1) adaptive biasing; and, 2) the dual tank. The first technique is implemented by feeding back the signal from the gate of $M_{1/2}$ to the gate of $M_{3/4}$. Since $M_{3/4}$ adjust their currents to follow the output signal, $M_{1/2}$ will be forced to switch faster, and spend less time in the equilibrium, where noise is the highest. Therefore, the adaptive biasing feedback increases the bias current when it is needed in order to expedite the transition and suppress the noise. In addition, by using two transistors for biasing, the second harmonic, which is present in the common node of the structure biased with a single transistor, is eliminated, and the flicker noise is significantly suppressed.

The conventional dual-tank structure optimizes the phase noise by increasing the voltage swing at the gate and thus reducing the operation time in the triode region, where the output impedance of the cross-coupled transistors is the smallest and the Q of the load is degraded. A similar optimization can be performed in the proposed transformer-based architecture, but in a much different manner. One major functional difference between the transformer-based and the conventional dual-tank oscillator is that the former affects both the coupling strength and the voltage swing at the gates of the cross-coupled transistors at the same time. Therefore, the trade-off between the phase noise and the coupling strength does not follow the same convention as most coupled oscillators, where decreasing the coupling strength always leads to better phase

noise. In order to illustrate this matter clearly, the simulated phase noise versus coupling factor, k, of the transformer is shown in Fig. 5, where AC gain is the ratio of $V_{IP,1}$ over $V_{g+,2}$, while constant current is maintained for different k values. When the coupling factor changes from -0.35 to -0.5, the coupling strength increases, and the phase noise improves. That is because when k is relatively small, phase noise still benefits from the reduced operation time in the triode region. By further increasing the coupling factor, phase noise starts to degrade due to the injection of the coupling signal at zero-crossing of the oscillation waveform, which is also the case for most prior-art coupled oscillators without phase shifting on the coupling paths.

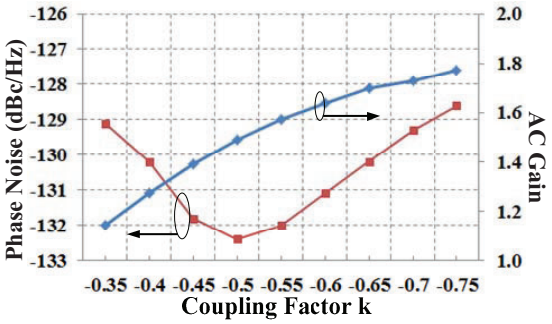
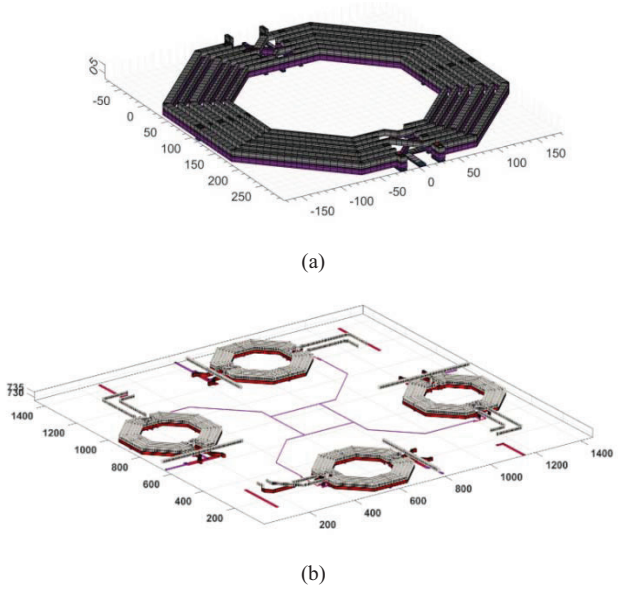


Fig. 5. Simulated phase noise and ac voltage gain versus the coupling factor of the transformer.



(a)

(b)

Fig. 6. (a) The 3D view of the transformer. (b) the 3D view of the transformers and the passive routings.

D. Transformer and Passive Design

In order to obtain the strong coupling factor k, a transformer with interleaved turns is used as shown in Fig. 6(a). The coils of the transformer are made by stacking two top metals in order to minimize the DC resistance and achieve the best possible quality factor. Simulated plots of the transformer performance are shown in Fig. 7, where L_1 and L_2 are 2.5nH and 7.4nH, respectively at 2.4 GHz.

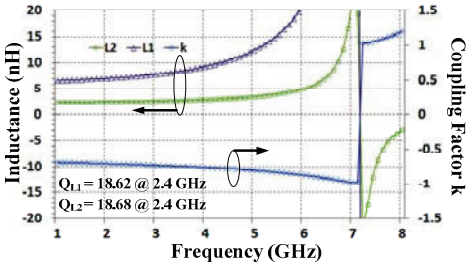


Fig. 7. Simulated plots of the transformer performance.

In addition, in order to capture the capacitive and magnetic coupling among all critical routings in the layout, the EM model is created using *EMX 5.2 from Integrand Software, Inc.*. As shown in Fig.6(b), the 37-port EM model includes the transformers, the routings among all oscillator cores, the routings of control signals, the power supply, and ground traces. The reference ground plane is at the substrate of the die, and the mesh and the thickness parameters of the EM simulation are set to 1. Therefore, undesired coupling among routings can be avoided during layout design. In addition, the oscillation frequency is accurately predicted; e.g., the difference between simulated and measured frequency is only 80MHz.

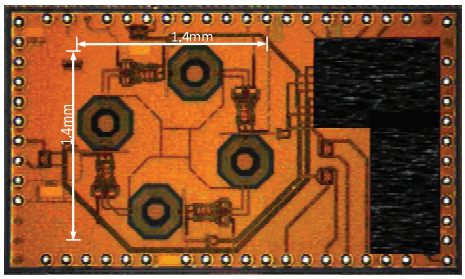


Fig. 8. The die photo of the proposed multi-phase coupled-oscillator RFIC.

III. Measurement

The prototype 8-phase oscillator is fabricated in a 65nm CMOS RF SOI process. The die photo is shown in Fig. 8. The core area of the proposed coupled oscillator circuit is $1.4 \times 1.4\ mm^2$. In order to make the connections among oscillator cores more symmetric, a circular floor plan is adopted by taking advantage of the transformers. Table I summarizes the performance of this work and provides comparison with state-of-the-art multi-phase oscillator designs. The equations used to evaluate the figure-of-merit FoM and $FoM_{\text{per phase}}$ are provided below

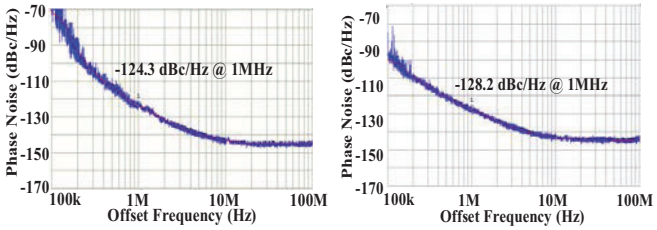
$$FoM = 10log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1mW}{P}\right] - \mathcal{L}(\Delta f) \quad (4)$$

$$FoM_{Per\ phase} = 10log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1mW}{P} N\right] - \mathcal{L}(\Delta f) \quad (5)$$

where N is the number of phases.

A. Measured Phase Noise

The phase noise is measured using an Agilent E4440 spectrum analyzer with phase noise option. Fig. 9 illustrates measured phase noise of –124.3 dBc/Hz and -128.2 dBc/Hz @ 1MHz offset from 2.41GHz with power consumption of 28mW and 60mW, respectively. Since a three-bit capacitor array is implemented for frequency tuning, the operating frequency can be digitally tuned from 1.815GHz to 2.42GHz. In addition, measured phase noise versus the operating frequency is shown in Fig. 10 under three different DC operating points for each core: 1) V=0.7V and I=5mA; 2) V=1V and I=7mA; 3) V=1.5V and I=10mA.



a) b)

Fig. 9. Measured phase noise: a) total power comsumption is 28mW, b) total power comsumption is 60mW.

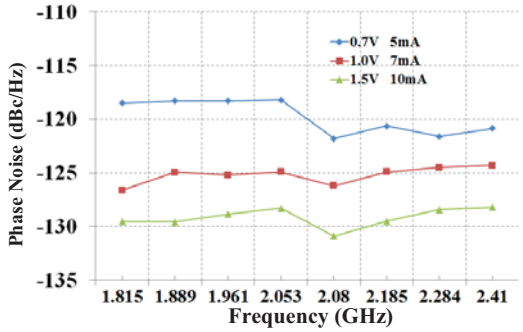


Fig. 10. Measured phase noise @ 1MHz offset versus the operating frequencies under different DC bias currents.

B. Measured Output Waveforms

The output waveforms of the proposed 8-phase oscillator are measured by a Rohde & Schwarz RTO scope, which supports simultaneous four-channel measurement. Fig. 11 exhibits four measured phases, out of eight phases, of the four-core oscillator, where the other four phases are the differential counterparts and not shown.

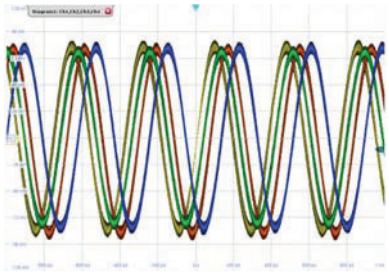


Fig. 11. Measured multi-phase output waveforms.

IV. Conclusions

This paper presented a novel transformer-based architecture for multi-phase clock generation. The concept of the prototype circuit is proven by both simulation and measurement. EM modeling was utilized to ensure proper coupling among routings, thus improving the correlation between simulation and measurement. The highest measured FoM is 187 dBc/Hz at 1MHz offset from the carrier, and the frequency range can be digitally tuned from 1.815 GHz to 2.41 GHz with 8 steps.

TABLE I. Performance Summary and Comparison

Ref.	Performance Metrics						
	Process	*Freq (GHz)*	*P.N (dBc/Hz) @ 1MHz*	*Power (mW)*	*FoM*	*No. of Phases*	*FoM Per Phase*
			-120.1	14	176.3	8	185.3
			-124.3	28	177.5	8	186.6
			-128.2	60	178	8	187
[5]	65nm CMOS	4.07	-136	126	188	4	194
[6]	65nm CMOS	3.8	-123.7	7	185	4	191
[7]	0.18µm CMOS	1.1	-128	20	180.1	4	186.1
[8]	0.13µm CMOS	4.9	-112	3.2	180.8	4	186.8

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