A 14-Bit, 1-ps Resolution, Two-Step Ring and 2D Vernier TDC in 130nm CMOS Technology

Hechen Wang and Fa Foster Dai
Dept. of Electrical and Computer Eng., Auburn University, Auburn, AL 36849

***Abstract*— This paper presents a time-to-digital (TDC) design with large detectable range and fine resolution, combining a ring TDC with a 2-dimentional (2D) Vernier TDC. The detectable range has been greatly increased to 14 bits with the ring structure. A 1-ps resolution was achieving with 2D Vernier architecture. Utilizing the 2nd order ΔΣ modulators (SDM) and a 2D spiral arbiter array, the proposed TDC greatly mitigates the quantization errors introduced by digitally controlled delay cells and the intrinsic arbiter line folding errors associated with the 2D array topology. The measured maximum DNL/INL are 0.41/0.79ps with ΔΣ linearization. A prototype TDC chip fabricated in 130nm CMOS technology achieves a conversion rate of 10 MS/s while consumes 2.4 mW power.**

***Keywords*— TDC, resolution, detectable range, linearization, INL, DNL, ΔΣ modulation, quantization error.**

I. Introduction

Digital phase locked loop (DPLL) has been intensively studied nowadays, and there are many different DPLL architecture. Time-to-digital converter (TDC) plays a significant role, among all kinds of DPLL variants. Since the resolution of the TDC is approaching 1-ps level and the nonlinearity has been greatly suppressed with newly developed techniques [1-2], DPLL's main performance, in-band phase noise and fractional spur level, is now competitive with traditional analog PLLs. Overtaking analog PLL is not the reason why people keep focusing on DPLLs. It is because DPLL is more compatible with digital controlled system and is suitable for direct phase and frequency modulation. Unlike synthesizer designs, DPLL based modulator demands TDCs with large detectable range and excellent linearity [3-4]. Therefore, it's highly desirable to develop a TDC that can achieve large detectable range, fine resolution and good linearity simultaneously.

In this paper, we presented a TDC design with a large detectable range of 14 bits, fine resolution of 1ps and excellent differential linearity (DNL)/integral linearity (INL) of 0.41ps/0.79ps owing to the following novel techniques: (i) a combined ring and 2D Vernier TDC is used to 14 bits detectable range and 1ps resolution; (ii) a 2nd order ΔΣ modulator (SDM) is adopted to mitigates the quantization errors introduced by the delay cell nonlinearity; (iii) the 2D arbiter comparison path is arranged in a spiral form in order to improve its INL; (iv) an additional 2nd order SDM is used to randomize the arbiter line folding errors associated with the 2-D arbiter array topology. Traditionally, technologies with small feature size are preferred for mixed-signal designs such as TDC design to achieve better performance and power efficiency. However, after five decades, it seems that the Moore's low has come to a crossroads. As a result, there is an increased benefit to focus on circuit innovations rather than simply pursue the use of technologies with small feature size to further improve the circuit performance figure of merit (FoM). In this work, by using a large feature size technology (130nm CMOS) we presented a TDC achieving improved performance comparing to state-of-art TDC designs using small feature size processes.

II. Proposed TDC Architecture

Resolution and detectable range are two critical and contra-dictionary parameters for TDC designs. It is challenge to achieve fine resolution and large range simultaneously. Vernier based TDCs achieve good resolution, yet with limited range [5]. Ring based TDCs have a wide detectable range, while its resolution and linearity are imperfect [6]. We presented a TDC in [2], which achieved 1.25ps resolution and 0.4ps nonlinearity by using spiral 2D comparator array and SDM linearization techniques. However, its 8 bits range is not able to support DPLLs with output frequency less than 3GHz.

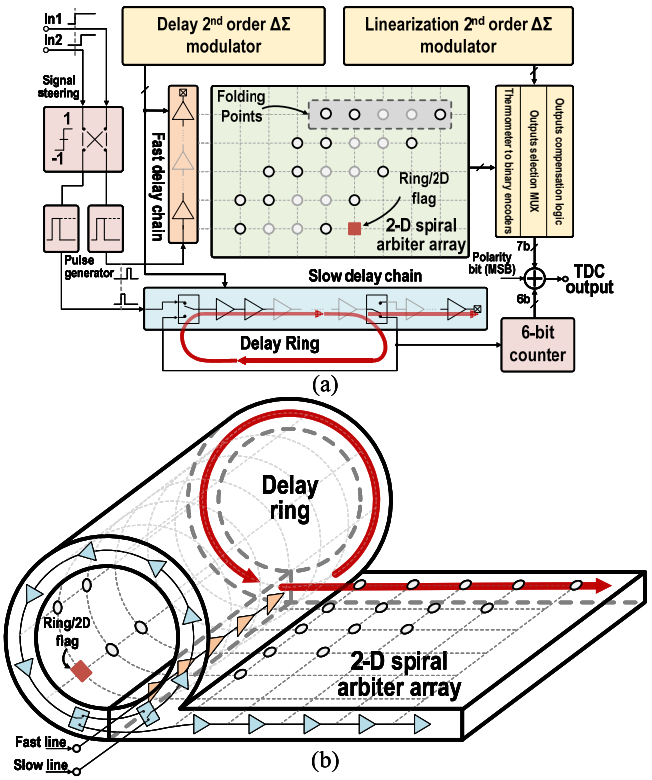

Fig. 1. (a) Proposed 2D spiral Vernier ring TDC with 2nd order ΣΔ linearization, and (b) ring/2D structure collaboration illustration.

In order to expand the detectable range while not panelizing resolution and linearity, we proposed a taped 2D Vernier ring TDC, shown in Fig. 1, with 2nd order ΣΔ linearization techniques and a spiral 2D arbiter array to achieve large range, fine resolution and improved linearity simultaneously. The TDC contains two delay lines and a 2D arbiter array formed a 2D Vernier TDC. The ring TDC is built with part of the slow delay chain. The comparison signals are fed into a steering block, which directs the leading and lagging signals to the slow delay line and the fast delay line, respectively. There are two switches in the slow delay line. The first switch is connected to the input signal node at beginning of each conversion, and is switched to the loop after the signal appears. The second switch is controlled by a "ring/2D flag". The time interval is measured by the ring TDC first. Once the interval residue falls into the 2D Vernier TDC range, it triggers the flag to activate the 2D Vernier TDC.

Once a delay line is formed into an end to end delay ring, a pulse generator is required to convert input edge signal into a pulse signal. The reason is shown in Fig. 2. An edge signal is able to propagate in a delay line. However, when propagating in a delay ring, the state of the cells need to be reset after the signal passes. Otherwise, there will be no more transactions when signal comes back after the first lap. The falling edge of the pulse signal resets the delay cell.

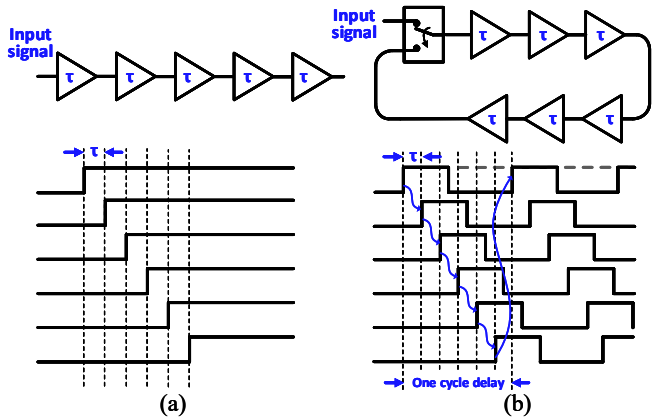

Fig. 2. Signal propagation difference between (a) straight delay line and (b) end to end connected delay ring.

To ensure a continuous transfer curve between the ring TDC and 2D Vernier TDC, only first 6 delay cells in the slow delay chain are used to form the delay ring. In a 2D Vernier TDC, the temporal delay and number of delay cells need to fulfill

$$n\,(\tau_S - \tau_F) = \tau_S, \qquad (1)$$

where τ_S and τ_F represent the temporal delays of a single stage in slow chain and fast chain, respectively; and n is the number of delay cells in the fast delay chain. The resolution of 2D Vernier TDC is thus given by $\tau_S - \tau_F$. Unit temporal delay τ_S and τ_F are affected by mismatches, which can be analyzed with Monte Carlo simulations. Table I shows the simulated temporal delays under different number of delay cells. If the delay is too small, the mismatch is relatively large. In order to minimize mismatches, larger delay is desirable. However, as shown in (1), the number of delay cells will increase when unit delay is enlarged, which also leads to larger mismatch. According to the simulations, we choose the unit delay τ_S / τ_F as 25ps/26ps.

TABLE I. MONTE CARLO COMPARISON OF UNIT DELAY AND NUMBER OF DELAY CELLS

Option	1	2	3	4
τ_S / τ_F [ps]	15/16	25/26	35/36	45/46
Delay cell number **n**	16	26	36	46
Mismatch **σ** [fs]	37	12	18	31

Theoretically, the proposed ring TDC's detectable range is only limited by the size of the output counter. However, the actual detectable range is limited by the mismatch between the transition times of the rising and the falling edges. In addition, unlike a delay based ring oscillator, there is no feedback to compensate the mismatch over time in a ring TDC. As a result, the duty cycle of a pulse propagating in a delay ring will either gradually increase or decrease, which eventually causes the pulse vanishing after passing a certain numbers of delay cells, limiting the achievable detectable range of the ring TDC. As illustrated in Fig. 3 (a), the unmatched rising time τ_r and falling time τ_f lead to a progressively increased pulse width, which eventually overlaps with the feedback pulse.

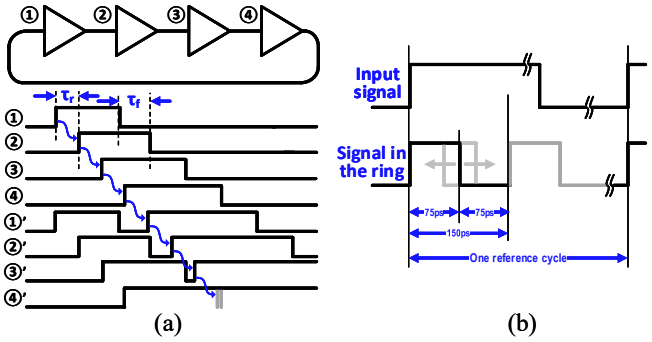

Fig. 3. (1) Signal propagating issue in a delay ring when rising delay is not equal to falling delay. (b) Pulse generation timing diagram.

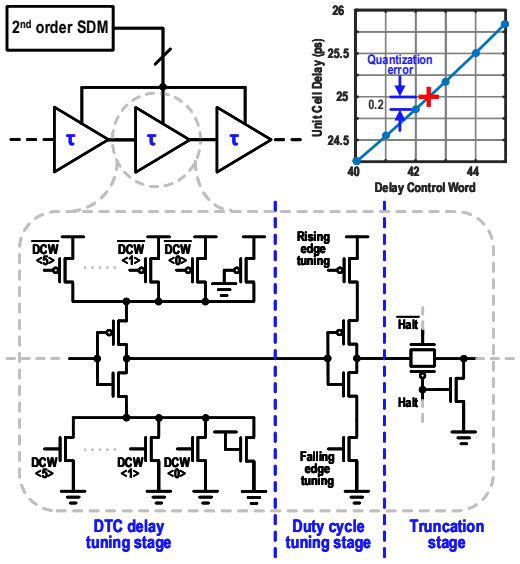

Fig. 4. Unit delay cell circuit diagram.

In this design, the rising and falling delays can be adjusted in the duty cycle tuning stage of the unit delay cell, shown in Fig. 4, in order to achieve the targeted large delectable range of

14 bits. Unit delay cells in both slow and fast delay chain comprise of three parts: delay tuning stage, duty cycle correction stage and signal truncation stage. The rising and falling edges are adjustable to regulate the pulse duty cycle and to compensate process, voltage, and temperature (PVT) variations. The truncation transmission gate switch stops the signal propagation to save power consumption once TDC conversion is completed. Its delay is digitally controlled by 6 tuning bits, capable to tune from 20ps to 42ps. Hence, each delay cell is a 6-bit digital-to-time convertor (DTC) with quantization errors. For instance, to get a 25ps delay, the closet reachable delay in the DTC is 24.8ps. The 0.2ps temporal error will be accumulated during the signal propagating in the delay ring and result in a poor INL of more than 5 least significant bits (LSBs). We therefore propose to interpolate the precise delay amount by toggling among a few adjacent delay control words following a sequence generated by a 2nd order SDM. The time averaged value among those discrete delay steps gives the correct desired delay value and the quantization errors generated in the process are noise-shaped to high frequency band by the SDM. As shown in Fig. 5, the measured INL has been suppressed from over 5 LSB to less than 2 LSB with the 2nd order SDM running at 8 times over-sample ratio.

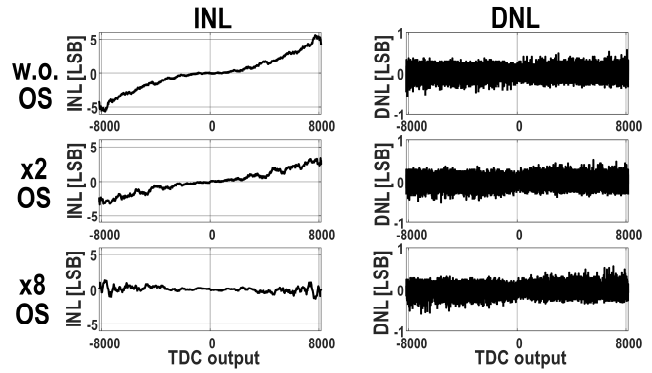

Fig. 5. Measured (a) INLs/ (b) DNLs under different delay over-sample ratio.

The prior-art 2D arbiter array suffers periodic nonlinearity associated with the transitions between arbiter lines (folding points) of the 2D structure. To further reduce the nonlinearity, we used a unique spiral 2D arbiter array, which reduces 2D Vernier TDC's INL, while doubles its detectable range. We also adopted the SDM folding location randomization technique to minimize the errors associated with the arbiter line's folding points [2]. Figure 5 illustrated the proposed arbiter spiral array and its linearization method. Instead of following a saw-tooth comparison path used in prior-art 2D TDC designs [5], the proposed spiral arbiter configures the comparison path in spiral format, which minimizes the errors due to mismatch. Arbiter folding locations in prior-art 2D structure are fixed in hardware once the delay chains and arbiters are chosen. If there are multiple sets of arbiter folding locations that can satisfy the condition given in (1), we can alter the folding locations in each comparison cycle, leading to a reconfigurable arbiter array that randomizes the folding point errors. As illustrated in Fig. 6, configuration "CFG 1" is the nominal arrangement with the delays τ_f=25τ and τ_s=26τ. The enlarged square labeled with "64, 65" indicates one of the folding locations in CFG 1, where a periodic error occurs. For "CFG 2, 3, and 4" with different delay settings, the folding points are shifted to "67, 69 and 72", which lead to different TDC transfer curves. These arbiter configurations are controlled by the output sequence of a 2nd order SDM. Figure 7 shows the improvement when applying the 1st order SDM and the 2nd order SDM and comparing to the case without SDM linearization. It is clear that the measured INL has been suppressed to 0.79LSB with the 2nd order SDM from an INL level of 1.8 LSB when no SDM is applied.

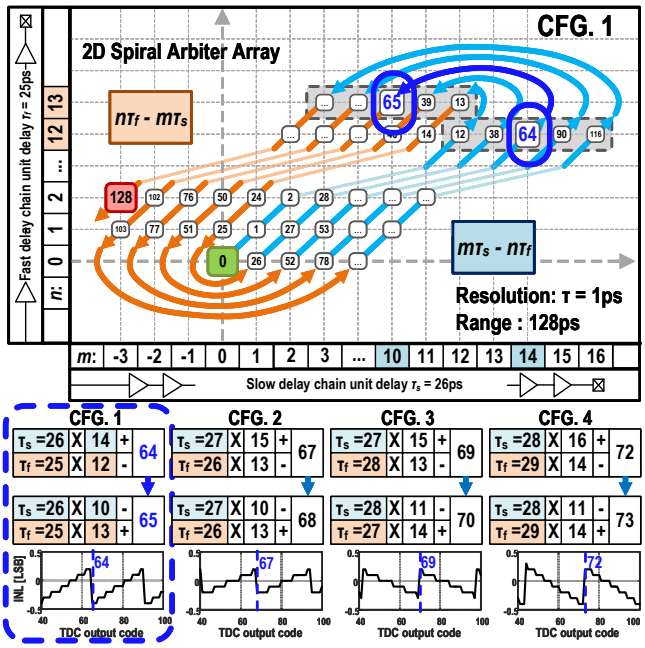

Fig. 6. Reconfigurable arbiter array and their corresponding INLs, showing periodic errors associated with their folding locations.

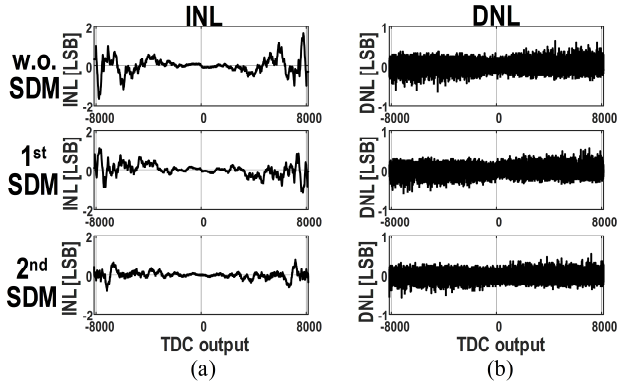

Fig. 7. Measured (a) INLs/ (b) DNLs with different SDM settings.

III. Measurement Resultsw

The proposed TDC was fabricated in a 130nm CMOS technology. As shown in the die photo of Fig. 8, the TDC core occupied an area of 0.06 mm^2 and other auxiliary parts (I/O buffers and digital unit) occupied another 0.06 mm^2 area. The TDC covers a conversion range over 1.6 ns with a 1 ps resolution. The measured full-range transfer curve and its corresponding INL are given in Fig. 9. The TDC consumes

2.4mW under a conversion rate of 10MS/s and 1.2-volt power supply. With a 2nd order delay SDM running at 80MHz for delay interpolation and a 2nd order linearization SDM running at 10MHz folding error linearization, our proposed architecture achieved a very competitive linearity performance with DNL/INL of 0.41/0.79 ps when compared with state-of-the-art TDC designs. Fig. 10 is a comparison considering both data converter FoM and TDC effective resolution. Table II summarized our TDC key performance and compared with newly reported TDC designs.

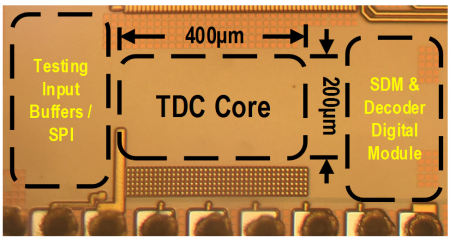

Fig. 8. Die photograph of the TDC prototype chip.

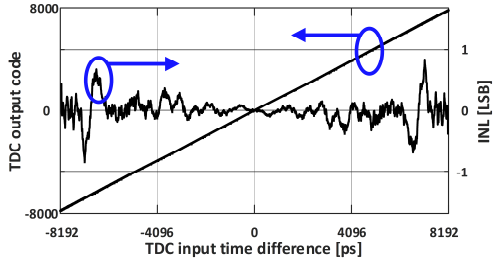

Fig. 9. Measured TDC full-range transfer curves and INL.

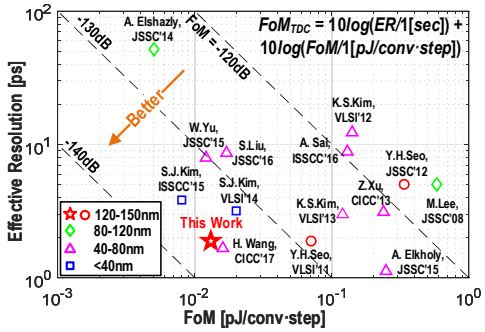

Fig. 10. Performance comparison.

IV. Conclusions

We presented a combined ring and 2D Vernier TDC with 14-bit (1.6ns) detectable range and 1-ps resolution. The delay ring TDC is equipped with a 2nd order SDM with 8 times oversampling ratio to interpolate the precise delays need for a taped measurement for calibrating the rising and falling delays in order to achieve the large detectable range and suppress INL accumulation in the ring. The 2D Vernier TDC consists 2nd order SDMs for both delay interpolation and folding error linearization. With 1ps resolution, the TDC still achieved state-of-the-art measured linearity performance with DNL/INL of 0.41ps/0.79ps, demonstrating a very competitive TDC design using a large feature size technology of 0.13um CMOS.

References

[1] C. W. Yao, W. F. Loke, et. al., "A 14nm Fractional-N Digital PLL with 0.14ps$_{rms}$ Jitter and -78dBc Fractional Spur for Cellular RFICs," *ISSCC*, pp. 421-422, Feb. 2017.

[2] H. Wang, F. Dai, H. Wang, "A 330μW 1.25ps 400fs-INL Vernier Time-to-Digital Converter with 2D Reconfigurable Spiral Arbiter Array and 2nd-Order ΔΣ Linearization," *CICC*, Apr. 2017.

[3] G. Marzin, S. Levantino, et. al., "A 20Mb/s phase modulator based on a 3.6GHz digital PLL with -36dB EVM at 5mW power," *ISSCC*, Feb. 2012.

[4] V. K. Chillara, Y. H. Liu, et. al., "An 860μW 2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (bluetooth smart and Zigbee) applications," *ISSCC*, Feb. 2014.

[5] L. Vercesi, A. Liscidini, et. al., "Two-dimensions Vernier time-to-digital converter," *IEEE J Solid-state Circuits*, vol. 45, pp. 1504-1512, Aug. 2010.

[6] J. Yu, F. Dai, et. al., "A 12-bit vernier ring time-to-digital converter in 0.13 μm CMOS technology," *IEEE J. Solid-State Circuits*, pp. 830-842, Apr. 2010.

[7] S. J. Kim, T. Kim, et. al., "A 0.63ps, 12b, synchronous cyclic TDC using a time adder for on-chip jitter measurement of a SoC in 28nm CMOS technology," *VLSI*, pp. 1-2, Jun. 2014.

[8] S. J. Kim, W. Kim, et. al., "A 0.6V 1.17ps PVT-tolerant and synthesizable time-to-digital converter using stochastic phase interpolation with 16× spatial redundancy in 14nm FinFET technology," *ISSCC*, Feb. 2015.

[9] A. Sai, S. Kondo, et. al., "A 65nm CMOS ADPLL with 360μW 1.6ps-INL SS-ADC-Based Period-Detection-Free TDC," *ISSCC*, pp. 336-337, Feb. 2016.

TABLE I. TDCs Performance Comparison

	VLSI 14 [7]	ISSCC 15 [8]	ISSCC 16 [9]	CICC 17 [2]	ISSCC 17 [1]	**This work**
Topology	Cyclic	Stochastic	SS-ADC	2D Vernier	SAR-ADC	**Ring+2D Vernier**
Process	28nm	14nm	65nm	45nm	14nm	**130nm**
NoB	12	10	6.1	8	7	**14**
ENoB (1)	9.74	8.28	5.76	7.58	3.68	**13.2**
Resolution	0.63ps	1.17ps	6ps	1.25ps	0.2ps	**1.0ps**
ER (2)	3.15ps	3.85ps	7.60ps	1.67ps	2ps (4)	**1.74ps**
Speed [MHz]	10	100	40	80	26	**10**
DNL [LSB]/[ps]	0.5/0.32	0.8/0.94	---/---	0.25/0.31	---/---	**0.41/0.41**
INL [LSB]/[ps]	3.8/2.39	2.3/2.7	0.27/1.6	0.34/0.4	9/1.8	**0.79/0.79**
Power [mW]	0.82	0.78	0.36	0.33	---	**2.4**
FoM (3)	0.02	0.01	0.13	0.02	---	**0.02**

1. ENoB = NoB – $\log_2$(INL+1).
2. Effective Resolution (ER) = Resolution × $2^{(NOB-ENOB)}$.
3. FoM = Power / (2^{NOB} × F_S) [pJ / conv-step].
4. calculated based on in-band phase noise. PN = $10\log(N^2(2\pi f_r)^2 t_{res}^2/12/f_r)$.