A 330µW 1.25ps 400fs-INL Vernier Time-to-Digital Converter with 2D Reconfigurable Spiral Arbiter Array and 2nd-Order ΔΣ Linearization

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Abstract **—This work presents an 8-bit 1.25ps resolution Vernier TDC with 2D reconfigurable spiral arbiter array and ΔΣ linearization for ADPLL. The 2D spiral arbiter array improves both linearity and detection range. The quantization errors introduced by delay cells and 2D arbiter array folding points are minimized using a reconfigurable arbiter array with 2nd order ΔΣ modulators. The prototype in a 45nm CMOS technology consumes 0.3mW power under a 1V power supply with 80MHz conversion rate. The measured maximum DNL/INL are 0.31/0.4 ps with ΔΣ linearization and 1.35/1.03 ps without ΔΣ linearization, respectively.**

Index Terms **— ADPLL, auto-calibration, DNL, linearization, INL, time-to-digital converter (TDC), Vernier TDC, ΔΣ modulation (SDM).**

I. Introduction

Time-to-digital converter (TDC) is a key building block in all digital PLL (ADPLL) applications. In order to improve ADPLL's performance and lower its in-band phase noise, the TDC resolution has been pushed to around 1-ps level according to the recently reported data. However, improving TDC's linearity performance faces increasing challenges when its resolution shrinks. The non-linearity will not only jeopardize ADPLL's in-band phase noise but also lead to a higher fractional spur level.

Vernier TDC formed by two delay chains with slightly different delays achieves improved resolution and linearity since the 1st order mismatches are automatically cancelled. However, its conversion range is greatly limited due to the reduced conversion step size. Consequently, a large number of delay stages are needed to cover the detection range, resulting in high power consumption. ADC based TDCs and other ΔΣ TDCs struggle with low conversion rate while performing with good linearity and resolution [1], [2]. Gated Ring Oscillator (GRO) based TDC achieves fine resolution with large range while suffering nonlinearity due to leakage problems [3].

Vernier TDCs with a 2-dimensional (2D) arbiter array, as illustrated in Fig. 1 (a), are widely used to achieve improved detection range with fine resolution [4]. The linearity of a 2D Vernier TDC is more sensitive to delay variations compared to normal Vernier TDC. A linear conversion using 2D topology requires that $n\ (\tau_s - \tau_f) = \tau_s$, where τ_s and τ_f denote the delays of a single cell in slow chain and fast chain, respectively, and n is the number of delay cells in fast chain. This condition demands precisely matched delays in both delay chains. A small delay deviation can lead to large periodic nonlinearity. Mismatches lead to slope error and gap or overlap between each of the two arbiter lines, producing errors with periodicity in both differential nonlinearity (DNL) and integral nonlinearity (INL). Indeed, the periodic errors in the TDC transfer curve can be related to the folding points of the 2D arbiter array. To illustrate the problem, a 4% delay mismatch is assumed and simulated. Fig. 1 (b) and (c) present TDC's transfer curve, DNL and INL. These plots illustrate that a small delay mismatch could lead to a large non-linearity. In addition, the number of periodic cycles in the non-linearity plots correspond to the number of arbiter lines with the peaks located at the folding points between each of the two arbiter lines.

This work presents an 8-bit 1.25ps resolution Vernier TDC with a novel 2D spiral arbiter array and 2nd order ΔΣ modulations to randomize two types of errors associated with (1) delay quantization of the digital-to-time convertors (DTC) based delay cells and (2) folding points when an arbiter line transits from one to another. Fabricated in a 45nm CMOS technology, the prototype TDC consumes 0.33mW under 1 V power supply with 80MHz conversion rate and achieves 0.4ps maximum INL.

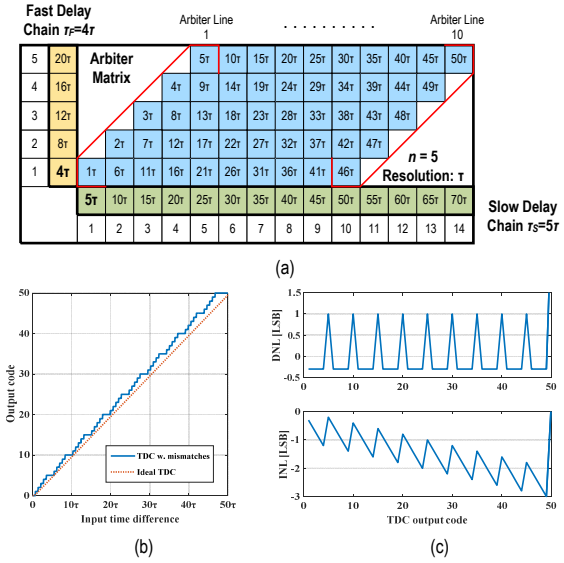

Fig. 1. Illustration of a conventional 2D Vernier TDC. (a) Vernier delay lines and the 2D arbiter array, (b) simulated TDC transfer curve, and (c) non-linearity with 4% delay mismatch.

II. Proposed Architecture and Circuit Implementation

In order to overcome the nonlinearity problem associated with the conventional 2D Vernier TDC, we propose to construct the arbiter array in a 2D spiral form, as shown in Fig. 2. Instead of folding the arbiter line in a saw-tooth form in one direction, we propose to arrange the arbiter path in a spiral shape such that the maximum mismatches along the comparison path can be reduced at least by half. Furthermore, the 2D spiral arbiter array is able to double the detection range with only 5 additional delay cells in the slow chain in this design.

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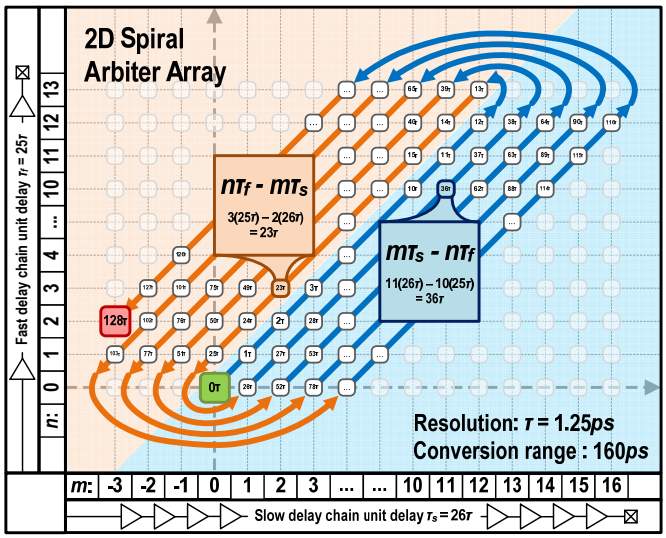

Figure 2: Proposed Vernier TDC with 2D spiral arbiter array.

Figure 3 shows a comparison between the proposed spiral arbiter array and conventional arbiter array to show the spiral architecture alone provides improved linearity. Scheme '1' shows a spiral 2D arbiter placement, while schemes '2' and '3'provide the same conversion range of 64τ by using conventional 2D Vernier TDC schemes. Scheme '2' extends the number of the delay cells while keeping identical temporal delay, while scheme '3' reduces the temporal delay by half to keep the same amount of arbiter line in the array. Among these 3 options, the spiral 2D scheme has the least number of delay cells which indicates less power consumption and delay mismatch as well as the best linearity with the same delay error as shown in the TDC transfer curve.

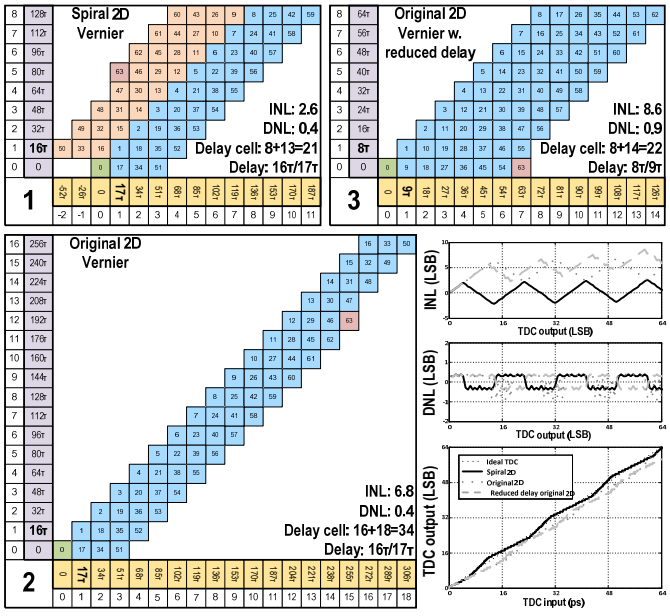

Fig. 3. A comparison among spiral 2D arbiter array (scheme 1) and conventional 2D arbiter formations (scheme 2 and 3), indicating a better linearity with spiral 2D formation.

The unit delay cell in the delay chain comprises a pair of cascaded inverters as shown in Fig. 4. To reduce mismatch, both fast and slow delay chains use identical unit delay cells. The unit delay is tunable from 19ps to 43ps with 7 digital control bits in order to meet tuning requirements against PVT variations. Hence, each delay cell is a 7-bit digital-to-time convertor (DTC) with quantization errors due to its digitized tuning. For instance, to achieve a 31.25ps time delay, the closet reachable delay in DTC is 31.15ps shown in Fig. 4. This 0.1ps time difference introduces a 0.3% delay error that leads to an INL of more than 2 least significant bits (LSBs). We therefore propose to interpolate the precise delay amount by toggling among a few adjacent delay control words (DCW) following a sequence generated by a 2nd order ΔΣ modulator.

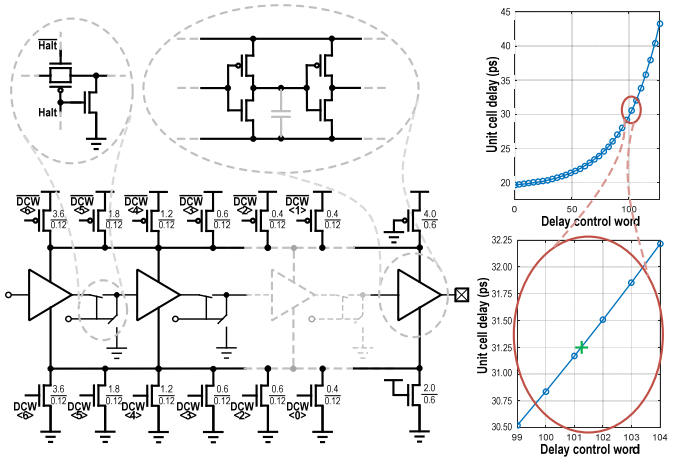

Figure 4: 7-bit digitally controlled tunable unit delay cell with 2nd order ΔΣ modulation to minimize delay quantization error.

Delay chain contributes more than 80% of the total power in a Vernier TDC. The unit delay cells use only parasitic capacitance to generate the delay and are optimized for noise, mismatch and power consumption. Moreover, transmission gates are used to switch off the signal propagation through the remaining delay stages once the comparison process is completed. This switching scheme can dramatically cut down the TDC power consumption by 50% in a fractional-N DPLL and by as much as 90% in an integer-N DPLL.

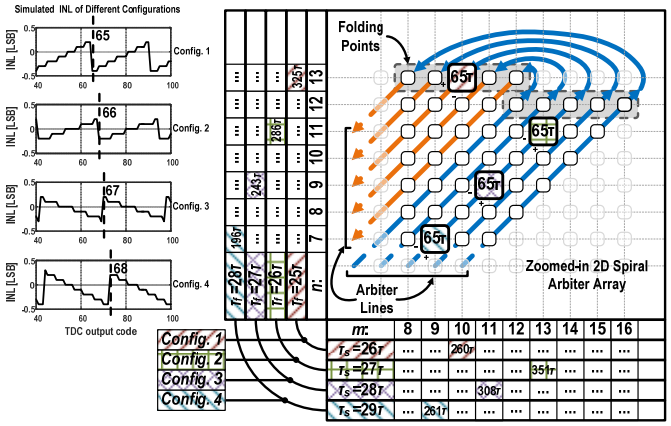

Figure 5: 2D arbiter array with reconfigurable folding configurations used to randomize TDC output periodic errors.

2D Vernier TDC suffers periodic nonlinearity from the transition (folding points) between different arbiter lines in a 2D array. Arbiter folding locations are fixed in hardware once the delay chains and arbiter parameters are chosen. To reduce the nonlinearity, we propose to randomize the folding locations. If there are multiple sets of arbiter folding locations that can satisfy the condition $n\ (\tau_s - \tau_f) = \tau_s$, we choose different folding points in each comparison cycle, leading to a reconfigurable arbiter array structure that randomizes the mismatch errors. Figure 5 illustrates four valid configurations of a spiral 2D arbiter array, in which

"Config. 1" is the nominal arrangement with delay τ_f=25τ, τ_s=26τ. The enlarged square labeled with "65τ" indicates one of arbiter line folding locations in Config. 1, where the maximum periodic error occurs. In "Config. 2, 3, and 4" with different delay settings, the "65τ" nodes are moved to different locations and the corresponding folding points in the simulated INL curves are shifted to TDC output code 66, 67, and 68. These four arbiter configurations are controlled by the output sequence of a 2nd order ΔΣ modulator, leading to dramatically improved DNL and INL.

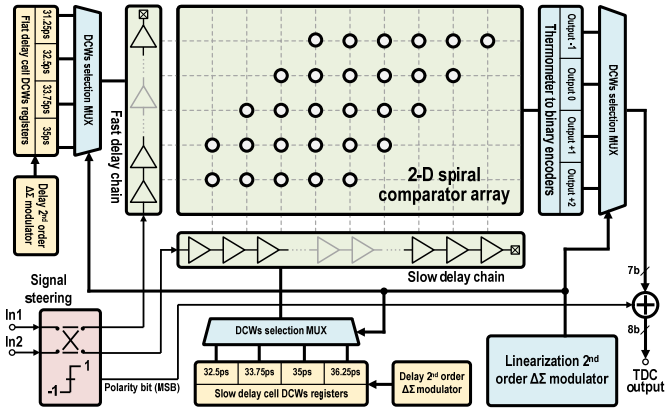

Figure 6: Block diagram of the proposed reconfigurable 2D spiral Vernier TDC with 2nd order ΔΣ linearization.

Figure 6 shows the entire block diagram of the proposed TDC. The 2D spiral Vernier TDC provides 7 output bits and a steering module that detects lead or lag information as the polarity bit (the 8th bit). The reconfigurable structure comprises only one 2D spiral arbiter array in hardware, with one of the four valid configurations selected based on the output sequence of a ΔΣ modulator at the beginning of each reference cycle. Arbiter array outputs are processed by thermometer to binary encoders for final TDC output.

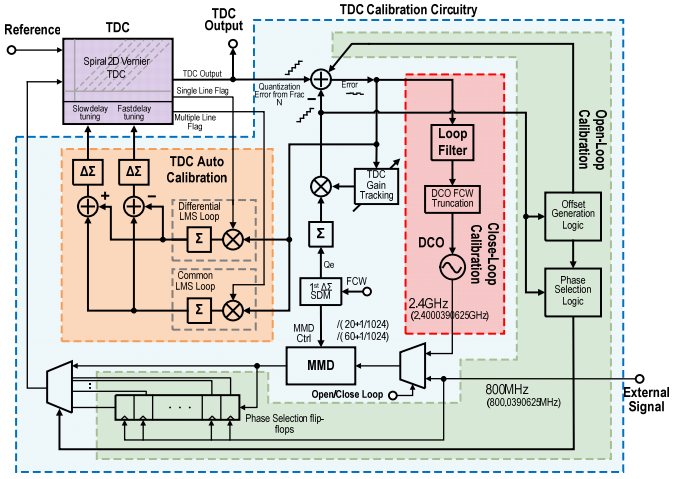

Fig. 7. Automatic 2D Vernier TDC close-loop and open-loop delay calibration.

The proposed 2nd order ΔΣ linearization technique needs precise delay calibration. This work leverages the least mean squares (LMS) algorithm with the digi-phase technique and is capable of both open-loop and closed-loop calibrations [5]. The block diagram of the TDC calibration circuit is shown in Fig. 7. The calibration is accomplished with a 40 MHz reference clock to insure enough time for digital calculation. The loop's output frequency is set to a certain number with a small fractional part such as 60+1/1024, shown in the figure. With the small fractional number, the quantization error generated by the factional-N accumulator generates a staircase ramp waveform with fine step size that can be used to sweep the TDC input over one DCO cycle. The corresponding TDC output is further subtracted from an ideal ramp signal, creating an error signal that is used to automatically adjust the TDC delays. Two LMS loops are designed to collect the differential and common error signals used for fast and slow delay calibrations. Similarly, the open-loop calibration uses an external signal to mimic the loop's behavior. However, although the frequency is pulled close to the desired value, the phase can still be unknown without a loop. A large phase error could saturate the TDC's output and the calibration algorithm would fail. Thus, proper logic circuits are needed to shift the correct phase error back to the TDC detection range.

III. Measurement Results

This TDC design was fabricated in a 45nm CMOS technology. As shown in the die photo of Fig. 8, the 2D Vernier TDC core occupies an area of 0.03 mm^2. Other auxiliary circuits occupy 0.03 mm^2 space. The measured full-range TDC transfer curves of the TDC with and without the 2nd order ΔΣ modulator, are presented in Fig. 9. The TDC covers a conversion range from -160 ps to 160 ps, namely 8 bits output with a 1.25 ps resolution.

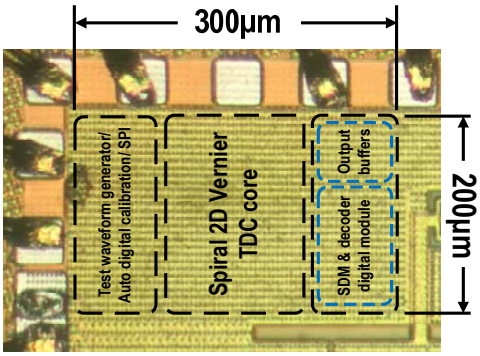

Figure 8: Die photograph of the TDC prototype chip.

For comparison, linearity performances are measured with 2nd order, 1st order (averaging) and no ΔΣ modulations, as shown in Fig. 10. Periodic errors as large as 1.27LSB were observed in the measured INL without ΔΣ modulation, showing dominant nonlinearity associated with the folding points of 2D arbiter array. With 2nd order ΔΣ randomization, the measured INL and DNL have much lower errors of 0.34LSB and 0.25LSB, respectively. To illustrate the robustness of the linearity, the INL is measured over a temperature range from 25°C to 125°C and a voltage range from 0.8V to 1.2V, shown in the corner of Fig. 9. This TDC was designed to cover 8 bits with 1.25 ps resolution. Taking non-linearity into consideration, the effective number of bits (ENOB) is 7.58 bits with 1.67 ps effective resolution.

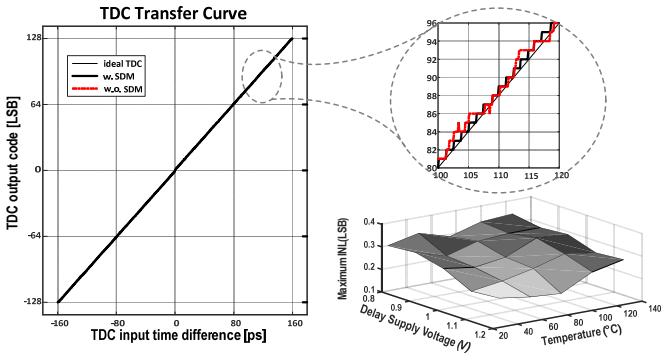

Figure 9: Measured TDC full-range transfer curves with and without the 1st order ΔΣ modulation and maximum INL under voltage/temperature variations.

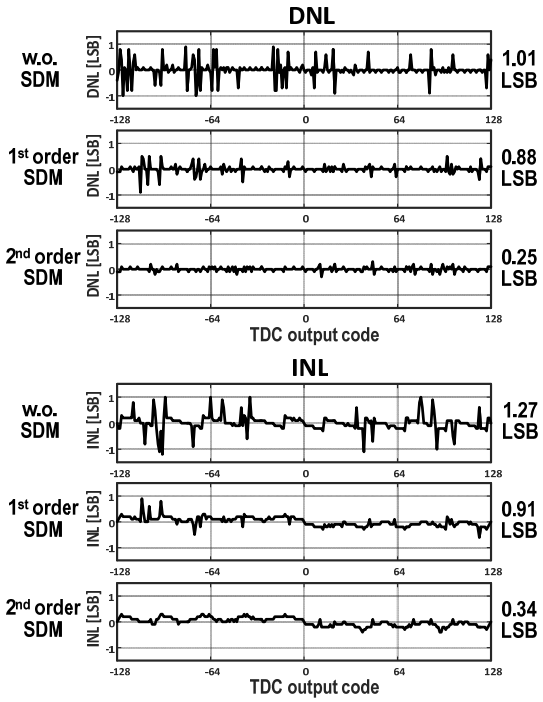

Figure 10: Measured DNL and INL of the proposed TDC without ΔΣ modulation, with 1st order ΔΣ modulation and with 2nd order ΔΣ modulation.

In the measurement, the TDC consumes 0.3mW under a conversion rate of 80MS/s and a 1.0 V power supply when the TDC input is swept with a staircase ramp signal similar to a fractional-N mode operation in ADPLL. It consumes 0.7mW if every cycle of the input phase difference exceeds the TDC's full range. It consumes less than 0.1mW when dealing with small time interval input, for instance, in an integer-N mode operation in ADPLL.

Performance summary and comparison with prior-art TDC designs are listed in Table I. FoM_E is a well-accepted figure of merit among ADC designs, which takes the converter's linearity performance into consideration. For TDC designs, effective resolution is an important factor that directly impacts ADPLL's performance. Comparing with both effective resolution and FoM_E, we summarized the performance of recently reported state-of-the-art TDCs and present the comparison in Fig. 11; demonstrating a competitive TDC design, among the state-of-the-art, with excellent linearity.

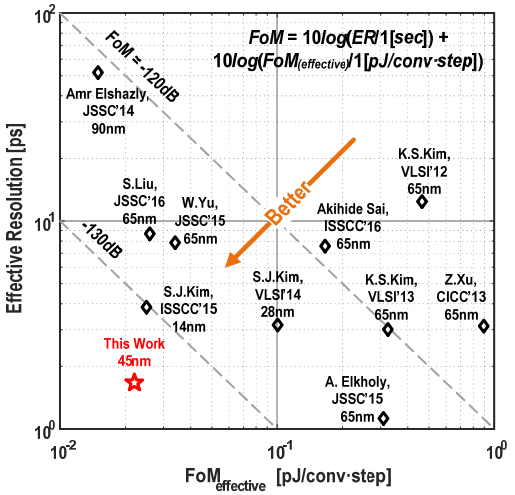

Figure 11: Performance summary and comparison with prior art TDC designs.

TABLE I. PERFORMANCE COMPARISON WITH RECENTLY REPORTED TDCS

	JSSC 10 [4]	ISSCC 15 [6]	ISSCC 16 [7]	This work
Topology	2D Vernier	Stochastic	SS-ADC	Spiral 2D Vernier
Process	65nm	14nm	65nm	45nm
NOB	7	10	6.1	8
ENOB*	4.90	8.28	5.76	7.58
Resolution	4.8	1.17ps	6ps	1.25ps
ER**	20.58	3.85ps	7.60ps	**1.67ps**
Speed [MHz]	50	100	40	80
DNL [LSB] /[ps]	0.9 /4.32	0.8 /0.94	---	**0.25** **/0.31**
INL [LSB] /[ps]	3.3 /15.8	2.3 /2.7	0.27 /1.6	0.34 **/0.4**
Power [mW]	1.7	0.78	0.36	**0.33**
Area [mm^2]	0.02	0.036	0.022	0.04
FoM_E***	1.14	0.025	0.166	**0.022**

* ENOB = NOB – $\log_2$ (INL+1).
** Effective Resolution (ER) = Resolution × $2^{(NOB - ENOB)}$.
*** FoM_E = Power / ($2^{ENOB} \times F_S$) [pJ / conv-step].

IV. CONCLUSIONS

In this paper, we presented an 8-bit 2D spiral Vernier TDC with 1.25ps temporal resolution. A novel spiral formation arbiter array is developed to enlarge the TDC detection range and to reduce the nonlinearity. The 2nd order ΔΣ modulatiors are adopted to lower the quantization error of the DTC based delay cells and the intrinsic periodic errors due to the folding of the 2D arbiter array. The measured maximum DNL and INL of the proposed TDC are 0.25 LSB and 0.34 LSB, respectively. With the transmission gate switches added in the delay cell, power consumption of the TDC is greatly reduced. Fabricated in 45nm CMOS technology, the TDC prototype consumes 0.33mW under a 1 V power supply with a conversion rate of 80MHz. It achieves 1.67 ps effective resolution and a FoM_E of 0.022.

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