A 0.8~1.3 GHz Multi-phase Injection-locked PLL Using Capacitive Coupled Multi-ring Oscillator with Reference Spur Suppression

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Abstract — **This paper presents an inductor-less injection-locked PLL (IL-PLL) using capacitive coupled multi-ring oscillator (MRO) implemented in a 0.13 um CMOS technology. The multi-ring coupled oscillator with capacitive coupling achieves improved phase noise by minimizing noise injection from tail current sources and adjacent rings. The 1.1 GHz triple-ring coupled ring oscillator (TRO) achieved measured phase noise of -110.4 dBc/Hz @ 1 MHz offset, showing 7 dB phase noise reduction comparing to its single-ring oscillator (SRO) counterpart. When a reference signal is injected into the main ring, the output signals in auxiliary rings maintain the same low phase noise, yet achieve 12 dB lower reference spur. With a 50MHz reference, the MRO based IL-PLL generates 24 multi-phase outputs covering 800 MHz to 1.3 GHz with reference spur reaching -63 dBc. The proposed IL-PLL achieves an in-band phase noise of -121 dBc/Hz @ 1MHz offset and 513fs jitter at 1.1 GHz output frequency with 13.5 mW power.**

Keywords — Ring oscillator, inject-locking, IL-PLL; capacitive coupling, spur suppression; digital calibration.

I. INTRODUCTION

Analog components such as inductors present a challenge for technology scaling of analog circuits. In addition, area efficient circuits are now highly desirable for low cost applications such as Internet-of-Things (IoT). Emerging technologies such as phase array, beam forming, passive mixing, N-path filtering and interleaved data converters require multi-phase clocks. Multi-phase signal can be generated by ring oscillators with either resistive load or LC based delay cells. Conventional LC oscillators cannot achieve area efficiency and technology scalability. However, ring oscillators without LC tanks normally end up with unacceptable phase noise. Recent techniques such as sub-sampling PLL (SSPLL) and injection-locked PLL (IL-PLL) can achieve excellent in-band phase noise performance. With the greatly reduced in-band noise, the loop bandwidth can be widened to help reducing the oscillator's phase noise, enabling inductorless low jitter frequency synthesis.

Recent work on ring oscillator designs showed improved phase noise using injection locking technique [2-5]. Injection-locked ring oscillator based PLL can greatly reduce the in-band phase noise by resetting the jitter accumulated over a reference cycle. However, high reference spurs, high reference frequency and injection related loop stability issues present challenges for this technique to be widely adopted in practical communication transceivers. Reference spurs in IL-PLL mainly comes from two sources: (i) timing mismatches between injection signal and the oscillation waveform and (ii) distortion in the output waveforms induced by injection pulses as illustrated in Fig. 1. Due to non-ideal injection, the output waveform will be distorted and the distortion repeats every reference cycle even if the injection occurs at the waveform's zero-crossing points. This periodic distortion causes reference spur in output spectrum. Pulse width T_D sets the lower bound of the reference spur level in conventional IL-PLLs. Moreover, in ring oscillator based IL-PLLs, the distorted waveform in one stage will propagate through other stages, leading to large reference spurs in every output phases. Timing mismatches can be calibrated by using conventional charge pump PLL, as shown in Fig. 2 (a), to track the reference clock as its *N*th sub-harmonic, where *N* is the loop division ratio. Recent IL-PLL designs [2-4] have suggested aligning injection pulses with the oscillator's zero-crossing points for suppressing the reference spurs. However, the reference spur level achieved in these designs are still relatively high compared to traditional PLLs. Ref. [5] uses a "soft-injection" scheme to reduce the reference spur, yet it comes with the penalty of degraded phase noise and increased reference frequency, since it requires more often injections to compensate the weakened injection signal.

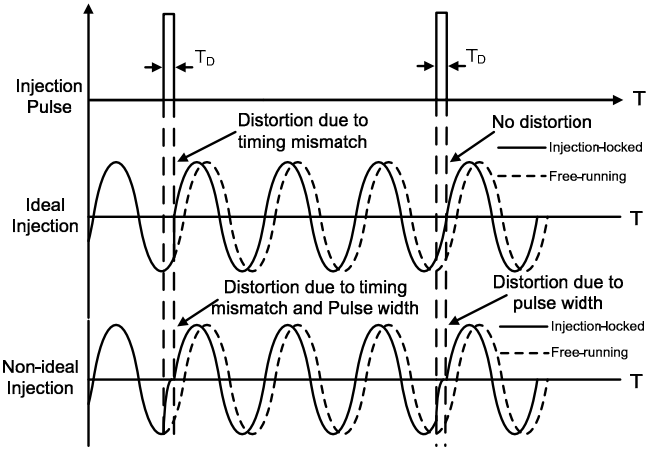


Fig. 1. Distortion of output waveform due to timing mismatch and non-ideal injection.

It is highly desirable to push the phase noise of ring oscillators close to what LC-based oscillators can reach. In this paper, we propose a multi-ring based ring oscillator (MRO) that couples multiple rings with proper phase shift to achieve

978-1-5090-5191-5/17/$31.00@2017 IEEE

improved phase noise and Figure of Merit (FoM) comparing to its single ring (SRO) counterpart. Common source coupling benefits from reduction of current tail noise [1] and introducing phase delays in coupling paths further minimizes noise coupled from the adjacent rings [6]. The resultant triple ring coupled ring oscillator (TRO) demonstrates phase noise improvement of 7 dB compared to its SRO counterpart. In this paper, we further demonstrate the capability of the proposed MRO for reference spur reduction when used in an IL-PLL. The combination of the proposed phase noise and spur reduction techniques solve the dilemma between the injection effectiveness and its resultant reference spurs, providing an area efficient multi-phase signal generation with low phase noise, low reference spur without using high reference frequency.

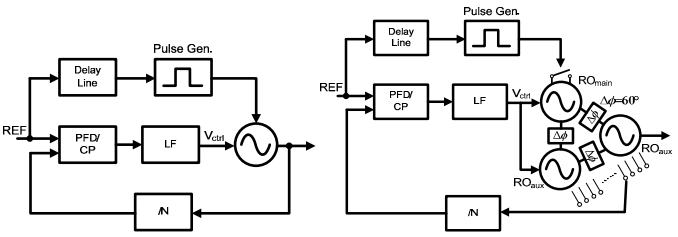


Fig. 2. (a) IL-PLL with frequency tracking loop, and (b) conceptual diagram of a multi-ring coupled ring oscillator (MRO) based IL-PLL.

II. Phase Noise and Reference Spur Reduction in MRO

As shown, the injection timing is critical for achieving low reference spurs. The proposed TRO triples the number of output phases that can be used as a coarse phase tuning to calibrate the injection point for reference spur reduction. In addition, a tunable reference delay cell can provide fine calibration that further aligns the injection point to zero-crossing of the output waveform. Increased number of output phases available in an MRO can be used to relax the tuning range of the reference delay stages in timing calibration. Moreover, we propose to inject the reference signal only in one ring, called "*main ring*", in an MRO structure. We demonstrate that the outputs from other rings, called "*auxiliary rings*", can maintain the same phase noise, yet with much lower reference spur level. The proposed TRO based IL-PLL, shown in Fig. 2 (b), employs three identical rings coupled at the virtual grounds of the differential pairs. The reference pulses are injected into the main ring (RO_{main}), which causes reference spurs as shown in the conventional IL-PLLs. However, the reference spur level in RO_{aux} is found to be at least 12dB lower than that in the RO_{main} since there is no injection pulse that periodically resets the oscillation waveform. In other words, the waveform existing in the auxiliary rings are much smoother and its phase noise is as good as the main ring waveform due to common source coupling as explained below.

To analyze the phase noise of RO_{main} and RO_{aux}, let's begin with an analysis of phase noise in RO_{main} without coupling with any auxiliary rings. Due to injection-locking, RO_{main}'s phase noise follows the reference's phase noise as $PN_{ref}+20\log_{10}(N)$ [2], where PN_{ref} is the phase noise of reference signal. Intuitively, injection-locked RO_{main} can be regarded as the signal source with phase noise of $PN_{ref}+20\log_{10}(N)$. Through common source coupling, the signals at common source nodes in the RO_{main} are injected into the RO_{aux} with division ratio of 1, which indicates that the phase noise in RO_{aux} should be the same as that of the RO_{main}.

The concept of reference spur suppression in MRO is illustrated in Fig. 3. Let's use a double-ring coupled ring oscillator (DRO) as an example, where the output phase relationship between RO_{main} and RO_{aux} is $\pi/2$ in stable state, while the waveforms at their common mode nodes have phase difference of π. The reference injection pulses T_D resets the signal in RO_{main} and causes the distortion of its output waveform, resulting in a phase shift of $\Delta\varphi$ compared to the waveform without injection. This abrupt phase/amplitude jump causes reference spurs in the main ring. However, when it's coupled into the auxiliary ring, the differential output waveform is not sensitive to AM since the perturbation is injected at the common-mode nodes of the auxiliary ring. The only observable effect is the variation of its bias current that leads to slight frequency shift without abrupt phase jump. This subtle FM is the key for auxiliary waveform to track the phase of the main waveform without noticeable waveform distortion that was the source of the reference spurs. The amount of frequent shift in the auxiliary ring is dependent upon the coupling strength, which dictates the amount of current coupled between the rings. After phase accumulation, the waveforms in auxiliary ring will eventually be phase-locked to that of the main ring, resulting in the same amount of phase correction ($\Delta\varphi/2$) to retain their stable state governed by their property of symmetry. Thus, the auxiliary ring outputs benefit from injection for phase noise reduction, yet without abrupt waveform distortion, which leads to greatly reduced reference spurs. It should be pointed out that coupling at the signal output nodes still introduces spurs from RO_{main} to RO_{aux} as the case using a phase interpolator in [5].

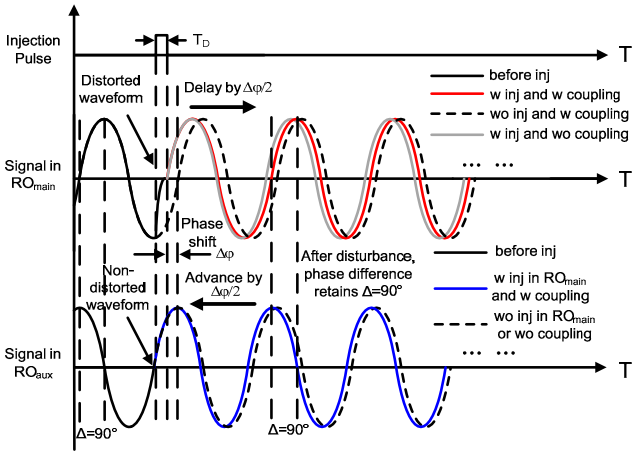


Fig. 3. Simulated transient diagram of output waveforms in main and auxiliary rings in the proposed IL-PLL using DRO.

III. Proposed MRO based IL-PLL

A. Proposed IL-PLL Architecture

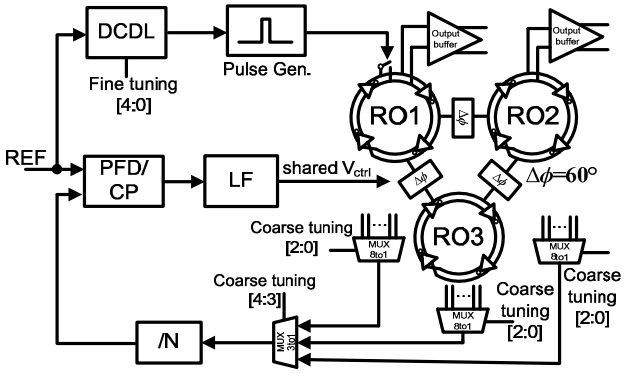
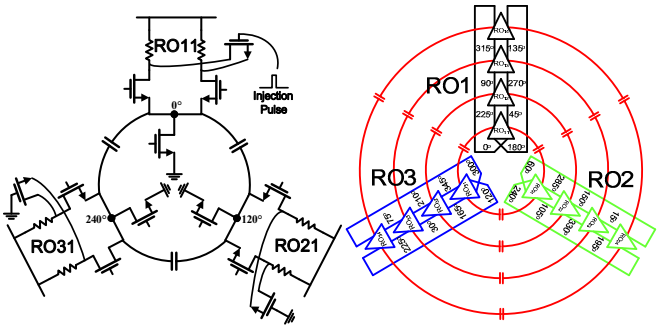


Fig. 4. Circuit implementation of proposed IL-PLL with TRO.

The proposed MRO based IL-PLL achieves improved phase noise and reference spur by coupling multiple rings through capacitive common source coupling. The available multi-phase outputs can also be utilized for injection timing calibration in conjunction with a tunable reference delay stage. The proposed IL-PLL architecture is composed of a TRO, frequency divider, phase/frequency detector (PFD), charge pump, reference pulse generator, and calibration unit with phase selector for coarse tuning and digitally controlled delay line (DCDL) for fine tune, as shown in Fig. 4. The reference injection signal from pulse generator is injected at the first stage of the main ring oscillator RO1 in the TRO. The outputs in auxiliary oscillators RO2 and RO3 as well as RO1 are buffered for outputs. One of the 24 output phases, whose zero-crossing is closest to the reference edge, is fed back to the frequency lock loop (FLL) that locks the ring oscillator output frequency to the *N*th harmonic of the reference signal.

B. Injection-Locked TRO



(a) (b)

Fig. 5. Circuit implementations of (a) the first stages in a TRO; (b) capasitive coupled TRO.

Circuit implementation of the proposed injection-locked triple ring coupled ring oscillator (IL-TRO) is shown in Fig. 5. The TRO is formed by connecting three identical ring oscillators with 4 delay cells per ring through capacitive coupling paths with 60º phase shift. Differential pair with resistive load is employed as unit delay cells. The first stage, RO11, of the main ring in the TRO contains an injection switch for reference signal injection as illustrated in Fig. 5 (a). Dummy switches are also added in the first stages of the auxiliary rings to keep the structure symmetry with balanced output load. Signals at the virtual ground nodes are forced to be 0º, 120º, 240º due to second harmonic coupling. The first ring's phases cover 0º, 45º, 90º and 135º as well as their anti-phases 180º, 225º, 270º and 315º. The second and third rings start with 60º and 120º phase offsets, respectively, and cover the remaining 16 phases. The implemented TRO generates total 24 uniformly spaced output phases. Common source coupling reduces noise from current tail sources and its associated phase delays minimizes noise coupled from the adjacent cores by avoiding injection at the sensitive zero-crossing points [6].

C. Phase Calibration in IL-PLL

The 24 output phases from the TRO can be utilized for injection timing calibration. Phase selection was done by monitoring the reference spurs. The lowest reference spur corresponds to an injection point that is closest to the zero-crossing of the output waveform. After the coarse phase selection, a DCDL is use to fine tune the injection point to further minimize the reference spur. To balance the loading and delay mismatch, a two-stage multiplexer is employed for phase selection. Multi-phase outputs in TRO reduces the required tuning range in the DCDL, leading to less in-band phase noise degradation due to reference delay cells. As the fine tune for the timing calibration, a 5-bit DCDL is formed using inverters with tunable capacitor arrays, which has a tuning range of 40 ps. The combination of 5-bit fine tuning and 5-bit coarse tuning covers the PVT variations and phase mismatches for frequency range from 800 MHz to 1.3 GHz in simulation.

IV. Measurement Results

The prototype of the 800MHz-1.3GHz IL-PLL was fabricated using a 130 nm CMOS technology as shown in the die photo of Fig. 6. Three rings with their coupling capacitors are placed symmetrically in the layout with a core area of 350×350 μm^2. The measured phase noise of the free running ring oscillators operating at 1.1 GHz output is given in Fig. 7, where TRO with phase noise of -110.38 dBc/Hz achieves 4 and 7 dB noise improvement compared with its DRO and SRO counterparts, respectively. After injection-locking, the phase noise in RO_{aux} reaches -120.97 dBc/Hz @1MHz offset, while the phase noise in RO_{main} is measured as 120.52 dBc/Hz, demonstrating almost identical phase noise performance in both main and auxiliary rings (Fig. 8).

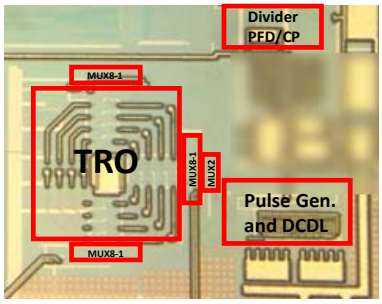


Fig. 6. Die photo of the proposed MRO based IL-PLL chip.

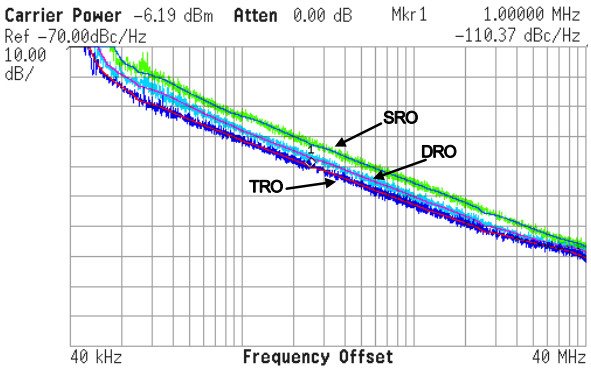


Fig. 7. Measured phase noise in free-running auxilairy rings @1 MHz offset at 1.1 GHz for SRO, DRO and TRO.

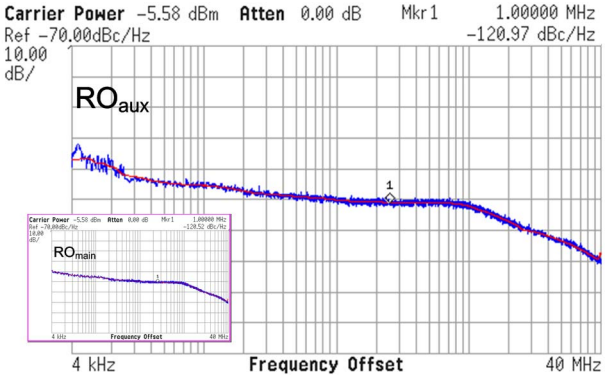


Fig. 8. Measured IL-PLL phase noise at auxilairy ring RO_{aux} output @1 MHz offset at 1.1 GHz.

Without coarse phase calibration, the reference spur level could be as high as -30 dBc and -38 dBc in main and auxiliary rings, respectively. The measured output spectra of RO_{aux} and RO_{main} with only coarse phase calibration are shown in Fig. 9 (a). By selecting the proper output phase for feedback in coarse calibration, their reference spur levels reduce to -52 dBc and -43 dBc, respectively. When both coarse and fine phase calibrations are turned on, the measured reference spur levels drop to -62.5 dBc for RO_{aux} and -50.3 dBc for RO_{main}, respectively. Fig. 9 (b) demonstrates about 10 dB spur rejection by fine phase calibration and about 20 dB spur suppression comparing to non-calibrated IL-PLL case. For the entire tuning range from 800 MHz to 1.3 GHz, the reference spur is measured from -48 ~ -52 dBc in RO_{main} and -60 ~ -62.5 dBc in RO_{aux}, respectively, demonstrating an average of 12 dB reference spur suppression comparing to the main ring outputs, as shown in Fig. 10 (a). The measured phase noise @ 1MHz offset, Fig. 10 (b), ranges from -119.5 dBc/Hz to -123dBc/Hz over the entire IL-PLL tuning range, showing similar phase noise performances for both main and auxiliary rings.

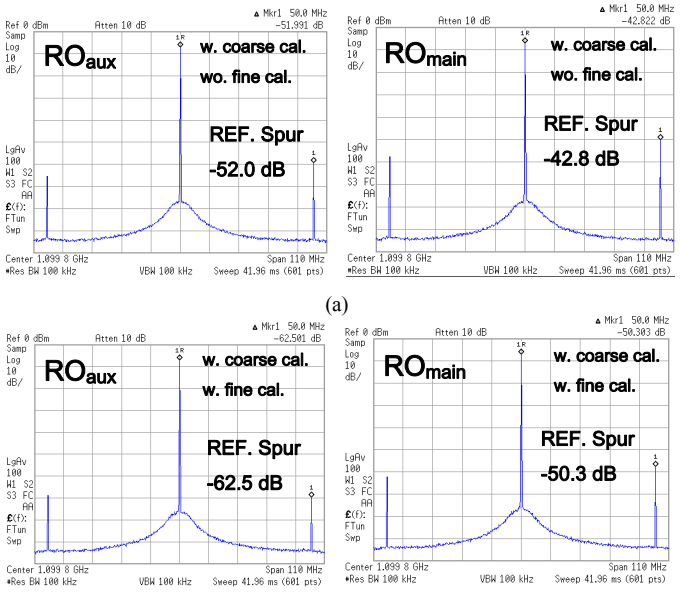
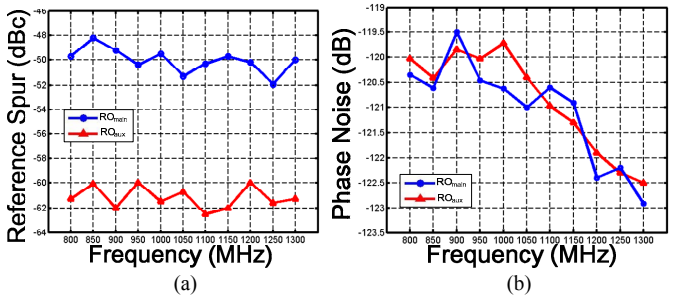


Fig. 9. Measured output spectra of auxilairy ring RO_{aux} and main ring RO_{main}, (a) with coarse calibration only and (b) with both fine and coarse calibration.



(a) (b)

Fig. 10. Measured reference spur levels (a) and phase noise @ 1MHz offset (b) in RO_{aux} and RO_{main} from 800 MHz to 1.3 GHz for the IL-PLL.

At output frequency of 1.1 GHz, the jitter in RO_{aux} integrated from 10 kHz to 40 MHz is measured as 513 fs with 13.5 mW power consumption under a 1.2 V power supply. Figure of merit of the proposed IL-PLL is thus -234.5 dB. Performance summary and comparison table is given in Table I. Compared to state-of-art ring oscillator based IL-PLL designs, this design demonstrated an effective reference spur and phase noise reduction technique with a low reference frequency of 50MHz.

V. Conclusions

We proposed an inductor-less multi-ring oscillator topology for use in IL-PLLs with 24 multi-phase outputs. The proposed common source capacitive coupling introduces proper phase delay that minimizes the noise injection from adjacent rings and the noise up-conversion from tail current sources, leading to greatly improved FoM per output phase. The TRO prototype achieved measured phase noise reduction of 7 dB compared to its SRO counterpart. It is also demonstrated that the common source coupling technique suppresses the reference spurs in auxiliary rings, while maintaining phase locking with its main ring where the reference pulses are injected. As a result, auxiliary ring outputs demonstrated 12 dB lower reference level comparing to the main ring outputs, while maintaining about the same phase noise. Furthermore, the available multiphase outputs in conjunction with a tunable reference delay cell with reduced tuning range are used to calibrate the injection timing, leading to greatly reduced reference spurs at -63dBc with a 50 MHz reference. Therefore, the proposed inductor-less MRO provides an area efficient technique for multi-phase clock generations with superior phase noise and spurious performances.

TABLE I. Performance Summary and Comparison with Other Ring VCO based IL-PLL Designs

	This work	[3] CICC15	[4] ISSCC16	[5] ISSCC15
Process(nm)	130	65	65	65
Reference (MHz)	50	125	120	380
Freq. (GHz)	0.8~1.3	2	0.96 ~1.44	0.8-1.7
Division Ratio	22	16	10	4
PN (dBc/Hz) @1MHz	-121 @1.1	-113 @2	-134.4 @1.2	-116 @1.522
Reference Spur(dBc)	-60 ~ -63	-48	-47 ~ -53	-63
Jitter σ_t (fs)*	513	971	185	3600
Power (mW)	13.5	9.5	3.74	3
Area (mm^2)	0.18	0.1	0.06	0.1
No. of Phases	24	8	10	28
FoM**	-234.5	-234.5	-244.9	-224.5
FoM$_P$ ***	-248.3	-243.5	-254.9	-239.0

* Integrated jitter σ_t for this work and [4] from 10K-40MHz, others from 1K -40M;

** $\text{FoM} = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1\,\text{mW}}{P}\right] - L(\Delta f)$;

*** FoM per phase: $\text{FoM}_P = \text{FoM} + 10\log(\text{No. of Phases})$.

Acknowledgment

We would like to acknowledge Dongyi Liao for help with PLL design and MOSIS for support of the chip fabrication under the MOSIS MEP program.

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