# Multi-Phase Sub-Sampling Fractional-N PLL with Soft Loop Switching for Fast Robust Locking

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***Abstract*— This paper presents a low phase noise sub-sampling PLL (SSPLL) with multi-phase outputs. Automatic soft switching between the sub-sampling phase loop and frequency loop is proposed to improve robustness against perturbations and interferences that may cause a traditional SSPLL to lose lock. A quadrature LC oscillator with capacitive phase interpolation network is employed to generate multi-phase outputs, which are further utilized to achieve fractional-N frequency synthesis. Implemented in a 130nm CMOS technology, the SSPLL chip is able to achieve a measured in-band phase noise of -120 dBc/Hz and a measured integrated jitter of 209 fs at 2.4 GHz, while consuming 27.2 mW with 16 output phases. The measured reference spur and fractional spur level is -72 dBc and -49 dBc, respectively.**

***Index Terms* — phase locked loop, subsampling, fractional-N, stability, multi-phase VCO, phase detector, jitter.**

## I. Introduction

Phase-locked loops (PLL) play a crucial role in wireless communication systems. The phase noise/jitter and spurious level of a PLL are the critical performance metrics that directly affect key performance metrics like error vector magnitude (EVM) and bit error rate (BER). Emerging wireless technologies like phased arrays with beamforming, high linearity passive mixing, N-path filtering, and interleaving data-converter all require multi-phase clock generation. Multi-phase clocks can be generated using poly-phase filters, which are narrow-band, or dividing a frequency that is N-times higher than the needed frequency. Neither technique provides multi-phase signals with low power and accurate phase across a wide bandwidth.

Recently, subsampling technique has been proposed as an alternative approach to the conventional tri-state phase-frequency detector (PFD) to achieve greatly improved in-band phase noise [1]. The SSPLL in [2] uses a tri-state PFD with large dead-zone to switch between the regular frequency/phase loop (FPL) and the subsampling loop (SSL). Due to the narrow capture range of the SSL, the SSPLL may lose lock in the presence of large perturbations. Moreover, potentially a long relocking time is required as phase errors may need to accumulate for quite some time before the dead-zone is passed and the FLL is switched on. This was solved in [3] by keeping both the FPL and SSL always on. In this paper, an automatic soft switching scheme is proposed to ensure agile and robust locking for improved SSPLL stability. When the phase error is approaching zero, the proposed scheme gradually increases the SSL gain and decreases the FPL gain, while maintaining a constant total loop gain. As a result, the loop dynamics such as gain and phase margins will not vary throughout the switching process. At lock, the gain of FPL is turned off while the SSL is turned on, resulting in improved in-band noise performance.

Furthermore, to achieve fractional frequency synthesis in subsampling mode, conventional methods involving toggling of frequency dividers and its associated sigma-delta noise shaping cannot be used directly, as VCO zero-crossing sampling by the SSL is wanted [1]. To resolve this problem, prior art has proposed to use digital-to-time converter (DTC) on the reference clock to offset this mismatch such that the reference edge remains aligned with the VCO zero-crossing even in fractional-N mode [4]. However, the DTC needs to cover one VCO cycle with high resolution to avoid phase noise degradation. In [5] a divider followed by phase interpolation has been proposed to greatly reduce the dynamic range of DTC, achieving very low in-band phase noise even in fractional mode. In this design, a Quadrature Voltage Controlled Oscillator (QVCO) is extended with a capacitive phase interpolation network to realize a 16-phase output. This enables fractional-N operation by selecting the closest desired phase in every reference cycle.

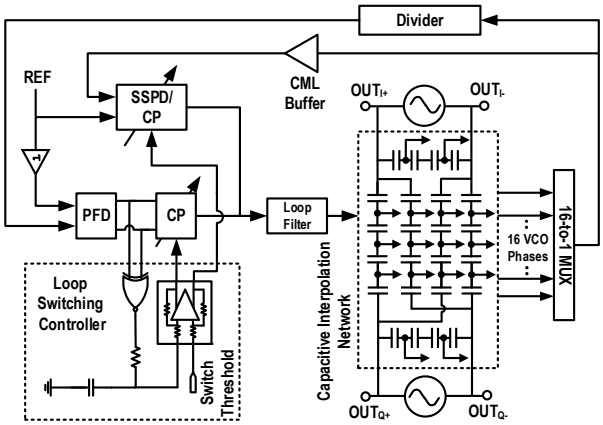


Fig. 1. Block diagram of the proposed fractional-N SSPLL architecture.

## II. Proposed Fractional-N SSPLL Architecture

As illustrated in Fig. 1, the proposed SSPLL includes two feedback loops: a FPL employing a conventional PFD for frequency acquisition with large frequency and phase errors and a SSL using a subsampling phase detector (SSPD) for

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close-in phase lock to achieve low in-band phase noise. A loop switching controller with variable switching threshold and bandwidth is implemented to achieve soft switching between the two loops. During the initial locking process, only the FPL with PFD is turned on. As the PLL approaches locking, the gain of the FPL will be gradually reduced while the gain of SSL will be gradually increased. The total loop gain is maintained almost constant throughout the switching process to ensure constant loop dynamics, thus improving loop stability. In order to compensate for the feedback delay difference between SSL and FPL, a tunable delay cell is inserted on the reference path before the PFD in the FPL. The optimal value of this delay can be programmed to be the propagation time through the dividers in the FPL. In other words, this delay is adjusted such that the VCO output is locked to the same edge of the reference in both FPL and SSL modes. This added delay avoids the sudden phase jump when switching from FPL to SSL.

### *A. A Robust Soft Loop Switching Scheme*

Even though a SSPLL can achieve superior phase noise compared with a conventional PLL, potential stability problems remain a concern for its practical applications. Due to the periodic nature of sinusoidal waveform, the detection range of a SSPD spans only one VCO period. If the instantaneous phase error exceeds one VCO period, e.g. due to interference, the SSL will not be able to track the phase error and the PLL will lose lock. To resolve this problem, an auxiliary frequency loop is employed for robust frequency locking. However, coordination between two loops remains a design challenge.

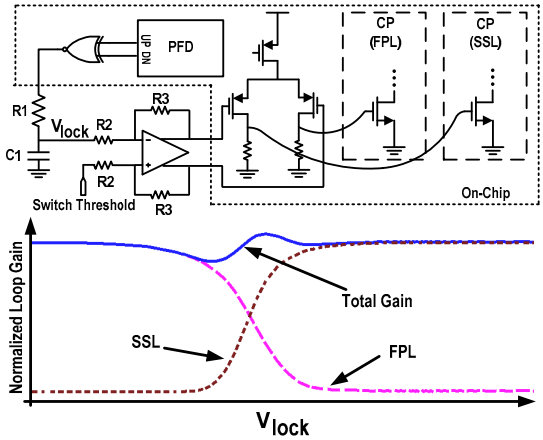


Fig. 2. (a) Diagram of the proposed loop switching controller. (b) Simulated gains of FPL and SSL as well as total loop gain during loop switching.

In our design, we propose a novel switching scheme in which the PLL instantly turns on FPL once the phase error exceeds the detection range of SSPD. As shown in Fig. 2, an XNOR gate with an RC filter constitutes the phase error measurement. Its output voltage $V_{lock}$ is inversely related to the average phase error. As the PLL drives toward phase lock, $V_{lock}$ will approach the supply voltage. On the other hand, $V_{lock}$ will be close to zero when the loop is completely out of lock. By adjusting parameters of the filter, different switching control bandwidth (switching speed) can be achieved. Next, an operational amplifier compares $V_{lock}$ with a switching threshold which can be programmed off-chip. Once $V_{lock}$ exceeds the threshold, a soft switching process kicks in where the FPL is gradually turned off while the SSL is gradually turned on. An integrated differential pair further scales the switching control signal to a proper voltage range that can be used to ensure a relatively constant total loop gain during transition region. The resulting control signal is applied as gate bias of the current source in the charge pumps (CP) to tune the gains from the two loops. Maintaining a relatively constant loop gain during switching ensures loop stability with sufficient phase and magnitude margin. Moreover, even though the FPL still needs to be running after lock in order to detect instantaneous phase error, the charge pump for FPL is turned off to avoid degrading in-band phase noise. The power consumption of the FPL is not a big contributor for the loop power budget.

### *B. Multi-Phase Clock Generation with Capacitive Interpolation Network*

Using four phases provided by a quadrature VCO (QVCO), additional phases can be generated through an interpolation network. As shown in Fig. 3 in a 16-phase generator, two pairs of $C_1$ and $C_2$ are connected in series between two quadrature phases which are 90° apart. These four capacitors interpolate three sub-phases that are each 22.5° apart, for an appropriate choice of the capacitance ratio between $C_1$ and $C_2$. Assuming $C_2/C_1 = \alpha$, it can be proved that $\tan\theta = \frac{\alpha}{\alpha+2}$, where $\theta$ represents the angle of the first sub-phase. By setting $\theta = 22.5°$, $\alpha$ can be calculated as $\sqrt{2}$ which is approximated as 1.414 in the actual implementation. The magnitudes of the four original quadrature phases from the VCO are slightly suppressed by $C_3$ and $C_4$ in order to generate the same magnitude as for the interpolated phases. This requires $C_4/C_3 = 1/\sqrt{2}$. The absolute values for these capacitors depend on two factors: (i) they should be as small as possible to avoid extra capacitive loading on the VCO, which could decrease its oscillation frequency, tuning range and Q-factor; (ii) they should be much larger than the load capacitance attached to each phase output, otherwise the interpolated phases will deviate from the desired value. Furthermore, an on-chip fractional accumulator controls a multiplexer implemented with current-mode-logic (CML) to select the closest VCO phase for fractional-N operation. The multiplexer is designed to minimize its loading effect to the capacitive network and VCO.

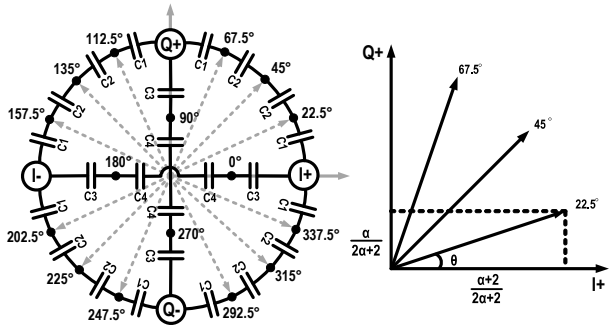


Fig. 3. (a) Capacitive phase interpolation network. (b) Interpolating arbitrary phases from a pair of quadrature signals with capacitance ratio $\alpha = C_2/C_1$.

## III. Circuit Implementation

### A. Subsampling Phase Detector & Charge Pump

As shown in Fig. 1, the multiplexer after VCO is connected to SSPD through a CML buffer. Similar to a sample and hold circuit, the SSPD consists of switches ($M_1$, $M_7$) and sampling capacitors ($C_s$ ~ 0.12pF) as shown below. Two shorted transistors $M_2$ and $M_8$ are connected to source and sink extra charges from the switching transistors. Their sizes are tuned to approximately half of $M_1$ and $M_7$. Similar to [2], two dummy paths consisting of $M_3$~$M_6$ with extra sampling capacitors are implemented to remain a constant loading on previous stages during sampling which helps reducing the reference spur. The gain of the SSL is controlled through tuning the gate bias of $M_{11}$ for loop switching. The charge pump is connected to the loop filter through a switch controlled by a tunable pulse signal PUL.

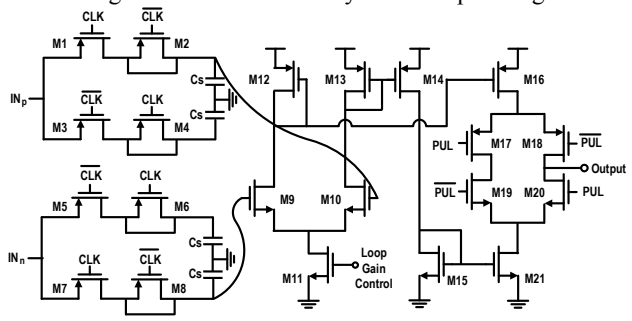


Fig. 4. Schematic diagram of the SSPD and CP.

### B. Quadrature VCO

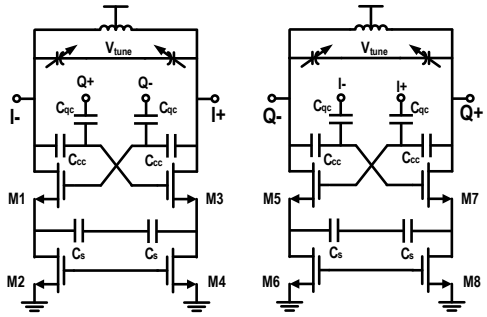


Fig. 5. Schematic diagram of quadrature capacitive coupled VCO.

The capacitive coupled QVCO is illustrated in Fig. 5, in which the oscillation signal of each oscillator core is coupled to the gates of the NMOS transistors in the next stage through the phase-coupling capacitor $C_{qc}$. The cross-coupling capacitor $C_{cc}$ path forms the $-g_m$ needed for oscillation. The combination of coupling factor, defined as $m = C_{qc}/C_{cc}$, source degeneration $C_S$ and $g_m$ can be used to tune the coupling path phase delay for minimum phase noise and phase error without multi-modal oscillation. We choose *m=0.6* and phase delay of 60° to achieve the optimized phase noise and phase error [6]. The I/Q outputs from the QVCO are connected to the interpolation network for multi-phase signal generation, as shown in Fig. 3.

## IV. Measurement Results

The proposed SSPLL is implemented in a 130 nm technology with the die photo shown in Fig. 6. The total active area is approximately 0.43 $mm^2$. The 16-phase multi-phase SSPLL consumes 27.2 mW with a supply voltage of 1.2 V. The VCO is able to tune from 2.33 GHz to 2.42 GHz.

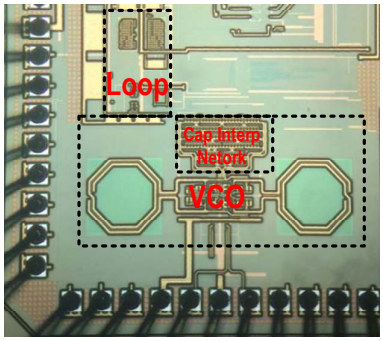


Fig. 6. Die Photo of the fractional-N SSPLL.

The reference clock was generated with a 50 MHz crystal oscillator. In integer mode, the measured phase noise at 2.4 GHz is shown in Fig. 7. With a loop bandwidth of 3 MHz, an integrated jitter of 209 fs was achieved with an in-band noise floor of -120 dBc/Hz owing to the low noise SSPD. With careful circuit and layout design, a very low reference spur of -72 dB was measured. In the fractional-N mode, the fractionality was set to 1/16 to synthesize a carrier frequency of 2.347 GHz. The measured phase noise is shown in Fig. 8, achieving an in-band phase noise of -118 dBc/Hz. The measured spectrum in fractional-N mode is shown in Fig. 9, showing a close-in fractional spur with power level of -49 dBc at 3.12 MHz.

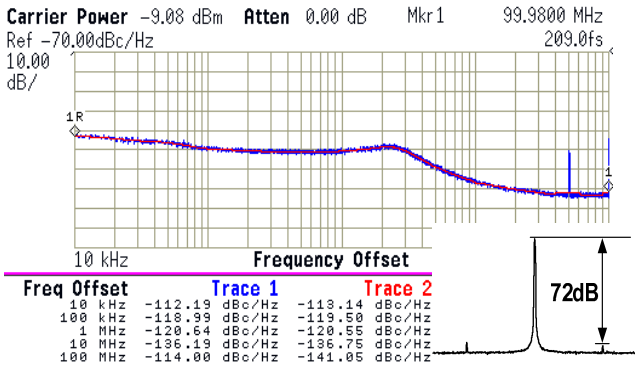


Fig. 7. Measured phase noise and reference spur at 2.4 GHz in integer mode.

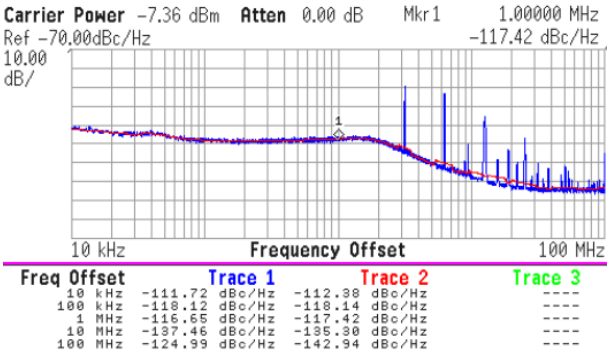


Fig. 8. Measured phase noise in fractional-N mode at 2.347 GHz.

To demonstrate the effectiveness of our proposed soft loop switching scheme, a perturbation on VCO's power supply is injected periodically in a way similar to [3]. Interestingly, our programmable loop controller is able to mimic the case of prior-art SSPLL using a large dead-zone of $T_{ref}/2$ in PFD as proposed in [2] by setting the switching threshold to $V_{CC}/2$. Equivalently the loop controller would switch from FPL to SSL if the phase error is less than $T_{ref}/2$.

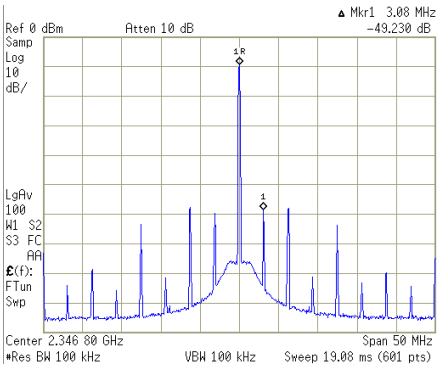


Fig. 9. Measured fractional spur at 2.347 GHz output.

As shown in Fig. 10 (a), a supply perturbation of approximately 150 mV causes the PLL to lose lock. The locking signal $V_{lock}$ instantly drops, indicating lock is lost. However, the FPL has not been enabled until the phase error becomes large enough to trigger the FPL. Note that soft switching is still applied in this case which is different from the hard switching case used in [2]. However, the issue of delayed relocking is clearly demonstrated.

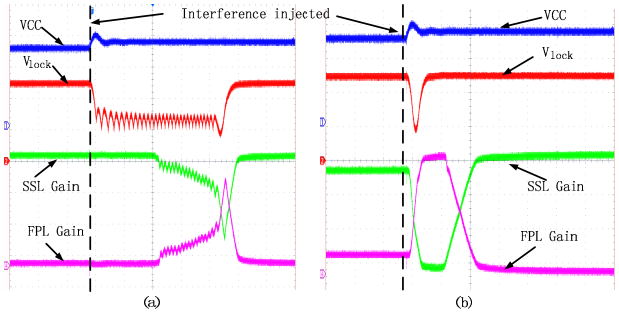


Fig. 10. Measured relocking transient behavior after a supply perturbation for (a) low switching threshold, similar to a SSPLL using FLL with large dead-zone; (b) high switching threshold, demonstrating fast relock for the proposed SSPLL.

In our proposed switching scheme, a high switching threshold close to $V_{CC}$ is applied (~1.15 V with a $V_{CC}$ of 1.2 V). This ensures that SSL is enabled only when the phase error is within its detection range. As shown in Fig. 10 (b), once the lock detection voltage drops below the switching threshold, the loop instantly switches to the FPL with PFD. The relocking process takes much shorter time than the prior-art result. After the loop is relocked, it is switched back to the SSL. Since FFL is completely disconnected from the loop filter after phase lock, the interference and noise from FFL can be minimized. A performance summary and comparison to other designs is given in Table I. Although the smallest fractionality (1/16) is limited by the number of available phases, finer fractional step size can be obtained by introducing tunable delays on the reference path. In this case, the interpolated VCO phases can be used as a coarse tuning, while the tunable reference delay cells can provide fine tuning with reduced tuning range.

TABLE.1 MEASURED SSPLL PERFORMANCES AND COMPARISONS.

| | Gao [2] JSSC-10 Integer-N | Hsu [3] TCAS-15 Integer-N | Narayanan [5] JSSC-16 Frac-N | This work Frac-N |
|---|---|---|---|---|
| Tech | 180nm | 65nm | 65nm | 130nm |
| Ref. (MHz) | 55.25 | 50 | 40 | 50 |
| Output Freq. (GHz) | 2.21 | 1.9-2.3 | 4.34-4.94 | 2.3-2.4 |
| In-band PN (dBc/Hz) | -121 | -122 | -120 | -120 |
| Int. RMS Jitter (fs) | 300 | 484 | 133 | 209 |
| Ref. Spur (dBc) | -80 | -41 | -70 | -72 |
| Frac. Spur (dBc) | - | - | -59 | -49 |
| Power (mW) | 3.8 | 8.8 | 6.2 | 27.2 |
| FoM (dB) | -244 | -236 | -249 | -239 |
| No.of Out. Phases | 2 | 2 | 4 | 16 |
| FoM per Phase ($FoM_p$) (dB) | -247 | -239 | -255 | -251 |

$FoM = 10log((\frac{\sigma_t}{1s})^2 \cdot \frac{Power}{1mW})$, $FoM_p = FoM - 10log(No.of\ Phases)$

## V. CONCLUSIONS

We presented a fractional-N subsampling PLL with fast robust locking using a soft switching between a frequency and sub-sampling phase control loop. The loop switching controller shows improved relocking capability without compromising in-band phase noise. The QVCO includes a capacitive phase interpolation network for multi-phase clock generation and fractional-N operation. This fractional-N SSPLL achieves a reference and fractional spurs of -72dBc and -49dBc, respectively. Measurement results showed an integrated jitter less than 209fs at 2.4GHz output.

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