A Low-Noise Inductor-less Fractional-N Sub-Sampling PLL with Multi-Ring Oscillator

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***Abstract* — In this paper, a compact inductor-less PLL using multiple coupled rings oscillator is presented. Sub-sampling technique with soft loop gain switching is applied to reduce the in-band phase noise. As a result, the loop bandwidth can be widened, which suppresses the phase noise from ring oscillator as well. Fractional-N mode is implemented by utilizing the multiple phase outputs inherently generated by the ring VCO. Using multiple rings instead of one allows generating more phases for finer frequency resolution without decreasing oscillation frequency. The coupled multi-ring oscillator with proper phase shift also achieves reduced phase noise comparing to their single-ring counterpart. The PLL was implemented in a 0.13um CMOS technology, consuming 19 mW from a 1.3 V power supply. The measured largest in-band fractional spur at 2.08 MHz is -42 dBc. The measured integrated jitters were 571 fs and 690 fs around 1.2GHz output in integer mode and fractional mode respectively, achieving a FoM of -230 dB.**

***Index Terms* — ring oscillator, coupled-rings, sub-sampling, fractional-N PLL, phase noise, jitter.**

I. Introduction

Phase-locked loop (PLL) with LC tank based voltage controlled oscillator (VCO) occupies large area due to the associated inductors in the tank. Using inductors increase the fabrication cost and presents challenges for technology scaling. To implement an inductor-less PLL, ring based VCO has been commonly adopted. However, due to the inferior phase noise of ring oscillators (RO), the achievable jitter performance is usually largely degraded compared with those using LC tank based VCOs. Recently, techniques including injection locking (IL) and sub-sampling phase detector (SSPD) has achieved impressive in-band noise floor with ring PLLs [1]. The penalty from inferior phase noise of ring-based VCOs can be largely eliminated given a wide PLL bandwidth, while maintaining its benefit of small form factor and scalability with technology.

The prior-art sub-sampling PLL (SSPLL) uses a tri-state PFD with large dead-zone to switch between the frequency/phase loop (FPL) and the sub-sampling loop (SSL) [2]. Due to the narrow capture range of the SSL, the SSPLL may lose lock with perturbations. Subsequently, a long relocking time is required as phase errors need to be accumulated for a while before the dead-zone is passed and the FLL is switched on. In this work, an automatic soft loop gain switching scheme is implemented to ensure agile and robust locking for improved loop stability.

To achieve fractional frequency synthesis with SSPLL, approaches based on fractional injection and phase interpolator (PI) has been proposed [5-7]. Generally, most of the approaches can be related to generating and switching between multiple VCO or reference phases. For ring-based VCO, multiple output phases are inherently generated within the ring, making it very convenient to implement fractional-N mode for SSPLLs. Furthermore, utilizing multiple coupled ring oscillator as proposed in [3], more output phases can be generated without decreasing oscillation frequency. Meanwhile, the coupled multi-ring oscillators with proper phase shift can achieve reduced phase noise comparing to single-ring counterpart.

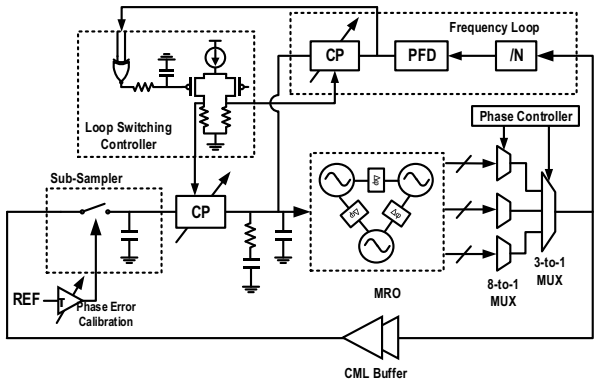


Fig.1. Proposed SSPLL architecture with coupled ring oscillators.

II. Proposed Architecture

Due to the narrow detectable range of SSPD, the sampling reference clock needs to be very close to the zero-crossing of VCO waveform. Maximum phase error must be within half of VCO cycle in order to avoid ambiguity due to the periodic locking nature of the SSPD [4]. One of the common solutions for fractional-N SSPLL is to introduce additional delay on the reference path forcing the reference edge to be aligned with the feedback waveform edge. Considering that the delay cells are on the reference path which involves an amplification of N^2 when the noise is transferred to PLL's output, the additional noise from reference delay cells has an enormous impact

on PLL's in-band phase noise performance. Thus the implemented design of fractional-N SSPLL with reference delays usually has a relatively higher in-band noise floor in fractional mode compared with their integer mode [7]. In our proposed design, the alignment of reference edge and feedback edge is achieved by selecting the closest phase from the RO without inserting large delays on the reference path as shown in Fig. 1. Instead, only a small delay cell for compensating the minor phase error between different VCO phases was employed. Thus the low in-band phase noise from SSPD can be maintained in both integer and fractional mode in our fractional-N SSPLL.

A. Multi-Ring Oscillator

In order to achieve finer frequency resolution, more VCO phases are needed. This requires more stages in ring oscillator which also leads to decreased oscillation frequency or higher power consumption in order to maintain the same oscillation frequency. However, using multiple coupled rings instead of one can break this trade-off. In our design, an MRO consisting of three coupled ring oscillator is adopted as shown in Fig. 2 (a), bringing in three times more VCO output phases with improved frequency resolution compared to single-ring architecture. The oscillation frequency of MRO is still determined by the total delay in a single ring while additional phases can be provided from other coupled rings. As another benefit of using multiple coupled rings, the phase noise can even be better than a single ring oscillator if proper phase delays are introduced on the coupling paths. Coupling with phase shifting avoids injecting noise from the adjacent rings at the most sensitive point of the oscillation waveform, i.e., its zero-crossing point. As a result, the overall phase noise will be improved by $10\log_{10} N$ theoretically, as the number of rings N increases. This indicates that the extra phases and improved phase noise can be achieved at the same time by using coupled rings. Due to PVT variations and non-ideal circuit behaviors, the multiphase outputs from an MRO are not perfectly spaced. By observing the phase error sampled by the SSPD, a fine delay inserted on the reference path can be tuned independently to compensate for each VCO output phase.

B. Multi-Modal Oscillation

In the implemented MRO, all the rings are designed to be identical in both schematic and layout in order to minimize the phase error between different phases. Thus multiple oscillation modes are possible, causing output phase ambiguity. Overall, the configuration could generate 8 possible oscillation modes with three rings, some of which are listed in Fig. 2. This creates problems for fractional-N mode since the relative phase needs to be predetermined for a particular fractional frequency. To cover different oscillation modes, programmable offsets are added to the multiplexer selection word in each ring such that the original phase order is always maintained.

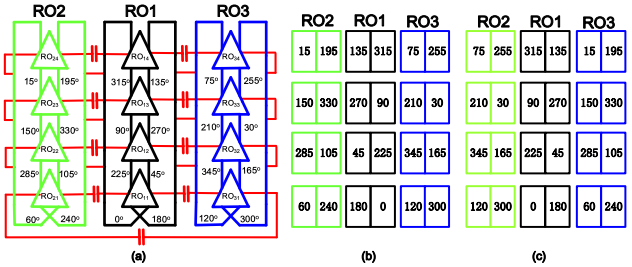


Fig. 2. (a) Block diagram of the implemented multi-ring oscillator; (b) and (c) other possible oscillation modes with phases in degree at different nodes in the MRO.

C. Soft Loop Gain Switching

In our proposed SSPLL, a SSL was adopted for low in-band phase noise; a FPL with a divider and a PFD is employed for initial frequency lock. A loop gain switching controller gradually switches the loop to the SSL after locking with the FPL. The gain switching is controlled by a lock detection signal which is generated using the outputs from PFD with an XNOR gate as shown in Fig. 1. Based on this lock signal, the current in the charge pumps (CP) of both loops is automatically tuned accordingly. The switching controller is implemented with a differential pair to ensure a constant total loop gain during switching. Compared with two prior art SSPLL designs where one uses PFD with a large dead-zone that disables FPL when phase error is smaller than the dead-zone [2], and another design that turns on both SSL and FPL all the time [4], our proposed soft gain switching scheme has much less gain variation across different phase errors as shown in Fig. 3(a). Consequently, our proposed SSPLL achieves much more stable phase margin during the loop switching, leading to greatly improved loop stability with robust relocking, as shown in Fig. 3(b).

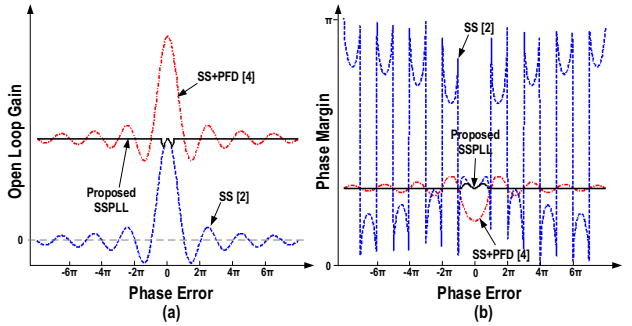
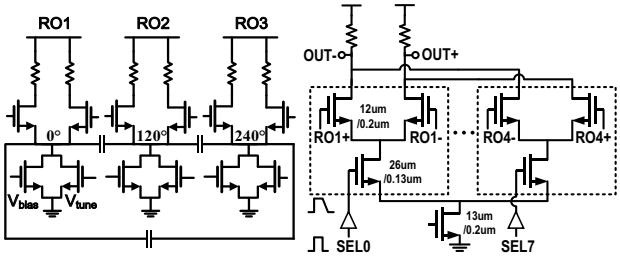


Fig. 3. Simulated loop gain and phase margin versus phase error with the proposed loop switching controller, SSL only [2] and SSL+PFD [4] schemes.

III. Circuit Implementation

A. Ring Oscillator



(a) (b)

Fig. 4. (a) Schematic diagram of the first stage in MRO; (b) Simplified schematic diagram of the first stage multiplexer.

As show in Fig. 4 (a), the MRO consists of 3 ROs where each ring has 4 stages of inverter. Each stage is implemented with a differential pair of resistive load to reduce the phase noise. Through a capacitive coupling at the common node in each stage, those three rings are constrained to oscillate with 0°, 120° and 240° at their common source nodes, respectively. Since common source nodes are the second harmonic of the oscillation frequency, the phase relations at the differential output nodes between ring oscillators are constrained to be 0°, 60° and 120°, respectively. It should be noted that the phase at the two output nodes of each differential pair may be reversible since only their common ground nodes are coupled together. The oscillation frequency is tunable using an extra current tail with V_{tune}. In the layout, the coupled ring oscillators are symmetrically placed as well as their coupling capacitors.

B. Multiplexer

In order to minimize the VCO load variation while switching to different phases, a two-stage CML based multiplexer is employed. Directly attached to the ring oscillator, the first stage multiplexer selects one phase from each ring as shown in Fig. 4 (b). Eight branches of differential pair sharing one pair of load resistors and a current source is connected to each ring, thus each output node in RO is only loaded by two parasitic gate capacitors. In fractional-N mode, the output phases are chosen rotatory in descending order to synthesize fractional frequencies. In addition, an asymmetric buffer is inserted on the selection words to sharpen its rising edge while flatten its falling edge before feeding into the multiplexer. This ensures a small amount of overlap between two adjacent selection bits to further reduce glitches at multiplexer output during switching which might disrupt divider in the frequency loop.

IV. Measurement Results

The SSPLL with MRO prototype was implemented in 0.13 um CMOS technology with the chip photo shown in Fig. 5. The core area occupies 0.21 mm^2. Smaller area can be achieved with a more compact layout in a finer technology. The reference clock was generated with a 50 MHz Crystek CVSS-945 crystal oscillator. The whole PLL consumes 19 mW from a 1.3 V power supply in which the phase loop and the MRO consumes 4 mW and 15 mW, respectively. The measured MRO oscillation frequency ranges from 0.8 GHz to 1.3 GHz.

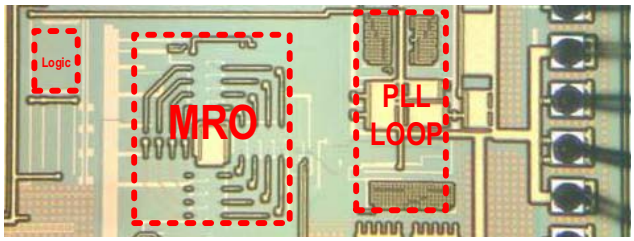
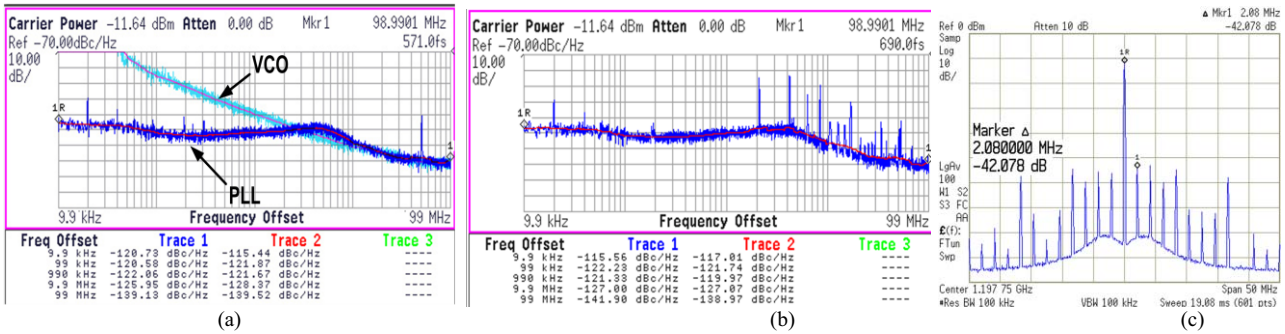


Fig. 5. Die photo of the proposed fractional-N SSPLL with MRO.

As shown in Fig. 6(a), the MRO has achieved a free-running phase noise of -110 dBc/Hz at 1 MHz offset frequency. An in-band noise floor of -122 dBc/Hz with an integrated jitter of 571 fs (from 10 kHz to 100 MHz) was achieved with the phase loop using SSPD. A wide loop bandwidth of 5MHz is assigned where the phase noise of MRO and in-band noise floor intersects. Thus the close-in



(a) (b) (c)

Fig. 6. (a) Measured phase noise in integer mode at 1.2GHz; (b) Measured phase noise in fractional-N mode at 1.198GHz; (c) Measured fractional spur at 1.198 GHz with worst spur at -42dBc level.

phase noise from MRO is largely suppressed by SSPD.

In fractional-N mode, the smallest fractional offset frequency achievable with this design is 2.08MHz where only one phase jump is experienced in each cycle. Using this setting, the loop locks to a center frequency around 1.198 GHz. The measured phase noise in fractional-N mode is shown in Fig. 6(b), also achieving an integrated jitter of 690 fs. Compared with the integer mode, only minor phase noise degradation was observed in fractional-N mode owning to the minmial delay inserted on the reference path, which is used for calibration of the VCO phases only. The measured output spectrum in fractional-N mode is shown in Fig. 6(c). A closest spur at 2.08 MHz of -42 dBc was measured. The spur completely falls within the loop bandwidth, thus it experiences no suppression from the loop filter. Fractional-N operation with wide loop bandwidth is challenging due to lack of spur attenuation by the loop filter.

The robustness of our proposed SSPLL at the presence of external interference has also been tested as shown in Fig. 7, where a step voltage of 200 mV was inserted on the RO's Vcc. In response to this perturbation, the lock detection signal in the loop switching controller instantly goes down, indicating the phase loop loses lock. The gain of the SSL is decreased while the gain of the FPL is increased. However, the total loop gain remains almost constant, leading to a stable loop dynamics during switching. After locking is regained with help of the FPL, the PLL switches back to the SSL for SS operation.

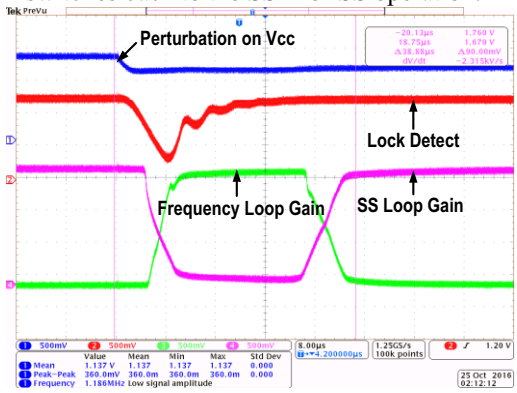


Fig. 7. Measured transient loop switching behaviour, demonstrating robust relocking when SS loop loses lock due to a perturbation on Vcc.

V. Conclusions

The SSPLL presented in this paper demonstrated a compact inductor-less design which is technology scalable. By using a multi-ring coupled ring oscillator, fractional-N mode can be implemented with little extra complexity and power. Through using the proposed coupled multi-rings with proper phase shift and the sub-sampling loop with a wide loop bandwidth, the phase noise degradation from using ring oscillators can be largely eliminated. A measured integrated jitter of 571 fs and 690 fs has been achieved in integer mode and fractional-N mode, respectively, achieving a FoM of -230 dB without using high reference injection.

Acknowledgement

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Table.1 Measured PLL Performances and Comparisons.

	Nandwana [5] JSSC15	Liang [6] ISSCC15	Marucci [7] ISSCC14	**This work**
Architecture	Ring+PI	Ring+PI	MDLL	**MRO+ SS**
Technology	65nm	40nm	65nm	**130nm**
Ref. (MHz)	50	26	50	**50**
Output Freq. (GHz)	4.25-4.75	2.002	1.6-1.9	**0.8-1.3**
In-band PN (dBc/Hz)	-103	-91	-112	**-121**
Int. RMS Jitter (ps)	1.46	2.36	1.4	**0.69**
Frac. Offset Freq. (MHz)	9.78	0.002	0.72	**2.08**
In-band Frac. Spur (dBc)	-50.1	-70	-47	**-42**
Power (mW)	11.6	9.1	3	**19**
FoM (dB)	-226	-223	-232	**-230**

$$FoM = 10log\left(\left(\frac{\sigma_t}{1s}\right)^2 \cdot \frac{Power}{1mW}\right)$$

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