Effect of CMOS Device Sizing on Circuit Noise Performance

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***Abstract*—An often-overlooked but important CMOS device sizing approach that significantly affects circuit noise performance has been discussed theoretically and verified by simulation. It has been demonstrated that sizing a CMOS device using maximum number of gate fingers results in as much as 9dB improvement in circuit noise figure. Furthermore, and as side benefits, parasitic capacitance, linearity, and power consumption are also improved considerably. For the purpose of simulation, Common-Gate Low-Noise Amplifier (LNA) has been utilized as the reference circuit. The simulation has been carried out using 0.12µm CMOS process.**

***Index Terms*—CMOS, device sizing, interdigitated gate, linearity, multi-finger, noise, parasitic capacitance, power consumption.**

I. INTRODUCTION

The thermal noise due to the Ohmic sections of the MOSFET has generally been ignored in noise modeling and performance analysis [1]. For long transistors, this assumption might be acceptable to some extent, as the drain and source resistance is typically negligible [1]. However, as the device scales down, the thermal noise due to the Ohmic resistance becomes noticeable. Particularly, the Gate resistance contributes significantly to the degradation of noise performance.

Figure 1 illustrates the basic geometry of a MOSFET, where W, L_g, and y represent the Width, Length, and the Height of the Gate, respectively.

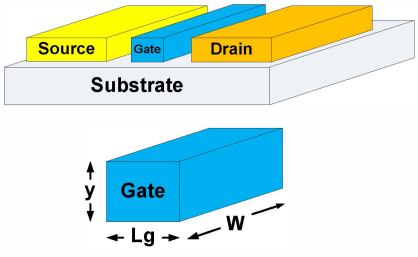

Figure 1. Basic geometry of the MOSFET.

The Gate Resistance, R_g, may be derived as follows [2]:

$$R_g = \frac{\rho W}{3 y L_g} \tag{1}$$

where ρ is the resistivity of the Gate material, and the factor 3 in the denominator is due to the distributed nature of gate resistance [3]. It is clear that by scaling down the transistor, R_g increases due to its inverse proportionality with the Gate length, L_g . Equation (1) also reveals a very important fact; namely, the direct proportionality of Gate resistance with the transistor's Width, W. In other words, increasing transistor's width will increase the Gate resistance, and consequently, its thermal noise. This is a very important conclusion. That is, in order to minimize the thermal noise of the Gate, the width, W, of the transistor must be kept the smallest possible.

The above conclusion is generally overlooked in analyses, and one of the key objectives of this paper is to emphasize that in RF circuit design, the minimum device width permitted by a given process technology must be utilized in order to improve noise performance. There are other desirable side effects in using the smallest device width; e.g., larger output impedance, lower parasitic capacitance, and lower power consumption. These statements will be supported with simulation results in Section III.

Another observation from (1) is that by increasing the height of the Gate, , the Ohmic resistance is reduced. Obviously, the height of the Gate is dependent on the process technology utilized, and is outside of the designer's area of influence. Nevertheless, in discrete Microwave transistors, the Gate is generally T-shaped, hence the name T-Gate, in order to increase its cross-section and reduce its resistance.

The last parameter in (1) that deserves attention is the Gate or channel length, L_g. It is evident that by increasing the Gate length, its resistance decreases; however, for high-frequency applications, the Gate length is generally kept at the minimum allowed by the process technology.

Although the above discussion identifies the elements that contribute to the Gate's thermal noise, it does not provide much flexibility to an IC designer in sizing the transistor for low-noise applications.

The organization of this paper is as follows: in Section II, the device sizing strategy for low-noise applications will be discussed followed by simulation results in Section III. Section IV will provide the performance summary for the proposed device sizing approach, and the conclusions will be drawn in Section V.

II. DEVICE SIZING FOR LOW-NOISE APPLICATIONS

While (1) did not explicitly provide a flexible parameter to control the Ohmic resistance of the Gate, fortunately, there is a design parameter that affects the Gate resistance, and may be controlled by the designer. This parameter is the number of Gate fingers.

Figure 2 illustrates the MOSFET with Multi-Finger Gate.

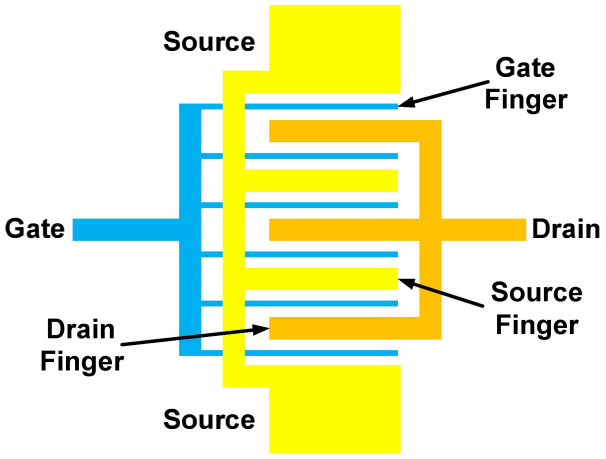

Figure 2. Multi-finger geometry of the MOSFET

The Multi-Finger Gates are connected in parallel; resulting in the Gate resistance to be reduced by a factor of m^2 [2], where m is the number of Gate fingers. Consequently, (1) may be revised as follows to accommodate the number of fingers:

$$R_g = \frac{\rho W}{3m^2 y L_g} \tag{2}$$

Clearly, the number of fingers plays a significant role in the reduction of Gate resistance and ultimately its thermal noise contribution. Equation (2) suggests that for low-noise performance, especially at high-frequencies, the device must be sized primarily by using the number of fingers, and other dimensions shall be kept the minimum permissible by the process technology.

The above conclusion is so important, and will be verified by simulation in Section III.

Before proceeding to the simulation results, a brief reference to some of the previous relevant work is in order.

As the authors of [4] have stated, while multi-finger devices have extensively been used, their properties have not been extensively studied in the literature. For example, even though their noise improvement properties have been studied to some extent, their effect on parasitic capacitance, linearity, and power consumption have not been discussed, hence the absence of any rule on the appropriate number of fingers that shall be used for a given design objective.

While (2) is a simple, yet important, expression that highlights the major elements affecting the Gate resistance in a multi-finger device structure, a different and more involved expression for the equivalent lumped gate resistance as a function of both the number of fingers and interconnects has been presented in [5].

Additionally, and as another evidence to the positive impact of the number of fingers on the noise performance of circuits, [6] has demonstrated that the equivalent input-referred noise voltage is divided by the square root of the number of fingers.

Finally, in [7], the number of fingers was used as a variable to obtain the optimum noise figure and gain for the very low-voltage and low-power LNA.

We are now at a position to discuss the circuit topology that will be used for simulation purposes.

Figure 3 illustrates the single-ended tuned Common-Gate amplifier topology that will be utilized in the verification of the effect of Gate fingers on noise and other performance characteristics such as input return loss, gain, parasitic capacitance, and power consumption. The load tank inductor, L_1 , and the capacitor, C_1 , have been sized such that they resonate at 1.96GHz, the center frequency of the PCS downlink band.

Often, the Common-Gate amplifier is characterized as a noisy configuration. This choice has been made deliberately to demonstrate how the proposed Multi-finger device dimensioning will change the common perception of this amplifier topology from being too noisy to one with comparable noise performance to other configurations.

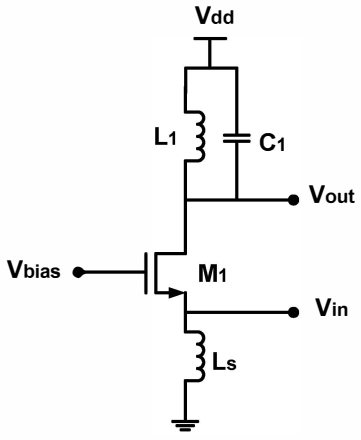

Figure 3. Single-ended tuned Common-Gate Amplifier

For input power matching purposes, the following equation must hold:

$$g_{m1} = \frac{1}{R_S} = 20mS \quad (3)$$

where g_{m1} and R_S are the transconductance of transistor M_1 and the source impedance, respectively.

In Section III, for the same transconductance (i.e., 20mS) and load tank component values, transistor M_1 will first be sized solely by modifying its Width, W, while keeping the Length, L, the minimum permissible by the process technology and setting the number of Gate fingers equal to one (1). We will, hereinafter, call this method of device sizing the "Width-only device dimensioning." Then, the transistor will be sized by keeping the Width and the Length the minimum permissible by the process, and setting the number of Gate fingers appropriately. We will call this second method of device sizing the "Finger-only device dimensioning."

The simulation results for the "Width-only device dimensioning" and "Finger-only device dimensioning" will clearly demonstrate the significance of the effect of the number of fingers on circuit performance.

While at the time of publication of [4] and [5] circuit simulators did not support multi-finger devices, and such devices were treated as very wide transistors, and that there was no visibility into the effect of the number of fingers on the noise performance of the devices, in today's circuit simulators, the effect of both the gate resistance and the gate interconnect resistors of multi-finger devices are taken into account, and the simulation results that follow will demonstrate this cumulative effect.

III. SIMULATION RESULTS

Before we proceed with reviewing the simulation results, it shall be noted that the parasitic effects of the device and the components of Fig. 3 were included in all simulations.

Figure 4 illustrates the noise figure of the circuit of Fig. 3 when the transistor is sized with both Width-only and Finger-only dimensioning approaches.

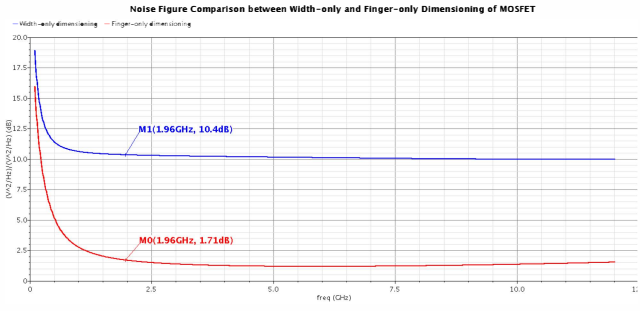

Figure 4. Noise Figure comparison for Width-only and Finger-only dimensioning approaches.

Figure 4 clearly demonstrates the superiority of the Finger-only device dimensioning in achieving excellent noise performance. The improvement with the Finger-only approach is about 9dB on average. This result also invalidates the statement made in [8] that the theoretical minimum noise figure of the common-gate configuration is 2.2dB.

A similar effort to this paper was made in [9], where up to 4dB of improvement in minimum noise figure was demonstrated by increasing the number of fingers from 6 to 72 for both 65nm and 80nm devices and over a frequency range of 200MHz – 18GHz.

While we acknowledge that the Width-only device dimensioning is rarely used for RF applications (e.g., LNAs, Mixers, and Oscillators), it is not uncommon to encounter it in current mirrors that bias these RF devices, whose noise has direct and significant effect on the overall circuit noise performance. Furthermore, we acknowledge that circuit-level noise cancellation techniques (e.g., capacitive cross-coupling and cross-coupled transistor pair) have also been introduced [10-11]; however, device-level approaches such as that proposed here, are general, technology-independent, and do not introduce and require additional components.

As mentioned earlier, there are other circuit performance characteristics that benefit from and are improved by utilizing the Finger-only device dimensioning approach. One such characteristic is the Gain of the amplifier.

Figure 5 illustrates the voltage gain of the circuit of Fig. 3, where the transistor is sized using both the Width-only and the Finger-only dimensioning approaches.

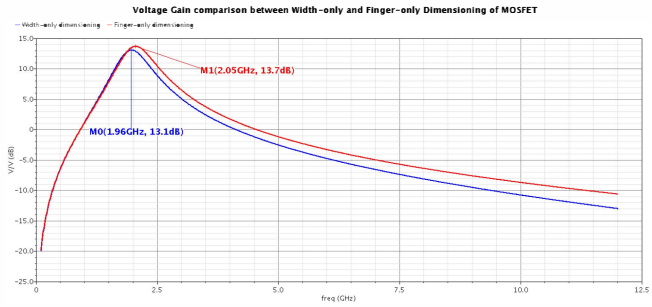

Figure 5. Voltage Gain comparison for Width-only and Finger-only dimensioning approaches.

Figure 5 confirms that the Finger-only device dimensioning approach provides 0.6dB higher gain than that of Width-only approach. Furthermore, given that the load tank component values have been kept identical for both of these device dimensioning approaches, the 90MHz upward shift of the peak gain frequency in the Finger-only approach confirms that the parasitic capacitance of the transistor in the Finger-only approach is smaller than that of the Width-only approach; i.e., the output impedance is larger, as claimed earlier in this paper.

Comparison of the current draw of the circuit in both device sizing approaches reveals that the Finger-only approach draws 0.6mA less current; i.e., it consumes 0.7mW less power than its Width-only counterpart. Although the power consumption improvement does not appear significant at first glance, it shall be noted that in a multi-transistor circuit topology, this small gain will become significant. In summary, the Finger-only device dimensioning approach provides another method of reducing the power consumption of the

circuit, and, in the case of an amplifier, achieving higher voltage gain.

The last, but not the least, performance characteristic that will further demonstrate the importance of device dimensioning approach on circuit performance is the input return loss.

Figure 6 illustrates the input return loss (S_{11}) of the circuit in Fig. 3, where the transistor is sized with both Width-only and Finger-only dimensioning approaches.

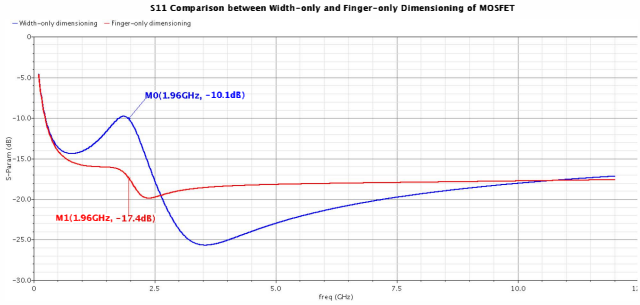

Figure 6. Input Return Loss (S_{11}) comparison for Width-only and Finger-only device dimensioning.

As expected, the input return loss of the circuit when Finger-only dimensioning is utilized is superior to that of Width-only dimensioning. For example, near the resonance frequency of the tank, the Width-only approach produces -10dB of return loss. If wire-bonding and parasitic effects associated with pads are considered, the return loss will degrade further. Additionally, the Width-only approach does not produce a monotonic behavior. In contrast, the Finger-only approach provides significantly better input return loss at the tank resonance frequency, and guarantees acceptable input return loss even when the wire bonding and parasitic effects due to pads are considered.

IV. Performance Summary and Comparison

Table I provides the performance summary and comparison for the Width-only and Finger-only device sizing approaches at the center frequency of the amplifier tank; i.e., 1960 MHz.

TABLE I. CIRCUIT PERFORMANCE SUMMARY AND COMPARISON

Parameter	Width-only	Finger-only
Noise Figure (dB)	10.4	1.71
Voltage Gain (dB)	13.1	13.7
Input Return Loss, S_{11} (dB)	-10.1	-17.4
Drain Parasitic Capacitance [a]	C_D	$0.91C_D$
Power consumption (mW)	P_o	$P_o - 0.7$

a. C_D represents parasitic capacitance seen from Drain when device is sized using Width-only approach

Table I clearly confirms that the Finger-only device dimensioning has superior performance to Width-only approach for all important circuit parameters.

The most noticeable parameters affected by device dimensioning approach are as follows: noise figure, input return loss, and parasitic capacitance. While the 9dB improvement in noise figure is the main message of this paper, other equally-important enhancements such as the 9% reduction in the parasitic capacitance of the device and 0.7mW saving in power consumption are also significant achievements at no cost.

It is worth mentioning that all devices in [12] were sized using the Finger-only dimensioning approach; as such, the circuit exhibited the lowest noise figure and power consumption in comparison to other published works as referenced therein.

V. Conclusion

The effect of device sizing approach on circuit noise performance is reviewed theoretically and confirmed by simulation. It has been demonstrated that the finger-only device dimensioning approach yields significant improvement in noise performance. It has also been shown that lower power consumption, less parasitic capacitance, higher gain, and significantly better input return loss are achieved as a result of employing this technique.

Given the all-positive effects of the Finger-only device dimensioning on key circuit performance characteristics, it is imperative to utilize this method in device sizing.

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