

A 3mW 8-Bit Radiation-hardened-by-design DAC for Ultra-wide Temperature Range from -180°C to 120°C

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Abstract- This paper presents an 8-bit low power digital to analog converter (DAC) with radiation-hardened-by-design (RHBD) for cryogenic applications. Implemented in a 0.5 μ m SiGe BiCMOS technology, this cryogenic DAC is capable of operating over an ultra-wide temperature (UWT) range from -180°C to +120°C and under high-energy particle radiation environment on the lunar surface. A segmented R-2R binary code with thermometer code architecture is used for the DAC core, and a quadrature layout is used to improve the matching. The DAC achieves a measured differential nonlinearity by integral nonlinearity (DNL/INL) of $\pm 0.2/0.3$ least-significant-bit (LSB) in 27°C and $\pm 0.6/0.9$ LSB in -180°C. It consumes only 1mA current and occupies only 0.25mm² die area.

Keywords: DAC, cryogenic circuits, UWT, RHBD, SiGe.

I. INTRODUCTION

With the development of aerospace exploration, the considerations for extreme environments have been included more comprehensively into most designs related to aerospace engineering. The extreme environments, such as temperature, radiation, pressure, vibration, etc, will easily preclude the use of conventional terrestrial engineering designs for operation, actuation and movement under ambient conditions. Although the moon is relatively close to the earth and the radiation level there is not too high, the extreme temperature conditions on the lunar surface can still invalidate conventional electronic components and systems for control, sensing, and communication. This is problematic, since the development of modular, expandable, and reconfigurable human and robotics systems for lunar missions clearly requires electronic components and integrated packaged electronics modules which can operate robustly without external thermal control.

For use on the NASA Lunar-Mars series of missions, a data acquisition system is being developed. The unit will accept inputs from multiple types of sensors, employing three types of input channels that each incorporates programmable elements to accommodate a wider variety of input signals. The extreme space environment of those projects gives tough challenges to even aging circuit technologies. This paper presents an 8-bit DAC which is a key part of the NASA data acquisition system for a sense-and-control circuit. To save the precious energy and weight in space equipment, this DAC is required to be optimized for low power and small size. Although the speed of this DAC is not a big concern, but the linearity and power consumption are crucial for the NASA

application. Moreover, this design has to consider both extreme temperature and radiation environments.

The chosen SiGe BiCMOS technology for this design inherently provides both novel bipolar devices (SiGe HBTs) and Si CMOS. Unlike conventional Si transistors, SiGe HBTs are very well suited for operation in the lunar environment [1]. The addition of Ge allows tailoring of the device bandgap which can be used to optimize device behavior as a function of temperature. SiGe BiCMOS offers unparalleled low temperature performance, wide temperature capability, and optimal mixed-signal design flexibility at the monolithic level by offering power efficient, high speed SiGe HBTs and high density Si CMOS [1][2].

This paper presents the design of an 8-bit low-power radiation-hardened-by-design (RHBD) DAC for cryogenic applications. In Section II, the circuit structure and design considerations are presented. Section III describes the RHBD layout rules. The measurement results and some discussion are given in section IV. Finally, the conclusions are drawn in Section V.

II. CIRCUIT DESIGN

This cryogenic DAC comprises a segmented R-2R 8-bit DAC core, a digital logic part, an ultra-wide temperature (UWT) band-gap reference and a differential to single output convertor.

By considering the low power requirement and extreme application environment, an R-2R resistor ladder structure is selected for this design. This structure is more robust than other DAC structures for its simplicity and using less active component. It also consumes less current than the current-steering DAC structure for using only one current source and its capability to achieve smaller current for the LSB branch. If using only binary code for all 8 bits, the switching of MSB will introduce large glitch on the output signal in the transition time. On the other hand using thermometer code can reduce the output glitch and also relax the matching but occupy more area. By balanced considering the tradeoff, the DAC is segmented as 5 LSBs with R-2R binary codes and 3 most significant-bits (MSBs) with thermometer codes, as shown in Fig. 1.

To achieve the low power design requirement, only 400 μ A total is designed to be supplied to the R-2R resistor ladder so that the divided current drawn on the LSB branch is less than 2 μ A. On the other side, the value of the resistors used in the R-2R resistor ladder is limited for small area requirement.

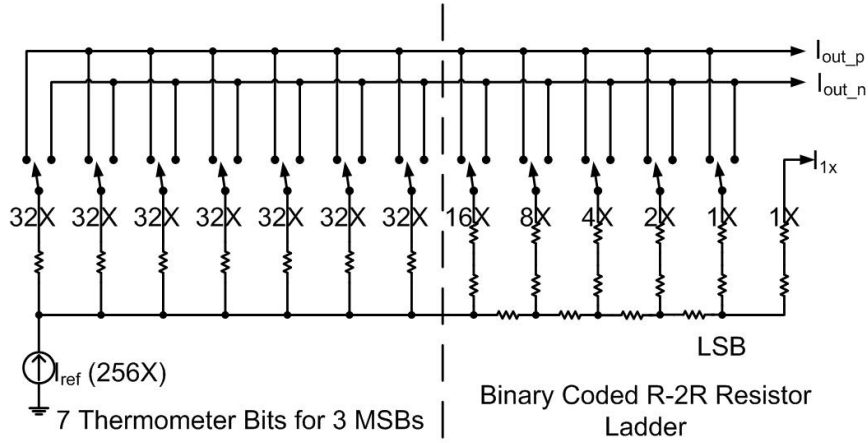


Fig. 1. 8-bit segmented architecture for the DAC core.

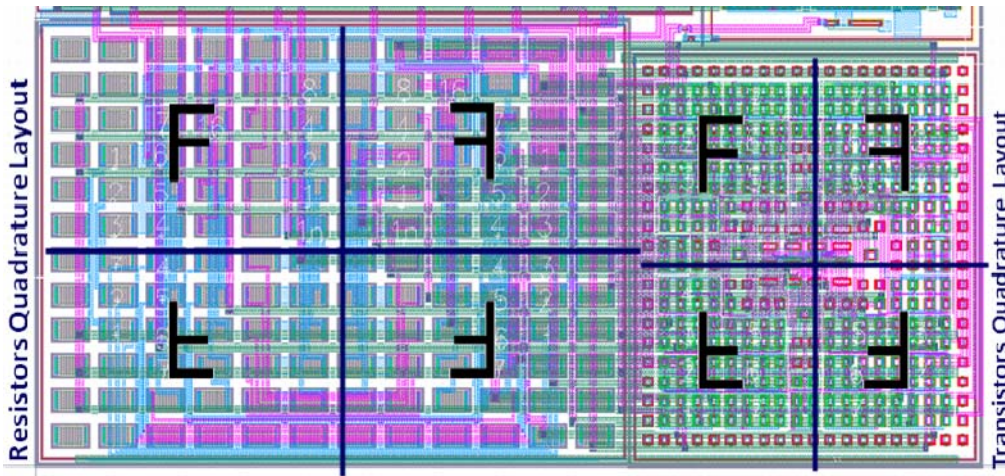


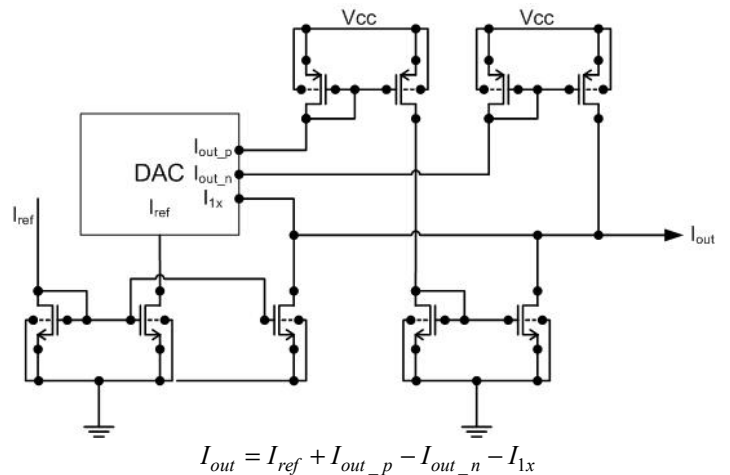
Fig. 2. Quadrature layout for resistors and transistors.

Therefore, the matching is a big challenge for this design. To improve the matching and linearity, all the resistors and most transistors used in the ladder are integer multiple of a base size one, and then the base size resistors and transistors are divided again into four parts to allow a quadrature layout style as shown in Fig. 2. This technique compensates the effects of gradients or other systematic mismatches [3][4]. The measurement results in Section IV show the good linearity results achieved by these design considerations.

The digital logic part of the DAC includes a thermometer decoder which converts 3 binary MSBs to 7 thermometer code and clocked input buffers for the input bits of the DAC.

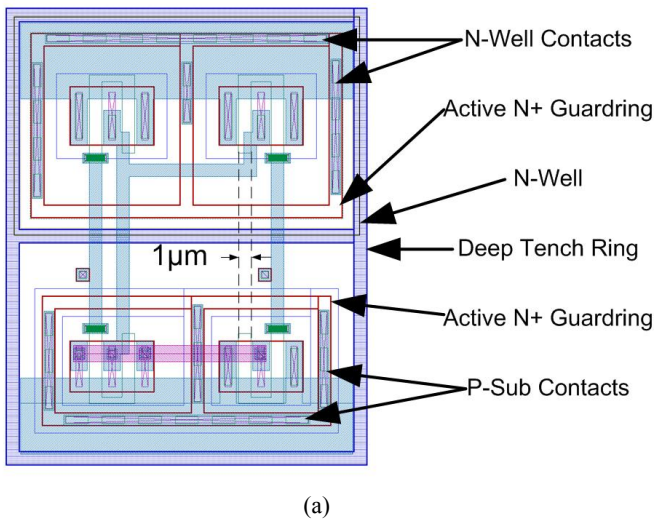
As shown in Fig. 3, by using several accurate cascode current mirrors to realize the current addition and subtraction, the output convertor converts the differential current output from the DAC to a single current output with full swing from $0\mu\text{A}$ to $32\mu\text{A}$ which is required by the NASA project architecture. The output current signal is centered on the DC current of I_{ref} . As shown in Fig. 1, the reference current source for DAC provides 256 times LSB current while the full swing output of both positive and negative differential outputs are 255 times LSB current. Therefore, to reach $0\mu\text{A}$ as lower

bound of the single output swing, the amount of the current on one LSB branch is output from DAC and subtracted from the output current.

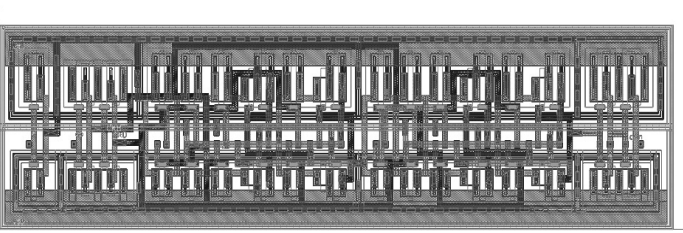


$$I_{out} = I_{ref} + I_{out_p} - I_{out_n} - I_{1x}$$

Fig. 3. Current differential to single output convertor. (cascode transistors are not shown in figure for simplification)



(a)



(b)

Fig. 4. (a) NAND gate by RHBD layout rules; (b) D-flip-flop by RHBD layout rules

A UWT band gap reference is used and tuned to give a constant current output in the UWT range [5]. In the post-simulation the temperature coefficient is less than 40ppm from -180°C to 120°C with full swing output.

III. RADIATION HARDENED BY DESIGN

To improve the robustness in the radiation environment: the minimal transistor width is chosen as $1\mu\text{m}$ other than the default $0.5\mu\text{m}$. And to prevent the single event latch-up caused by the positive feedback formed in the parasitic transistors, some special RHBD layout rules are applied in this design to reduce the well/substrate parasitic resistance and reduce the gain product of the parasitic NPN/PNP pairs. The RHBD rules include: active N+ (P+) guard rings are added around PMOS (NMOS); n-well and p-sub contacts are generously and frequently used; deep trench rings are added for isolation between PMOSs and NMOSs; and n-well and n+ source/drain are kept farther apart if possible [6].

Two example cells of RHBD layout in this design is shown in Fig. 4. As shown Fig. 4(a), by using those RHBD layout rules, the die size of this design is enlarged by several times compared with the normal layout without RHBD consideration. As shown in Fig. 4(b), NFETs and PFETs are grouped by function with active N+(P+) guard rings which reduce the area punishment by applying RHBD layout rules. This design still results relatively small area compared with

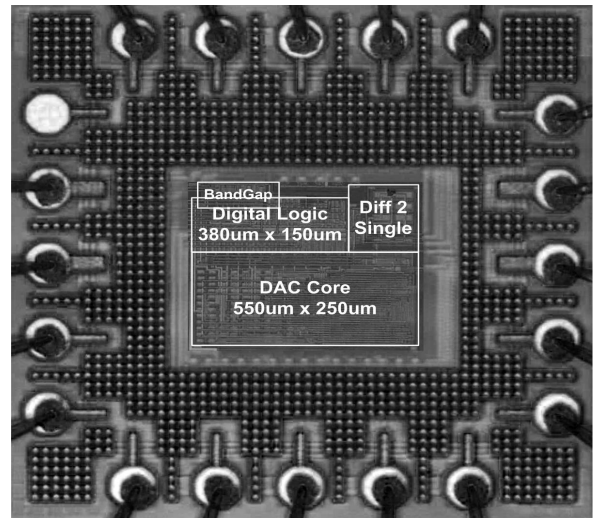


Fig. 5. Die photo of the 8-bit cryogenic DAC.

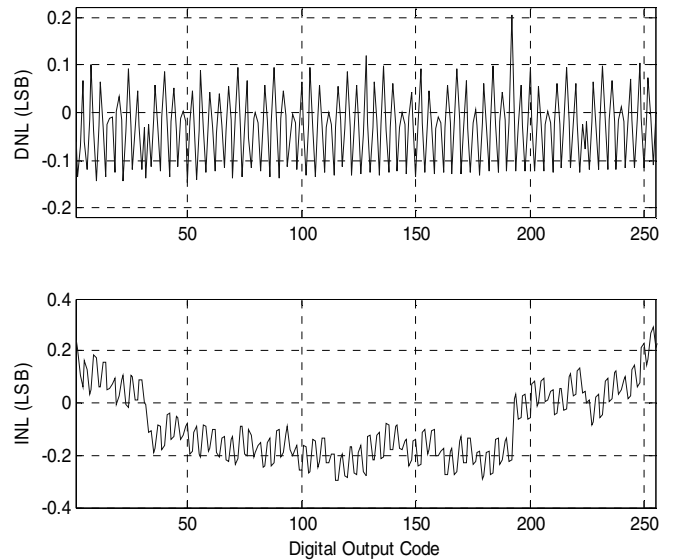


Fig. 6. Measured INL and DNL at 27°C temperature.

similar works by choosing the suitable circuit architecture and good layout floor plan.

IV. MEASURED RESULTS

The die photo of this DAC design is shown in Fig. 5. The active area is $0.55 \times 0.45 \text{mm}^2$ and the DAC core takes $0.55 \times 0.25 \text{mm}^2$.

Fig. 6 shows the measured DNL/INL performance. With the matching considerations in the circuit design and layout, especially the effort of quadrature layout, this design achieved the DNL/INL of $\pm 0.2/0.3$ at room temperature which is a good result for a low-power DAC without any calibration method compared with others work. Except the one big spike in the DNL figure, the DNL for other codes is around ± 0.1 .

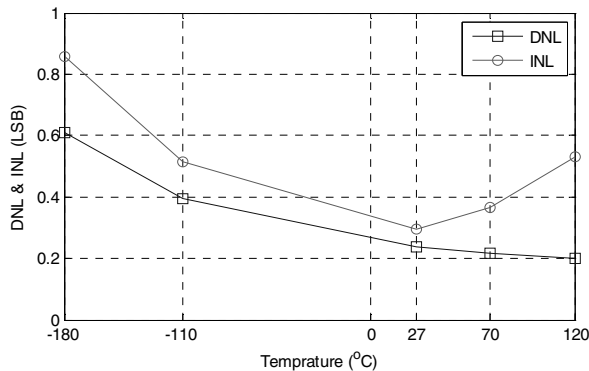


Fig. 7. Measured DNL and INL at from -180°C to 120°C temperature.

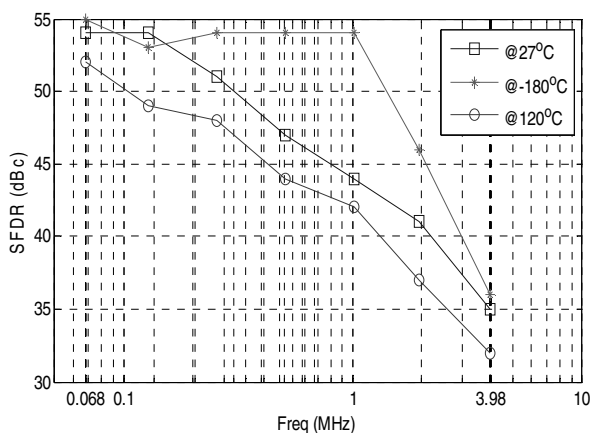


Fig. 8. Measured SFDR at -180°C to 120°C temperature.

The DAC is tested in UWT environment with temperature from -180°C to 120°C. Fig. 7 shows the measured DNL/INL performance over the UWT range. The worst corner is at the temperature of -180°C, the DNL/INL gets to $\pm 0.6/0.85$ LSB. However, it still meets the design spec for ± 1 LSB. And at the high temperature end with 120°C, the DNL/INL gets to $\pm 0.2/0.53$ LSB, which is slightly degraded from the room temperature performance. The INL curve shows the best performance at room temperature as designed for the matching of the design being tuned best at 27°C.

Fig. 8 shows the measured SFDR performance over the UWT temperature range and for the sample frequency to up to Nyquist frequency. The three curves represent the results in -180°C, 27°C and 120°C respectively. As shown in the figure, SFDR has the best performance at the low temperature corner of -180°C with highest SFDR read, 55dB, for low frequency input and widest bandwidth, 1MHz, for optimal SFDR performance. At room temperature, SFDR starts 1dB lower in low frequency and degrades faster with increasing input frequency. The high temperature corner gives the worst SFDR performance, from 52dB to 32dB. Though the performance well meets the project required spec. A summary of measured performance is listed in the Table. 1.

Table. 1. Summary of Measured DAC Performance

Parameter	Performance
Technology	0.5 μ m SiGe BiCMOS
Temperature Range	-180°C ~ 120°C
Resolution	8
Conversion Type	Segmented R-2R and Thermometer
Maximal Sampling Frequency	10 MS/s
Full-scale output	Differential 200uA; Single 32uA
SFDR	55dBc@63k,10MS/s 27°C
DNL/INL	$\pm 0.22/0.3$ at 27°C
Power Supply	3.3 V
Power dissipation	3 mW @ 10 MS/s
Die Size	0.55 \times 0.45 mm ²

V. CONCLUSION

A low power 8-bit DAC for cryogenic applications was developed with improved matching, low power dissipation and optimized die size. Special design considerations were given for the radiation and cryogenic environment. The measured results show that the DAC achieves DNL/INL of $\pm 0.6/0.85$ LSB over the UWT temperature range that meets the NASA requirements.

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